Insert new clauses and corresponding annexes as follows:

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_05_0114.pfd slide 8.

45.2.aa Where should we put PHY-Link registers?

45.2.aa.1 10GPASS-XR PHY Discovery control register (Register x.w, x.x)

The PHY Discovery process is used to bring up new CNUs on the EPoC Coax network. The PHY Discovery control registers direct this process which is fully described in subclause 102.4. The assignment of bits in the 10GPASS-XR PHY Discovery control registers are shown in Table 45–TBD.

Table 45–TBD—10GPASS-XR DS Profile descriptor control registers bit definitions

Bit(s)	Name	Description	R/W[a]
x.w.15:13	PHY Discovery Duration	Duration of next open PHY Discovery window relative to the PHY Frame Counter	R/W
x.w.12)0	PHY Discovery start	Time of next open PHY Discovery window relative to PHY-Link frame counter.	R/W
x.x.15	PHY Discovery open	1=PHY Discovery window is open or is going to open when Frame Counter[9:0] > PHY Discovery Start. 0=PHY Discovery window is closed.	R/W
x.x.14:13	Reserved	Ignore on read	RO
x.x.12:0	PHY Discovery period	Period, in PHY Frames, between PHY Discovery windows. Allows upper layers to control the frequency of PHY Discovery windows. Setting to zero allows upper layers to directly control PHY Discovery window via the PHY Discovery Complete flag	R/W

[a]RO = Read only, R/W = Read/Write

45.2.aa.1.1 PHY Discovery Duration

These bits are used to set the duration, in PHY-Link frames, of the next PHY Discovery window.

45.2.aa.1.2 PHY Discovery start

These bits determine when the next PHY Discovery window is opened.

45.2.aa.1.3 PHY Discovery open

This bit conveys when the PHY Discovery window is or is going to open. When the bit is set to a one via the MDIO interface a PHY Discovery window will be opened when PHY Discovery start is equal to PHY Frame counter (see). Whenever a PHY Discovery window is open the PHY sets this bit to a one. When the

PHY Discovery window closes (i.e., = PHY Frame counter = PHY Discovery start + PHY Discovery period) the PHY sets this bit to a zero. (00–1)

45.2.aa.1.4 PHY Discovery period

These bits determine the repetition frequency of the PHY Discovery window. When set to a non-zero value a PHY Discovery window will be opened once every PHY Discovery period PHY-Link frames. When set to zero a PHY Discovery window is sent the next time PHY Discovery start is equal to the PHY frame counter. if the PHY Discovery open bit is set to a one via the MDIO interface.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_05_0114.pfd slide 8 and should be placed in subclaluse 45.2.1

45.2.1 PMA/PMD registers

45.2.1.60d 10GPASS-XR PHY frame counter bit definitions

The assignment of bits in the 10GPASS-XR PHY frame counter bit definition is shown in Table 45–51d

Table 45–51d—10GPASS-XR frame counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.z.15:0	PHY Frame Counter	Counter that indicates the PHY-Link frame currently being processed by the PHY. This counter rolls over to zero and is incremented at the beginning of each PHY-Link frame	RO

[a]RO = Read only

45.2.1.60d.1 PHY Frame Counter (1.z.15:0)

These bits reflect the current PHY-Link frame count. This counter is incremented at the beginning of the PHY-Link frame and, on terminal count, rolls over to zero.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_06_0114.pfd slide 4.

45.2.1.60e10GPASS-XR DS PHY-Link control register (Register 1.a)

The assignment of bits in the 10GPASS-XR DS PHY-Link control register are shown in Table 45–51e.

Table 45–51e— 10GPASS-XR DS PHY-Link control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.a.15:12	Reserved	Ignore on read	RO
1.a.11:0	DS PHY-Link #1 Start	DS PHY-Link starting sub-carrier from 0 to 4095 in steps of 1 Sub-carriers or Sub-carrier pairs.	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.60e.1 DS PHY Link #1 Start (1.a.11:0)

The DS PHY Link #1 Start bits are used to set the starting sub-carrier (or sub-carrier pair in the case of a device operating with an FFT size of 8k) of the downstream PHY-Link. It specifies the lowest frequency sub-carrier of the downstream PHY-link used to carry PHY-Link information bits. See 102.2.1 for additional details on the downstream PHY-Link.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_06_0114.pfd slide 5.

45.2.1.60f 10GPASS-XR DS PHY-Link search control register (Registers 1.b, 1.c. 1.d)

The assignment of bits in the 10GPASS-XR DS PHY-Link search control registers are shown in Table 45–51f.

Table 45–51f—10GPASS-XR DS PHY-Link search control register 1 bit definitions

Bit(s)	Name	Description	R/W[a]
1.b.15	Reserved	Ignore on read	RO
1.b.14	DS PHY-Link search control	1 = Start a search 0 = Stop a search/search complete	R/W
1.b.13	DS PHY-Link search Status	1 = Indicates a successful completed search 0 = Stop a search/search complete	RO
1.b.12:0	DS PHY-Link search start freq	Frequency at which to start looking for the PLC Channel . From 1 to 5000 MHz in 1 MHz steps	R/W
1.c.15:8	Reserved	Ignore on read	RO
1.c.7:0	DS PHY Link Search Grid Step	Step frequency to use for PHY-Link search. From 1 to 256 MHz in 1 MHz steps	R/W
1.d.15:13	Reserved	Ignore on read	RO
1.d.12:0	DS PLC Search Count	Number of grid steps in search range.	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.60f.1 DS PHY-Link search control (1.b.14)

When this bit is set to a one the PHY is enabled to search for the PHY-Link. When set to a zero by the PHY this bit indicates searching has completed, when set to a zero by the MDIO interface searching is disabled.

45.2.1.60f.2 DS PHY-Link search Status (1.b.13)

When this bit is set to a one the PHY has successfully identified a PHY-Link. When set to a zero the PHY has completed searching and was unable to identify a PHY-Link.

45.2.1.60f.3 DS PHY-Link search start freq (1.b.12:0)

These bits specify the frequency, in 1 MHz steps, at which to begin searching for a PHY-Link.

45.2.1.60f.4 DS PHY Link Search Grid Step (1.c.7:0)

These bits specify the spectrum granularity, in 1 MHz steps from 1 to 256 MHz, the PHY is to use when searching for a PHY-Link.

45.2.1.60f.5 DS PLC Search Count (1.d.12:0)

These bits specify the number of grid steps through which to search for a PHY-Link.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_06_0114.pfd slide 6.

45.2.1.60g 10GPASS-XR US PHY-Link control register (Register 1.e)

The assignment of bits in the 10GPASS-XR US PHY-Link control register 1 are shown in Table 45–51g.

Table 45–51g—10GPASS-XR US PHY-Link control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.e.15:12	Reserved	Ignore on read	RO
1.e.11:0	US PHY-Link #1 Start	US PHY-Link starting sub-carrier from 0 to 4095 in steps of 1 Sub-carriers or Sub-carrier pairs.	R/W

[a]RO = Read only. R/W = Read/Write

45.2.1.60g.1 US PHY Link #1 Start (1.e.11:0)

The US PHY Link #1 Start bits are used to set the starting sub-carrier (or sub-carrier pair in the case of a device operating with an FFT size of 8k) of the upstream PHY-Link. It specifies the lowest frequency sub-carrier of the upstream PHY-link used to carry PHY-Link information bits. See 102.2.2 for additional details on the upstream PHY-Link.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_06_0114.pfd slide 7.

45.2.1.60h 10GPASS-XR DS OFDM channel center frequency control registers (Register 1.f through 1.f+n)

The assignment of bits in the 10g PASS-XR DS OFDM channel center frequency control registers are shown in Table 45–51h.

Table 45–51h—10GPASS-XR DS OFDM channel center frequency control registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.f.15:0	DS OFDM center freq ch1	This specifies the center frequency of sub-carrier 0 of the first OFDM channel transmission.	R/W
1.f+1.15:0	DS OFDM center freq ch1	This specifies the center frequency of sub-carrier 0 of the second OFDM channel transmission.	R/W
1.f+n.15:0	DS OFDM center freq ch1	This specifies the center frequency of sub-carrier 0 of the nth OFDM channel transmission.	R/W

[a]R/W = Read/Write

EDITORS NOTE (to be removed prior to publication); the value of n above will be determined by the number of OFDM channel we allow. Once this is determined this section should be updated.

45.2.1.60h.1 DS OFDM center freq ch1 (1.f.15:0)

These bits specify the center frequency, in steps of 65,536 Hz, of sub-carrier 0 of the first OFDM channel transmission. Since sub-carrier 0 is always excluded, it will actually be below the allowed downstream spectrum band. This definition equates to a center frequency from 0 to 4.29 GHz in 65.54 kHz steps.

*EDITORS NOTE (nOT TO BE INCLUDED IN DRAFT); TD 73 sets the lower bound for TDD spectrum at 10 MHz so it might be useful to adjust the F0 to 106 MHz (10 + 192/2). If so this just needs to be stated in the above definition; either as a **Minimum Value** or as an **Offset**. The proposed definition above is equivalent to the upper 16 bits of the F0 parameter used in MULPI 3.1 (32b f0 in 1Hz steps) per our component commonality agreement. The TF should agree on this parameter definition once to avoid churn in the draft.*

45.2.1.60h.2 DS OFDM center freq ch2 (1.f+1.15:0)

These bits specify the center frequency, in steps of 65,536 Hz, of sub-carrier 0 of the second OFDM channel transmission.

45.2.1.60h.3 DS OFDM center freq ch2 (1.f+n.15:0)

These bits specify the center frequency, in steps of 65,536 Hz, of sub-carrier 0 of the n^{th} OFDM channel transmission.

EDITORS NOTE (to be removed prior to publication); the above definition is to be repeated for each OFDM channel agree upon.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_06_0114.pfd slide 8.

45.2.7a OFDM registers

45.2.7a.1 10GPASS-XR 10GPASS-XR DS Profile descriptor control registers (Register 12.0 through 12.1024)

The assignment of bits in the 10GPASS-XR DS Profile descriptor control registers are shown in Table 45–191a.

Table 45–191a—10GPASS-XR DS Profile descriptor control registers bit definitions

Bit(s)	Name	Description	R/W[a]
12.0.15:12	DS Modulation Type SC3	Modulation to be used for a sub-carrier 3 or sub-carrier pair 6/7	R/W
12.0.11:8	DS Modulation Type SC2	Modulation to be used for a sub-carrier 2 or sub-carrier pair 4/5	R/W
12.0.7:4	DS Modulation Type SC1	Modulation to be used for a sub-carrier 1 or sub-carrier pair 2/3,	R/W
12.0.3:0	DS Modulation Type SC0	Modulation to be used for a sub-carrier 0 or sub-carrier pair 0/1 3210 0000 = null 0001 = BPSK, 0010 = QPSK, 0011 = 8-QAM(support optional), 0100 = 16-QAM (PHY-Link), 0101 = 32-QAM(support optional), 0110 = 64-QAM, 0111 = 128 QAM 1000 = 256-QAM, 1001 = 12-QAM, 1010 = 1024-QAM, 1011 = 2048-QAM, 1100 = 4096-QAM, 1101 = 8192-QAM, 1110 = 16384-QAM, 1111 = Cont. pilots Reserved valued interperated as null on receive	R/W
12.1 - 12.1023	DS Modulation Type SC4 through SC 4096	as above for sub-carrier 4-4096 (8/9 - 8191/8192)	R/W

[a]R/W = Read/Write

45.2.7a.1.1 DS Modulation Type SC3 (12.0.15:12)

These bits specify the modulation type of downstream sub-carrier 3 (or sub-carrier pair 6/7 if FFT size is 8k) for the first DS OFDM channel.

45.2.7a.1.2 DS Modulation Type SC2 (12.0.11:8)

These bits specify the modulation type of downstream sub-carrier 2 (or sub-carrier pair 4/5 if FFT size is 8k) for the first DS OFDM channel.

45.2.7a.1.3 DS Modulation Type SC1 (12.0.11:8)

These bits specify the modulation type of downstream sub-carrier 1 (or sub-carrier pair 2/3 if FFT size is 8k) for the first DS OFDM channel.

45.2.7a.1.4 DS Modulation Type SC0 (12.0.11:8)

These bits specify the modulation type of downstream sub-carrier 0 (or sub-carrier pair 0/1 if FFT size is 8k) for the first DS OFDM channel.

45.2.7a.1.5 DS Modulation Type SC4 through 1023 (12.1 to 12.1023)

These register specify the modulation type of the remaining downstream sub-carriers in the RF spectrum for the first DS OFDM channel. Each register, 1 to 1024, carries the specification for four sub-carriers as detailed above for sub-carriers 0-3 (or 0-7 for 8k FFT).