

EPoC FEC for Passive Coax Plants

Christian Pietsch (Qualcomm)

Stefan Brueck (Qualcomm)

Introduction and Scope

- During the Victoria meeting it was agreed to specify two sets of LDPC codes (prodan_3bn_01_0513.pdf):
 - One code set for passive plants
 - One code set for active plants
- This presentation specifies the LDPC codes for passive plants.

Codes Parameters and Deployment Scenarios

CODES	Rate	Length
A	$R_A = 8/9$	16200
B	$R_B = 8/9$	16200
C	$R_C = 0.848$	5940
D	$R_D = 3/4$	1120
E	$R_E = 41/46$	16560
F	$R_F = 26/30$	10800
G	$R_G = 13/15$	5400
H	$R_H = 3/4$	960

DEPLOYMENT	Passive plant	Active plant
US, low band	F, G, H	B, C, D
DS, low band	E, F, G, H	---
US, high band	E, F, G, H	---
DS, high band	E, F, G, H	A

Code Description

- All LDPC codes for passive plants are quasi-cyclic and binary
- The matrix M to calculate the parity bits has nearly upper diagonal form for all codes
 - Only the first sub-diagonal of the matrix M is non-zero
 - The parity matrices H are constructed so that encoding can be realized with low complexity
- In the following slides the parity check matrices H of the LDPC codes are given
- Description
 - In all tables the top row indexes columns of the parity check matrix
 - The second row of the tables indicates information (1) and parity (0) columns
 - The third row of the tables indicates transmitted columns (1) and punctured columns (0)

Parity Matrices for Codes E and F

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46			
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	.	203	.	.	188	278	.	.	313	56	308	248	206	142	25	309	.	355	257	99	.	42	.	303	197	126	359	308	257	342	113	.	318	109			
0	61	319	106	.	250	153	.	.	283	32	.	.	.	225	.	284	.	132	71	113	.	.	130	173	194	287	129	19	294	307	.	.	265	233	.	274	.	.	318				
.	61	113	.	.	.	268	330	.	.	142	202	.	279	282	.	132	99	.	203	129	26	347	.	74	181	352	84	.	293	353	212	309	.	199	.	.	303	.	210				
.	.	113	183	.	302	.	.	221	153	349	5	334	256	269	.	.	208	61	240	.	40	.	.	194	.	.	.	123	.	.	.	1	147	288	.	109	.	122	333	152	.	275	42	142					
.	.	.	183	244	.	.	89	.	105	.	301	331	.	.	194	.	237	155	.	36	.	.	142	248	.	182	51	51	.	191	.	107	54	91	.	18	254	.	75	225	111	200	116						
.	.	.	.	244	189	45	352	118	.	.	59	.	340	99	267	122	213	.	159	86	.	352	.	.	.	163	151	339	225	326	.	.	147	170	.	.	7	198	110	300	35			

Figure 8: Base code information bits: 41; (max) block length: 46. Lifting: ROTATION SPACE:NESTED CYCLIC:1: 360

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
183	90	.	.	160	295	.	.	268	240	182	127	.	187	.	.	179	288	.	167	14	327	96	.	215	359	.	.	273	344	261
183	0	.	.	.	276	291	.	.	58	308	348	286	.	4	93	.	.	171	.	.	.	207	54	190	352	309	34	223	84	62
.	0	61	.	.	.	184	160	212	235	.	.	.	256	.	39	191	236	303	324	.	.	.	292	.	83	132	189	224	251	142
.	.	61	122	351	.	344	51	.	.	.	267	122	.	284	341	94	335	.	.	256	194	270	.	240	127	351	234	.	202	228
.	.	.	122	175	104	.	206	42	.	91	.	198	329	266	.	.	.	284	269	73	192	.	93	1	.	220	197	44	.	266

Figure 4: Base code information bits: 26; (max) block length: 30. Lifting: ROTATION SPACE:NESTED CYCLIC:1: 360

Parity Matrices for Codes G and H

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	.	.	45	.	92	28	.	137	111	344	2	338	190	258	328	13
0	241	.	.	284	.	.	186	.	198	185	334	76	148	236	93	190
.	241	122	119	171	17	244	303	218	356	258	53	181	330	271	279	150
.	.	122	0	287	36	135	84	72	245	208	303	239	124	176	284	121

Figure 2: Base code information bits: 13; (max) block length: 15. Lifting: ROTATION SPACE:NESTED CYCLIC:1: 360

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0	16	.	.	21	9	.	.	33	44	.	.	15	40	4	56	47
0	1	12	39	42	40	2	.	54	33	32	12
.	1	32	.	.	4	46	50	.	.	44	7	43	47	23	.	48
.	.	32	3	34	.	44	58	8	.	.	54	14	4	.	43	26
.	.	.	3	27	43	41	.	.	38	56	20	20	.	13	16	10

Figure 1: Base code information bits: 12; (max) block length: 16. Lifting: ROTATION SPACE:NESTED CYCLIC:1: 60

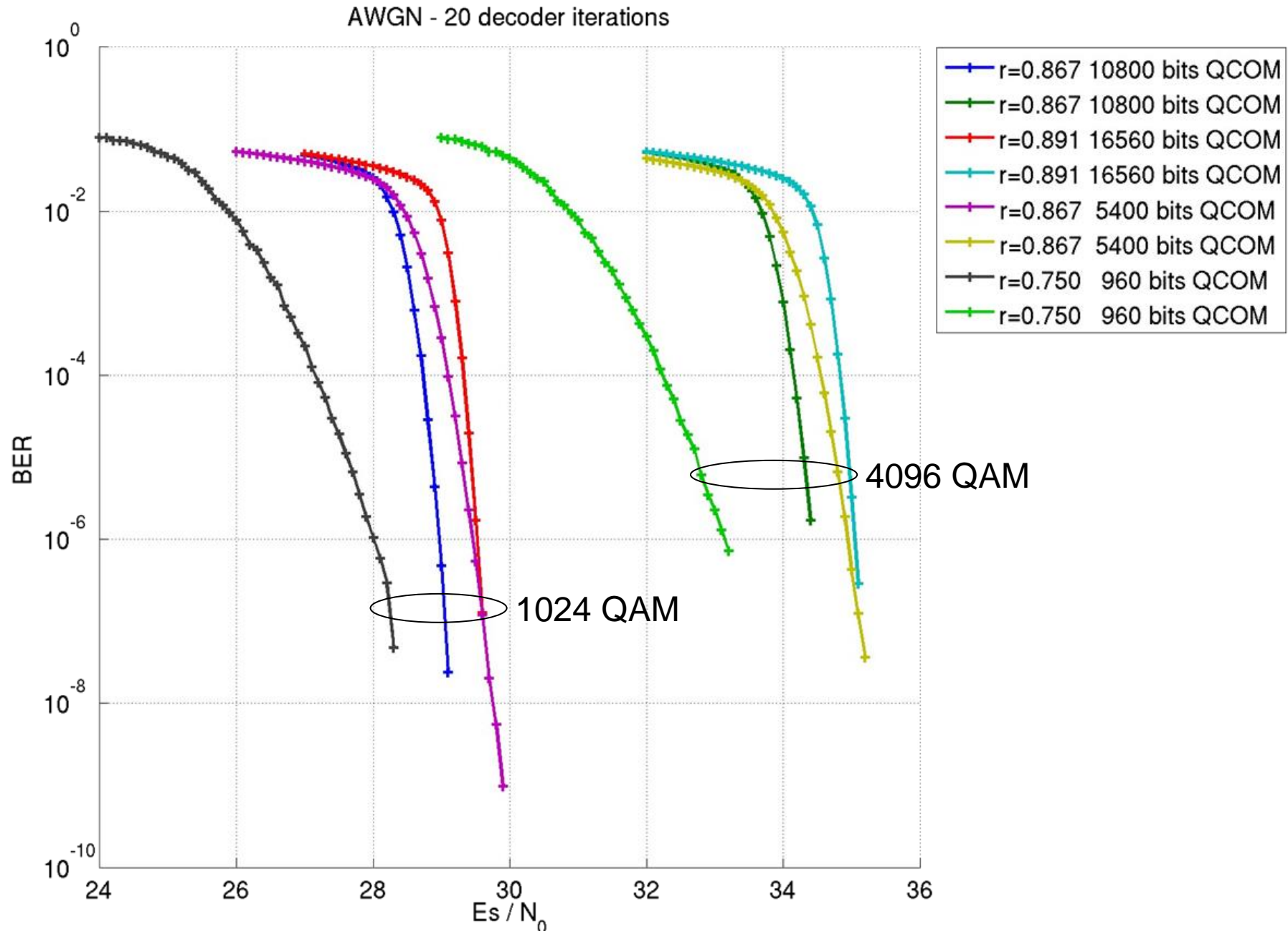
Edge Density, Parity Checks and Lifting Size

Base n	Base k	Rate	Lifting Z	Information Bits	Code word length	Parity checks	Based edges	Edge density
46	41	0.8913	360	14760	16560	2160	154	3.348
30	26	0.8667	360	9360	10800	1800	98	3.267
15	13	0.8667	360	4680	5400	1080 (1440)	54 (56)	3.6 (3.73)
16	12	0.75	60	720	960	300	53	3.3125

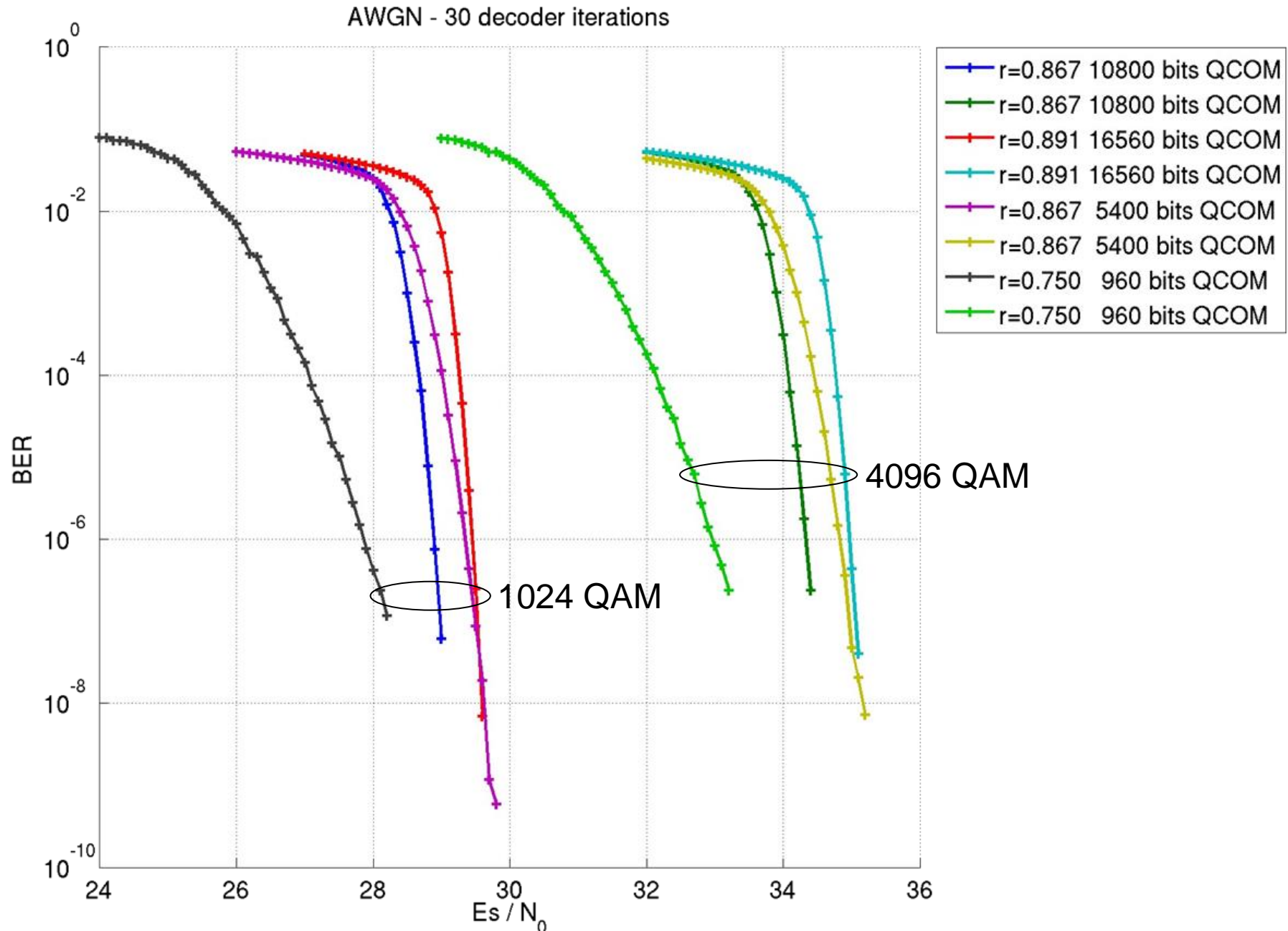
LDPC Decoder Assumptions

- Sum product decoder
- Flooding schedule
 - No layered iterations are applied
- The maximal number of iterations is set to 20 or 30, respectively
 - In the hardware implementation, layered iterations would be applied
 - This allows reducing the number of iterations roughly by 50%
 - Since the implementation and performance of a layered schedule is LDPC code specific, it is not used for code comparison
- Simulation methodology according to [prodan_3bn_02_0313.pdf](#)

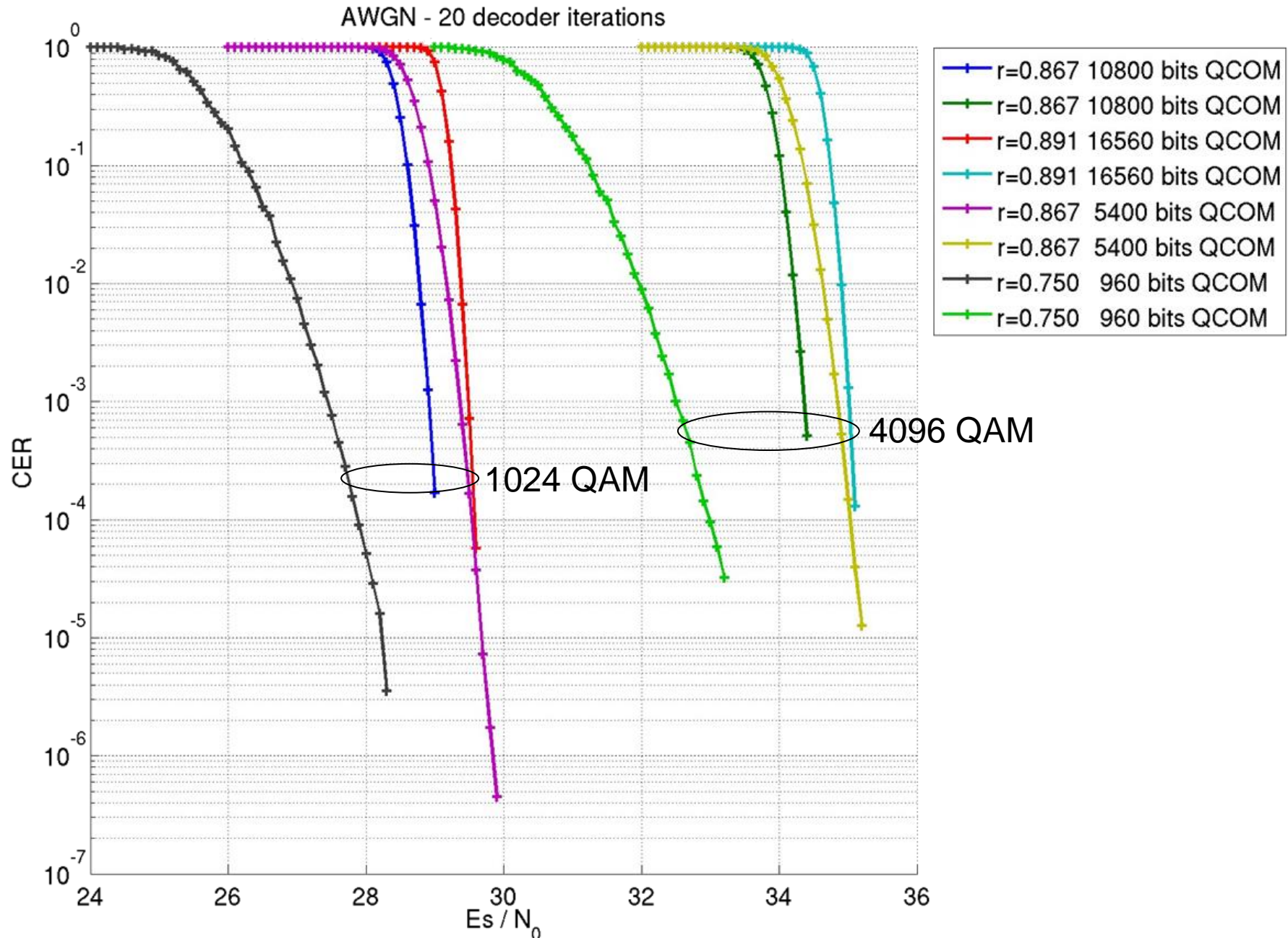
Performance Result: AWGN – 20 Decoder Iterations – BER



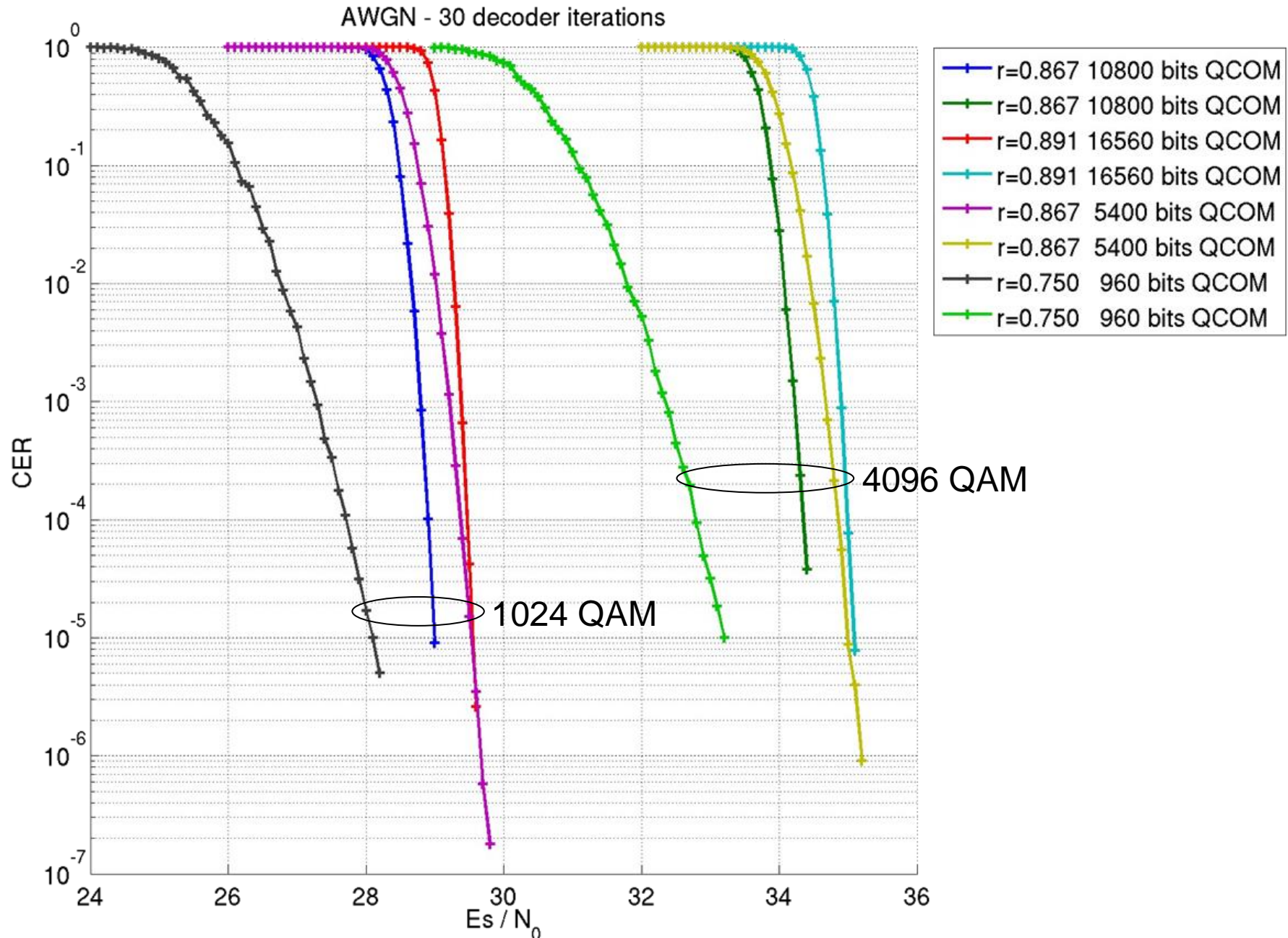
Performance Result: AWGN – 30 Decoder Iterations – BER



Performance Result: AWGN – 20 Decoder Iterations – FER



Performance Result: AWGN – 30 Decoder Iterations – FER



thank you