Some possible MDIO Field definitions for EPoC

A starting point

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PHY Commands

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes	CLT CNU
PHY_Address	Which PHY is targeted	RO?	1			48	MAC address - if we use MAC address on the PHY link we will need a table of ONU MAC addresses n x 48b long. Concept implied in Motion #11 Victoria (see boyd_3bn_02_0513 slide 8). Reviewed in PHY-Link call 6/5	B
Phy_Cmd_Opcode	Enumerated list of commands: NOP, Read, Write, Write/Read	RW	1	0	7	3	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8) Reviewed in PHY-Link call 6/5, some questions about need for this field, may need additional details on how upper layers talk to PHY-Link.	B
Register_Address	MDIO Address of targeted register	RW	1			16	email thread PHY frame (in PHY-Link ad hoc folder). Implied in principle motion #11 Victoria (see boyd_3bn_02_0513 slide 8) Reviewed in PHY-Link call 6/5, some questions about need for this field, may need additional details on how upper layers talk to PHY-Link.	B

Global

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes	CLT CNU
Flag:_Transmit_ enable	allow the CLT to activly transmit, default is disable. Allows PHY to respond to PHY Layer Discovery.	RW	1	0	1	1	Could use **Register 1.9.0** (**Table 45–11**) for this Global PMD Transmit disable except this bit is defined as default = enabled.	B
Flag:_PHY_Layer _Registered	for a CNU PHY this PHY has been registered (i.e,, PHY layer Discover has been completed).	RO	1	0	1	1	Discussed in PHY-Link call	B
Flag:_TDD/FDD	Sets network Mode; TDD / !FDD	RW	1	0	1	1	Discussed in PHY-Link call	B
Tx_Symbol_cou nter	Number of symbols transmitted, rolls over to zero at max count.	RO	1			16	basic PM	B
Rx_Symbol_cou nter	Number of symbols received rolls over to zero at max count.	RO	1			16	basic PM	B
FEC_Pointer	A pointer, in bits, to the first complete FEC codeword in the following PHY_Link frame	RO	1	0	16383	14	Proposed during PHY-Link call 5/1 in EPOC-Downstream-Framing-v0.9.pdf, pointer concept **implied in motion #11** Victoria. Reviewed in PHY-Link call 6/5, may not wish to include as to upper layers this will appear to be random.	B
FEC_Enable	A bit mapped 8 bit register to enable individual FEC code rates. Setting a bit to a logical high enable the FEC code rate. Code rate (listed from bit 0 to 8) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RW	1	0	255	8	Concept proposed/**implied in motion #5** from Victoria (see prodan_3bn_0513.pdf slide 6). Reviewed in PHY-Link call 6/5.	B
PHY_Config_ID	PHY Profile configuration in use, read only	RO	1	0	3	2	Discussed in PHY-Link ad hoc Straw Poll 10 & 11. In the CLT this may need to be a table with an entry for each CNU. **Implied in Motion #11** Victoria (see boyd_3bn_02 slide 8). Reviewed in PHY-Link call 6/5.	B

OFDM Descriptors

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
DS_OFDM_Duration	Enumerated list; 20 or 40 us.	RW	1	0	1	1	based on carrier spacing of 25/50 us (Motion #10, Geneva). Reviewed in RF Spectrum call 6/18.
DS_Cyclic_Prefix_length	Length of DS cyclic prefix for all channels. Enumerated list {0 = .9375 us, 1=1.25 us, 2=2.5 us, 3=3.75 us, and 4=5 us}	RW	1	0	4	3	Aligned with and **implied by Motion #26** Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event. Reviewed in RF Spectrum call 6/18.
US_OFDM_Duration	Enumerated list; 20 or 40 us.	RW	1	0	1	1	
US_Cyclic_Prefix_length	Length of US cyclic prefix. Enumerated list {0= 0.9375 us, 1= 1.25 us, 2= 1.5625 us, 3= 1.875 us, 4= 2.1875 us, 5= 2.5 us, 6= 2.8125 us, 7= 3.125 us, 8= 3.75 us, 9= 4.0625 us, 10= 4.375 us, 11= 4.6875 us, 12= 5 us, 13= 5.3125 us, 14= 5.625 us, and 15= 6.25 us}	RW	1	0	15	4	Aligned with and **implied by Motion #26** Victoria (see pietsch_3bn_02_0313 slide 2). Changing CP is a system reregistration event. Reviewed in RF Spectrum call 6/18.
US_Resource_Block_spectrum	An enumerated list defining the number of sub-carriers in an US Resource Block. {0 = 1 SC, 1 = 2 SC, 2 = 4 SC, and 3 = 8 SC}	RW	1	0	3	2	**Implied in motion #24** Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinement. Reviewed in RF Spectrum call 6/18.
US_Resource_Block_duration	The number of symbols in an US Resource Block from 1 to 17. When FFT size = 8k the maximum value is 17, when FFT size = 4k them maximum value is 9	RW	1	1	17	5	**Implied in motion #24** Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinement. Reviewed in RF Spectrum call 6/18.
US_Resource_Block_Pilot_Spacing	The Pilot spacing in an US Resource Block from tbd to tbd	RW	tbd	tbd	tbd	tbd	**Implied in motion #24** Victoria (see pietsch_3bn_01_0513 slide 3, 4), may been additional details/refinement. Reviewed in RF Spectrum call 6/18.

PLC Descriptor

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Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
DS_PLC_Center_Frequency_#1	Location of the DS PHY-Link center frequency from lower edge of RF Channel. In MHz from 1 to 192 in steps of 1 Mhz.	RW	1	1	192	8	Discussed in PHY-Link ad hoc 3/27. **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 3). Reviewed in PHY-Link call 6/5.
DS_PLC_Cycle_Time_#1	The PHY_Link cycle time, in symbols from tbd to tbd symbols.	RW	1	tbd	tbd	tbd	Discussed in PHY-Link ad hoc 3/27. **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 6). Reviewed in PHY-Link call 6/5.
DS_PLC_Internal_Guard_time_#1	Amount of guard time, in symbols, internal to the PHY-Link cycle.	RW	1	0	tbd	tbd	Discussed in PHY-Link ad hoc 3/27. **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 5). Reviewed in PHY-Link call 6/5.
DS_PLC_Ending_Guard_time_#1	Amount of guard time, in symbols, at the end of of the PHY-Link cycle	RW	1	1	tbd	tbd	Discussed in PHY-Link ad hoc 3/27. **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 5). Reviewed in PHY-Link call 6/5.

PLC Descriptor

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Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
DS_PLC_CRC_Errors_#1	Number of CRC Errors in the most recent period (tbd time). The 10P/2B TC CRC error register is a 16 bit counter that contains the number of TC frames received with the TC_CRC_error primitive asserted, defined in 61.2.3. These bits shall be reset to all zeros when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow.	RW	1	0	tbd	tbd	**Based on Motion #13** Victoria (see boyd_3bn_02_0513 slide 8) Reviewed in PHY-Link call 6/5, rationalize with previous CRC Error counter techniques (see example text).
DS_PLC_FEC_Corrected_Errors_#1	Number of FEC Correctable Errors in the most recent period (tbd time). The 10P FEC correctable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and corrected. ... These bits shall be reset to all zeros upon execution of the MMD reset and upon being read.	RW	1	0	tbd	tbd	**Based on Motion #13** Victoria (see boyd_3bn_02_0513 slide 8) Reviewed in PHY-Link call 6/5, rationalize with previous CRC Error counter techniques (see example text).
DS_PLC_FEC_Uncorrected_Errors_#1	Number of FEC uncorrectable Errors in the most recent period (tbd time). The 10P FEC uncorrectable errors counter is a 16 bit counter that contains the number of FEC codewords that have been received and are uncorrectable. .. These bits shall be reset to all zeros upon execution of the MMD reset and upon being read.	RW	1	0	tbd	tbd	**Based on Motion #13** Victoria (see boyd_3bn_02_0513 slide 8) Reviewed in PHY-Link call 6/5, rationalize with previous CRC Error counter techniques (see example text).

PLC Descriptor

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Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
DS_PLC_Srch_Freq_Start	Frequency at which to start looking for the PLC Channel . From 1 to 5000 MHz in 1 MHz steps	RW	1	1	5000	13	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 3 & 4). Reviewed in PHY-Link call 6/5.
DS_PLC_Srch_Freq_Step	Step frequency to use for PLC search. From 1 to 256 MHz in 1 MHz steps	RW	1	1	256	8	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, **Implied in Motion #1**3 Victoria (see boyd_3bn_02_0513 slide 3 & 4). Reviewed in PHY-Link call 6/5.
DS_PLC_Srch_Cnt	Number of grid steps in search range	RW	1	1	5000	13	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, **Implied in Motion #1**3 Victoria (see boyd_3bn_02_0513 slide 3 & 4). Reviewed in PHY-Link call 6/5.
DS_PLC_Srch_Cntrl	Start and Stop a search	RW	1	0	1	1	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 3 & 4). Reviewed in PHY-Link call 6/5.
DS_PLC_Srch_Status	Indicates a completed search and successful or unsuccessful	RO	1	0	3	2	Discussed in PHY-Link ad hoc 5/1 and presented in Victoria, **Implied in Motion #13** Victoria (see boyd_3bn_02_0513 slide 3 & 4). Reviewed in PHY-Link call 6/5.

PLC Descriptor

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Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
US_PLC_Center_Frequency_#1	Location of the US PHY-Link center frequency.	RW	1	1	192	8	Discussed in PHY-Link ad hoc 3/27
US_PLC_Cycle_time	Number of Symbols? Fixed/Configurable? Fixed in Std?	RW	1	tbd	tbd	tbd	Discussed in PHY-Link ad hoc 3/27 This may be same as DS Frame length

DS Channel Descriptor

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
DS_Center_Freq_Ch1	96 to 4904 MHz in 1 MHz steps. This eqates to channel bounds of 0 to 5000 Mhz. Permissable lower bound TDB.	RW	1	96	4904	13	1 MHz steps & upper bound of 5G **agreed in Motion #17** Orlando. Reviewed in RF Spectrum call 6/18, some discussion on precise description (i.e., center frequency of what).
DS_Lower_Exclusiont_Band_Ch1	Lower Exclusion band upper limit expressed as the distance in Sub-Carriers from lower limit of the RF Channel; 20 (1 MHz) to 4095 in integer number of sub-carriers. If set to 0 then Lower Exclusion band is disabled.	RW	1	0	4095	12	Should this cover full 4k/8k range?
DS_Upper_Exclusion_Band_Ch1	Upper Exclusion band upper limit expressed as the distance, in Sub-Carriers, from upper limit of the RF Channel; 0 (1 MHz) to 4095 in integer number of sub-carriers. If set to 0 then Upper Exclusion band is disabled.	RW	1	0	4095	12	Should this cover full 4k/8k range?
DS_Internal_Exclusion_band_1_Start_Ch1	Internal Exclusion band lower limit, in sub-carriers; 0 to 8192 sub-carriers in steps of 1.	RW	1	0	8192	13	Aligned with and Implied by **motion #15, 17, 19, & 20** Victoria. Still need to determine minimum step size. Reviewed in RF Spectrum call 6/18, note there would be some number of these fields, one for each internal exclusion band.
DS_Internal_Exclusion_band_1_Width_Ch1	Internal Exclusion band width, expressed in sub-carriers, from 20 (1 MHz) to tbd in steps of 1 sub-carriers. A value of 0 disables the exclusion band.	RW	1	20	tbd	tbd	Need to agree on max width

US Channel Descriptor

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
US_Center_Freq_Ch1	101 to 109 MHz in 1 MHz steps. This equates to channel bounds of 5 to 205 Mhz	RW	1	101	109	4	Modeled after DS Channel Descriptor
US_Lower_Exclusion_Band_Ch1	Lower Exclusion band upper limit expressed as the distance in Sub-Carriers from lower limit of the RF Channel; 20 (1 MHz) to 4095 in integer number of sub-carriers. If set to 0 then Lower Exclusion band is disabled.	RW	1	0	4095	12	
US_Upper_Exclusion_Band_Ch1	Upper Exclusion band upper limit expressed as the distance, in Sub-Carriers, from upper limit of the RF Channel; 0 (1 MHz) to 4095 in integer number of sub-carriers. If set to 0 then Upper Exclusion band is disabled.	RW	1	0	4095	12	
US_Internal_Exclusion_band_1_Start_Ch1	Internal Exclusion band lower limit, in sub-carriers; 0 to 4095 sub-carriers in steps of 1	RW	1	0	8191	13	
US_Internal_Exclusion_band_1_Width_Ch1	Internal Exclusion band width, expressed in sub-carriers, from 1 (1 MHz) to 192 in steps of 1 sub-carriers. A value of 0 disables the exclusion band.	RW	1	tbd	tbd	tbd	

CLT & CNU Ability

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
Number of DS OFDM Channels Supported	Indicates the number of downstream OFDM channels supported by the CLT from 1 to 10	RO	1	1	10	4	
Number of US OFDM Channels supported	Indicates the number of upstream OFDM channels supported by the CLT from 1 to 4	RO	1	1	4	2	
CLT_FEC_Capability	A bit mapped 8 bit register to indicate if the CLT PHY supports the individual FEC code rates. A bit set to a logical high indicaste support for a specific FEC code rate. Code rate (listed from bit 0 to 7) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RO	1	0	255	8	FEC concept proposed/implied in motion #5 from Victoria (see prodan_3bn_01_0513.pdf slide 6). Capability register suggesed on PHY-Link ad hoc call on5 Jun 13

Field_Name	Description	R/W	Step	Min	Max	Bits	Notes
Number of DS OFDM Channels Supported	Indicates the number of downstream OFDM channels supported by the CNU from 1 to 10	RO	1	1	10	4	
Number of US OFDM Channels supported	Indicates the number of upstream OFDM channels supported by the CNU from 1 to 4	RO	1	1	4	2	
CNU_FEC_Capability	A bit mapped 8 bit register to indicate if the CNU PHY supports the individual FEC code rates. A bit set to a logical high indicaste support for a specific FEC code rate. Code rate (listed from bit 0 to 7) are; RA = 8/9, RB = 8/9, RC = 0.848, RD = 3/4, RE = 9/10, RF = 9/10, RG = 13/15, and RH = 3/4.	RO	1	0	255	8	FEC concept proposed/implied in motion #5 from Victoria (see prodan_3bn_01_0513.pdf slide 6). Capability register suggesed on PHY-Link ad hoc call on5 Jun 13

Naming

- **Each PHY in 802.3 has a name (see CL 1.4)**
  - Typically refers to the Rate, modulation, line coding and other pertinent info
    - Rate – assumed in Mbps, G indicates Gbps
    - BASE – Baseband modulation. Currently the only OFDM like PHY is 10PASS-TS, an Ethernet variant of VDSL defined in Clause 61 & 62.
    - Line coding
      - X – 8B/10B
      - R – 64B/66B
- **What shall we name the EPoC PHY?**
  - Suggestion:**10GPASS-CR**
    - 10G – 10G rate
    - PASS – OFDM
    - CR – Coax, 64B/66B

Examples	
10GBASE-PR	10G EPON
10/1GBASE-PRX	10/1G EPON
1000BASE-PX	1G EPON
10PASS-TS	10M Eth VDSL

Thank you

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