PHY LINK CHANNEL FEC

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IEEE P802.3bn EPON Protocol over Coax (EPoC) Task Force
July 15-19,2013

PHY LINK CHANNEL (PLC) CONSIDERATIONS

- **Robustness: PLC must be received by new CNUs to enable joining the network**
  - PLC must be very robust to worst case expected channel conditions for the new CNU
    - Worse case SNR a modem should receive data
    - Protect against notches in spectrum caused by reflections
    - Need adding some margin to protect against spurs
  - Shall not use frequencies subjected to known external interference (LTE …)
- **Protection against burst noise**
  - PLC is not interleaved with data
  - PLC frame is separately spread over multiple symbols
  - FEC codeword size
    - Needs to be long enough to overcome expected burst durations
    - Should not be too long to increase the latency

FEC AND REQUIRED ROBUSTNESS

- **Target threshold SNR to received PLC on AWGN channel**
  - Our considerations
    - With 256-QAM the PHY data FEC requires an average SNR of 24 dB with no margin to achieve BER/WER=1e-8/1e-6
    - Worst case attenuation of a group of eight subcarriers due to SCTE 40 reflections is 4 dB
    - Assume some margin for worse loops and/or spurs and/or additional margin taken ~ 4 dB
  - SNR must be around 16(*24-4-4*) dB
- **Propose using rate 75% size 384 FEC code on 16-QAM**
  - Effective PLC data rate is about 1 Mbps
- **Burst Noise**
  - Worst case burst noise:
    - 16 µs @ 5 dB SNR over two OFDM symbols
  - Two OFDM symbols may be impacted by the burst noise
- **Considered FEC codes**
  - BCH (384, 285, t=11) code
    - 74% code shortened from BCH (511, 412, t=11) code. No 75% size 384 BCH code.
  - 6-bits extended RS (64,48) code ((384,288) in binary)
  - LDPC (384, 288) code
    - 75% code from punctured 60% LDPC (480,288) code

PROPOSED RATE 75% (384,288) LDPC CODE

- **75% (384,288) binary punctured LDPC code**
  - Mother LDPC code: 60% (480,288) code
    - 4x10 base parity check matrix with sub-matrix size (lifting value) equal 48.
    - Parity check matrix

16	1	28	9	40	38	16	-1	-1	-1
28	42	36	11	39	9	8	38	-1	-1
5	2	18	16	25	47	-1	2	19	-1
18	18	40	18	0	34	-1	-1	7	32

  - (384, 288) code is obtained by puncturing (480,288) mother code
    - Two periods puncturing
      - Period 1: size 48 start at 48 (puncturing information bits)
      - period 2: size 48 start at 384 (puncturing parity bits)

$\underbrace{a_{287}\cdots a_1 a_0}_{288}$ → **LDPC Encoder** → $b_{479}\cdots b_{288}a_{287}\cdots a_0$

288 information bits

$\rightarrow b_{479}\cdots b_{432}\underbrace{\times\times\cdots\times}_{48}b_{383}\cdots b_{289}b_{288}a_{287}\cdots a_{97}a_{96}\underbrace{\times\times\times\cdots\times}_{48}a_{47}\cdots a_1 a_0$

(2nd period) (1st period)

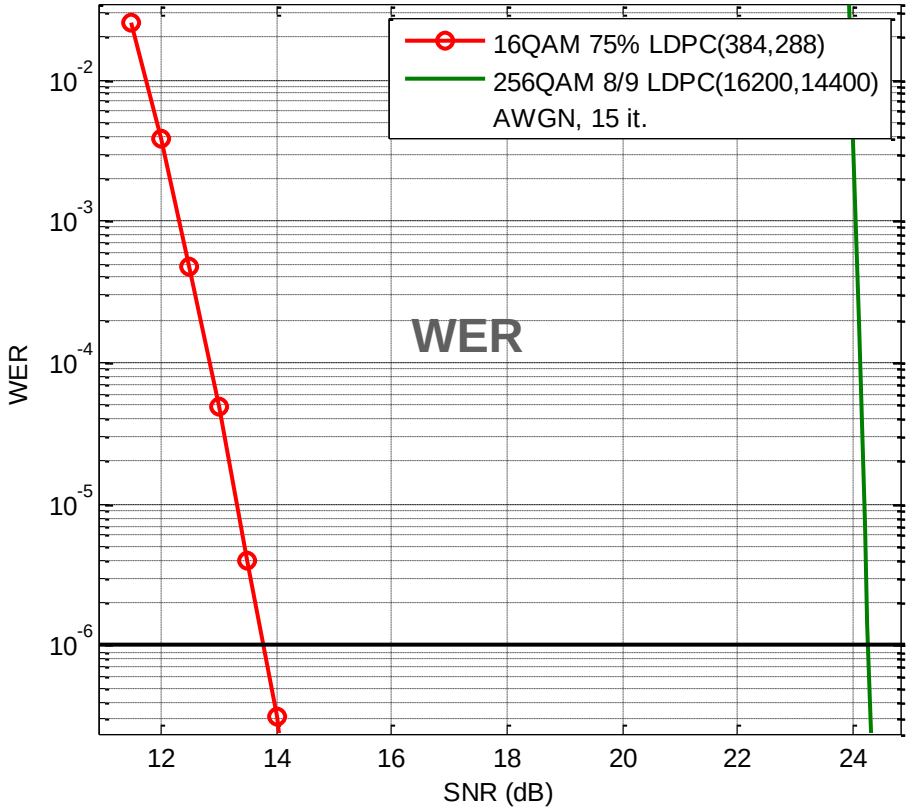
puncture

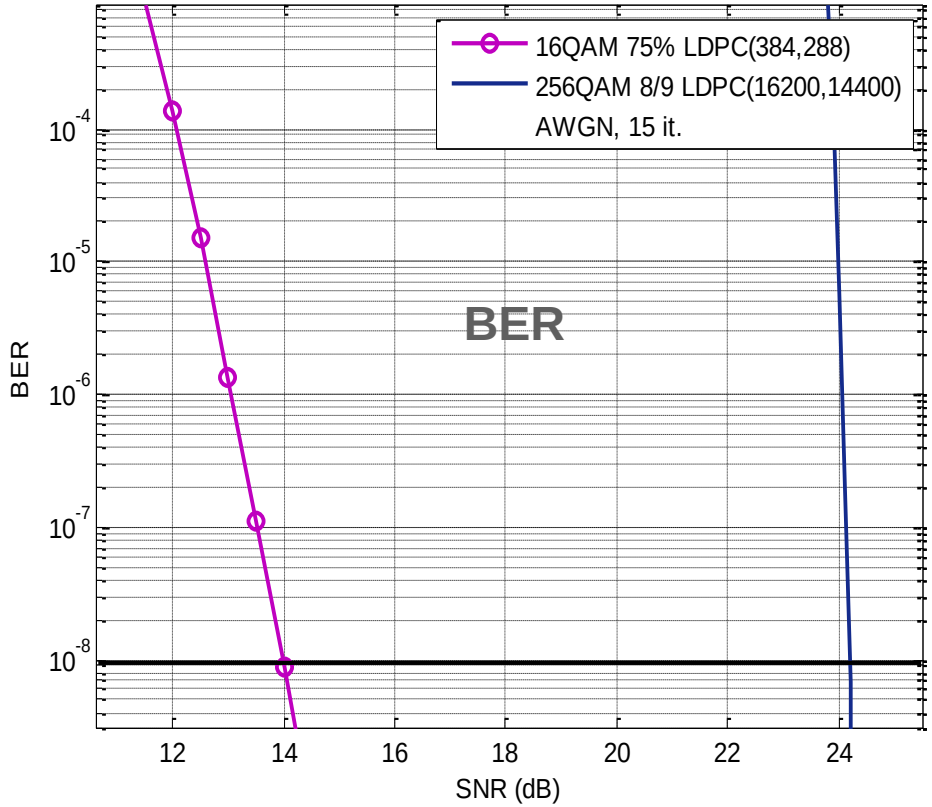
$\rightarrow \underbrace{b_{469}\cdots b_{432}b_{383}\cdots b_{288}}_{144}\underbrace{a_{287}\cdots a_{97}a_{96}a_{47}\cdots a_1 a_0}_{240}$

PERFORMANCE ON AWGN CHANNEL

75% LDPC (384,288) for PLC on 16QAM

8/9 LDPC (16200, 14400) for data on 256QAM

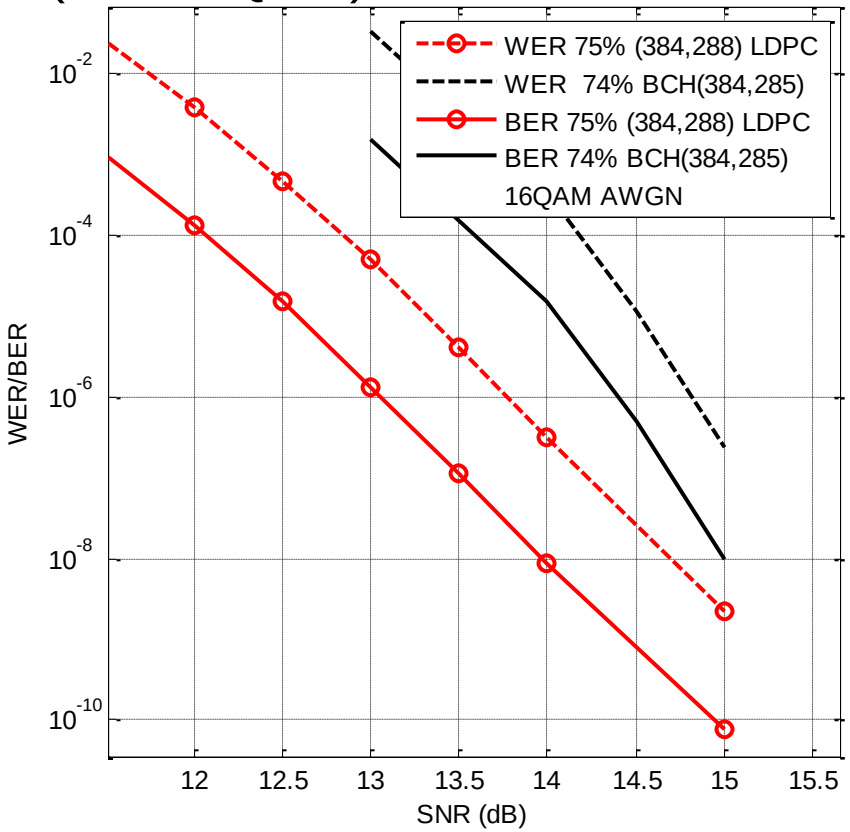




	WER=1e-6	BER=1e-8
75%(384,228)	13.8dB	14dB

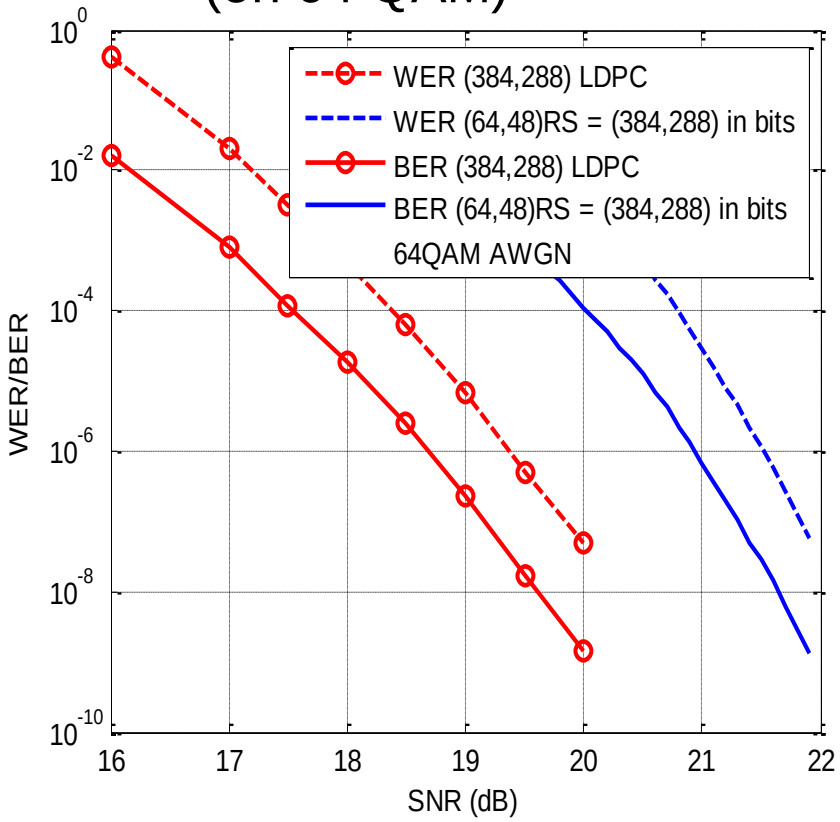
PERFORMANCE COMPARISON TO CLASSICAL CODES

74% BCH (384,285, t=11) (On 16-QAM)



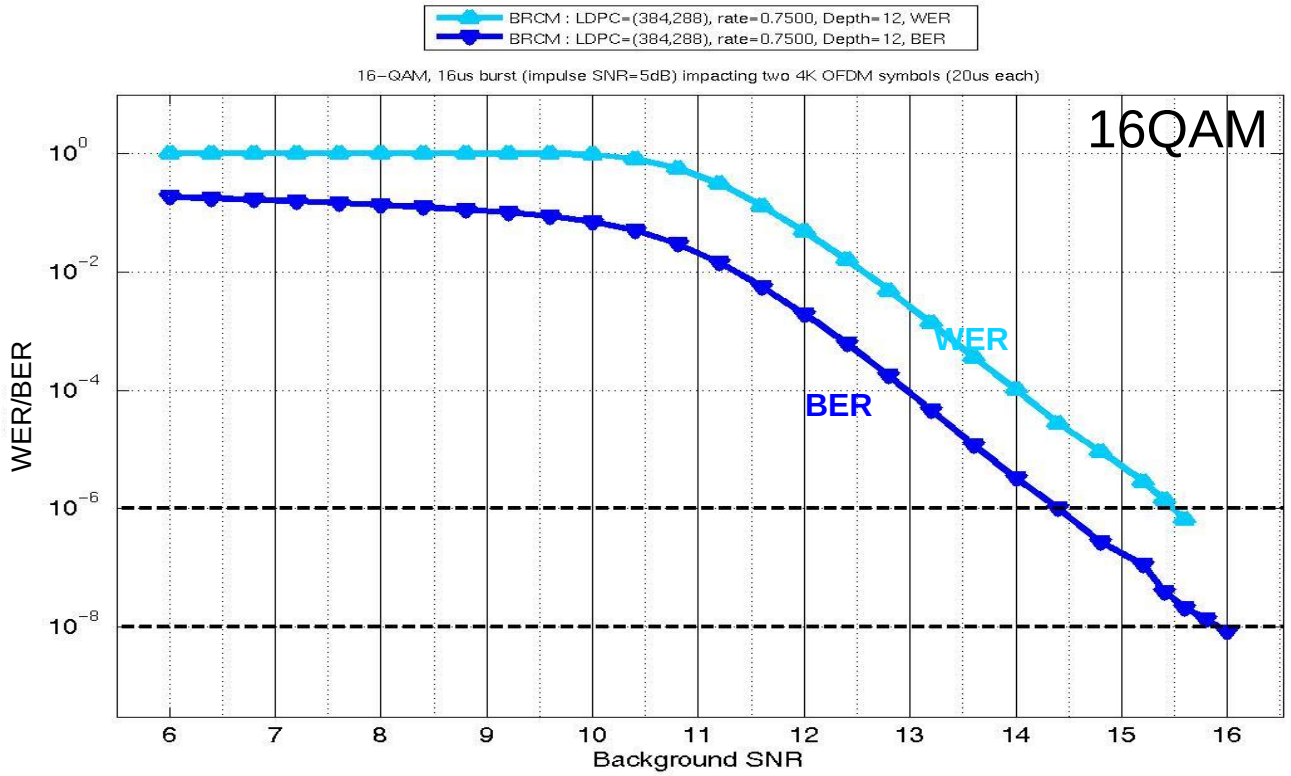
	WER=1e-6	BER=1e-8
74% BCH	14.8 dB	15 dB
75% LDPC	13.8dB	14dB
Difference	1dB	1dB

75% RS (64,48) (on 64 QAM)



	WER=1e-6	BER=1e-8
75% RS	21.5 dB	21.6 dB
75% LDPC	19.4dB	19.6dB
Difference	2.1dB	2dB

PERFORMANCE ON IMPULSE/BURST NOISE



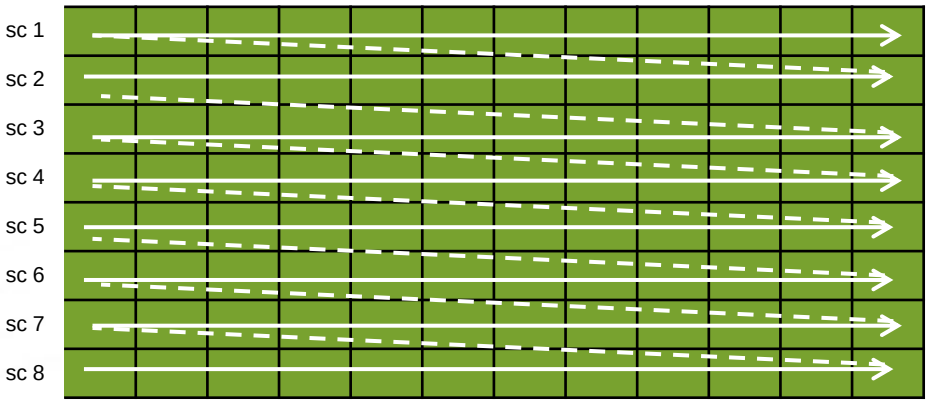
Max. 15 iterations

WER=1e-6	BER=1e-8
15.5dB	15.8dB

Burst: 16 µs duration and 5 dB SNR
Burst noise impacts two symbols

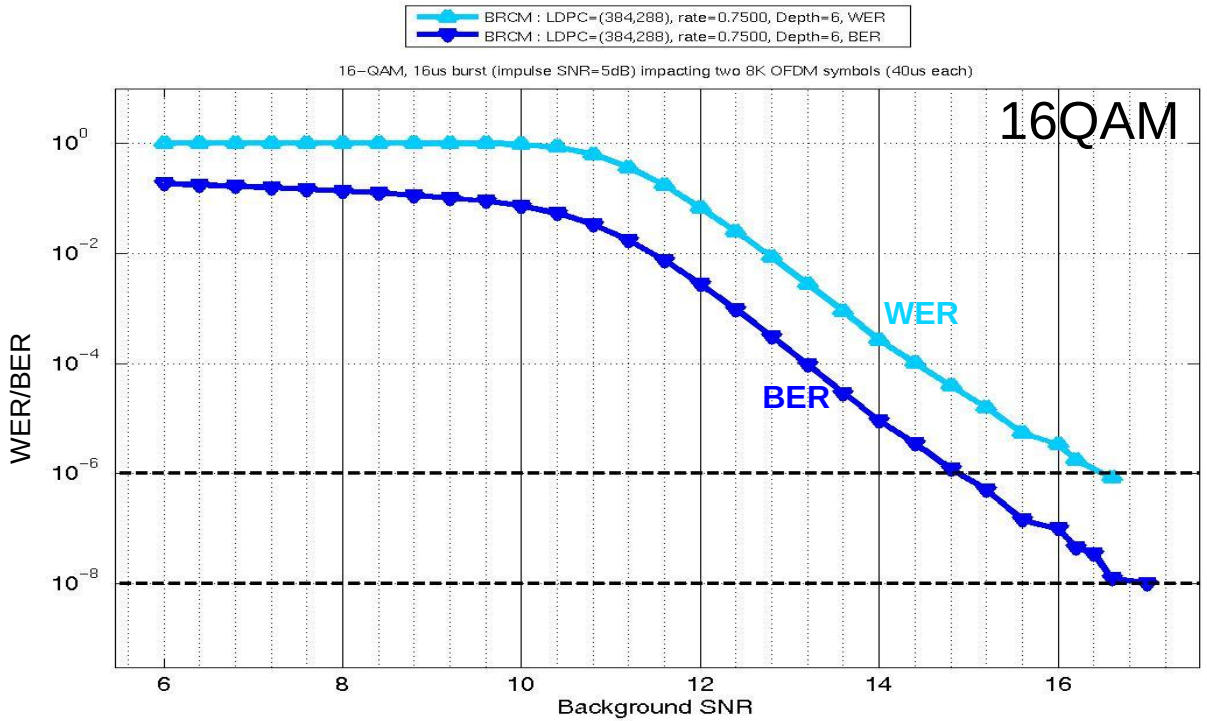
20 µs symbol with 2.5 µs CP
Latency: 270 µs (12 symbols)

8 4-bit sub-carriers per OFDM symbol
12 OFDM symbols
8*4*12=384 bits= one codeword size



Codeword bits distribution

PERFORMANCE ON IMPULSE/BURST NOISE



Max. 15 iterations

WER=1e-6	BER=1e-8
16.2 dB	16.2 dB

Burst: 16 µs duration and 5 dB SNR
Burst noise impacts two symbols

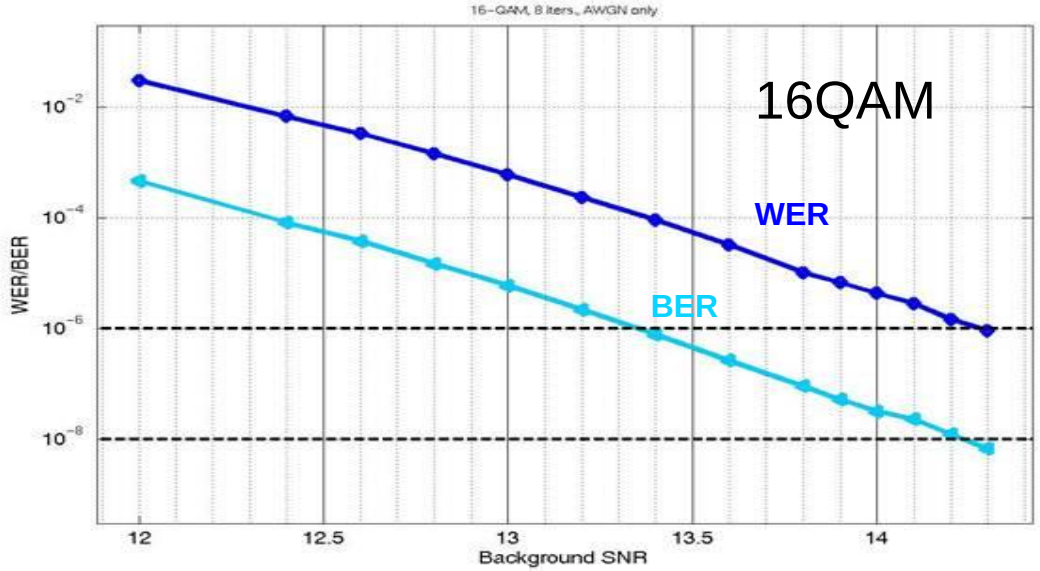
40 µs symbol with 2.5 µs CP
Latency: 255 µs (6 symbols)

16 4-bit sub-carriers per OFDM symbol
6 OFDM symbols
16*4*6=384 bits= one codeword size

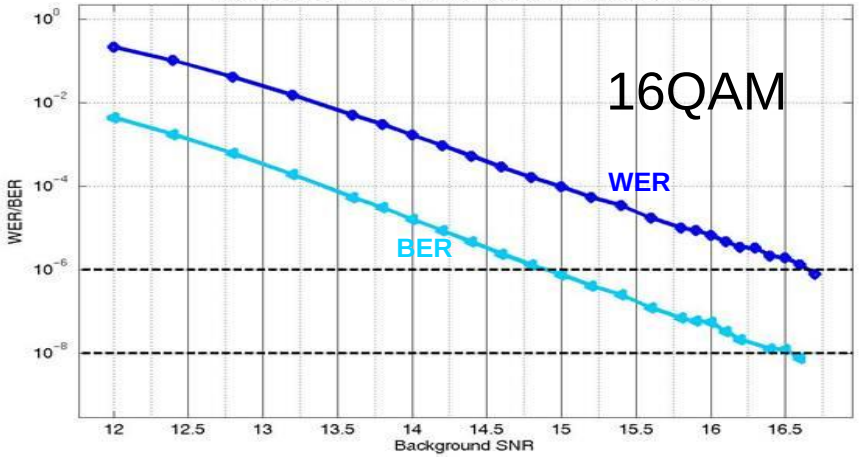
REDUCING NUMBER OF ITERATIONS

- **The figures below show the performance with maximum 8 iterations**

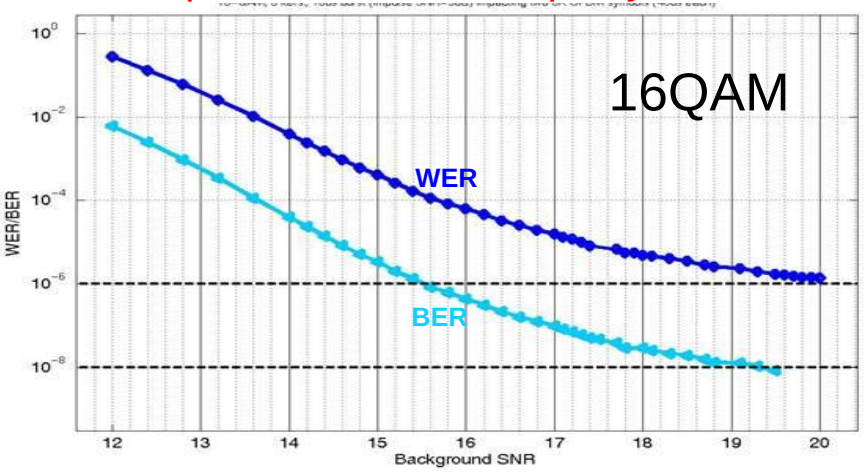
AWGN channel



16 µs burst on two 20 µs symbols



16 µs burst on two 40 µs symbols



- **BER< 1e-8 SNR = 14.5 dB with AWGN**
  - 0.5 dB degradation compared to 15 iterations
- **BER< 1e-8 SNR = 16.5 dB with burst noise on 20 µs symbol**
  - 0.5 dB degradation compared to 15 iterations
- **BER< 1e-8 SNR = 19.5 dB with burst noise on 40 µs symbol**
  - 3.3 dB degradation compared to 15 iterations

CONCLUSIONS

- **An (384,288) binary punctured LDPC code for PLC is proposed**
- **Code rate: 75%**
- **Code latency: 270/255 µs**
  - for 20/40 µs symbols with 2.5 µs cyclic prefix
- **SNR = 14 dB and 16 dB with AWGN and AWGN + burst noise**
  - 16 µs duration and 5 dB SNR burst noise over two adjacent symbols
- **Negligible complexity three orders of magnitude lower compared to the downstream data decoder**
  - 1 Mbps compared to 1+ Gbps throughput

PROPOSED MOTION

- **Do you support selecting the (384, 288) LDPC code for PLC FEC?**

Thank You