Data Rate Adaptation

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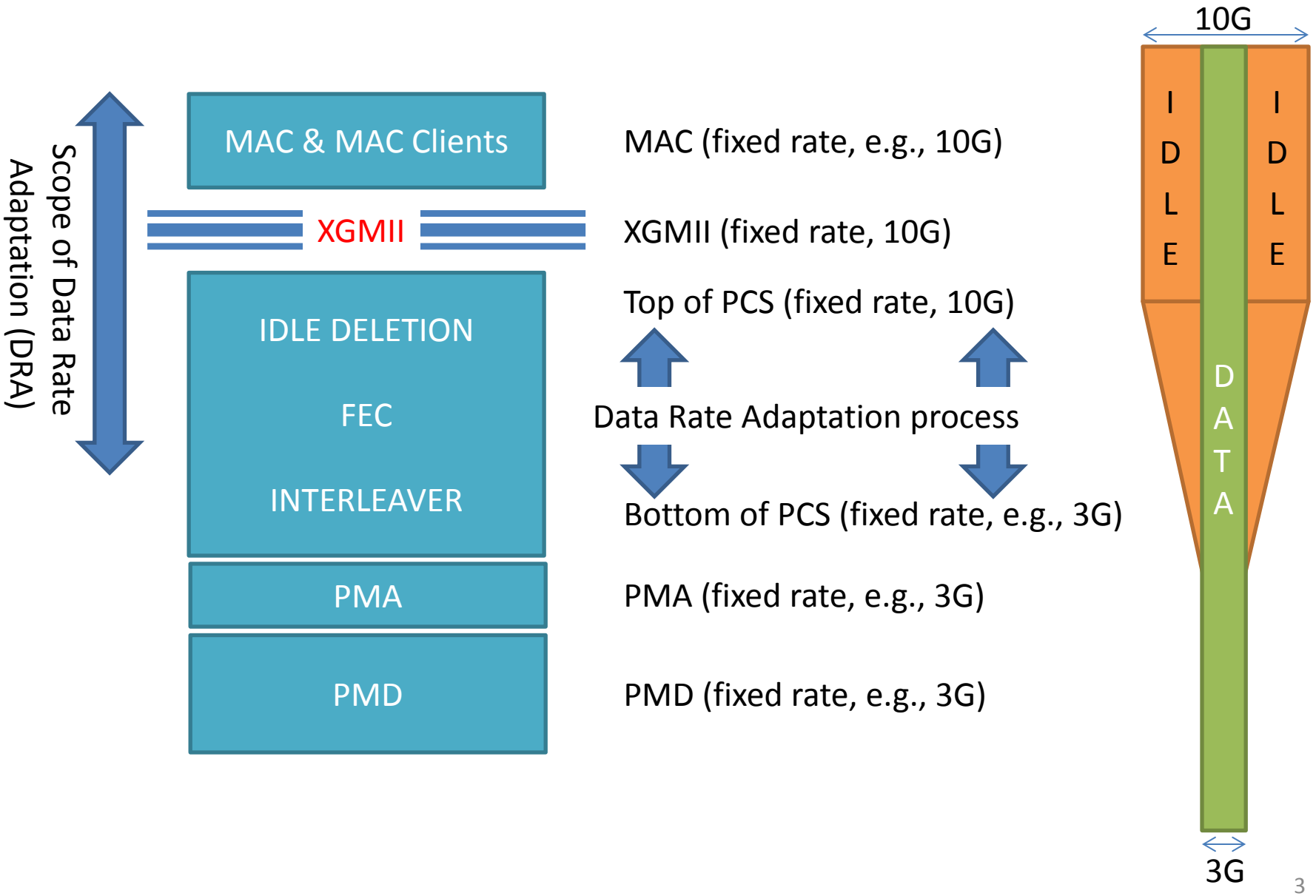
Summary

- Data Rate Adaptation (DRA) function decouples fixed MAC/XGMII rate from PHY rate at PMD
  - DRA has nothing to do with DBA, bandwidth allocation in EPoC / EPON, etc.
- There are various ways to implement DRA in Ethernet; we focus on mechanism used in 10G-EPON P2MP architecture
- This slide deck explains the need for DRA, its functional operation and highlights interaction between various elements in the 802.3 stack
- This discussion in then mapped into EPoC stack and individual functional layers

The Need for DRA (in picture)



The Need for DRA (in text)

- MAC operates at a fixed data rate (e.g., 10G). XGMII operates at a fixed data rate (10G)
- PMD operates at an effective data rate lower than MAC/XGMII data rate (e.g., 3G)
- Somewhere in PCS, data rate must be adapted between fixed MAC rate (10G) and effective PMD data rate (3G)
- Adaptation process may rely on removal of excess IDLE characters inserted by MAC between frames (see 10G-EPON example)

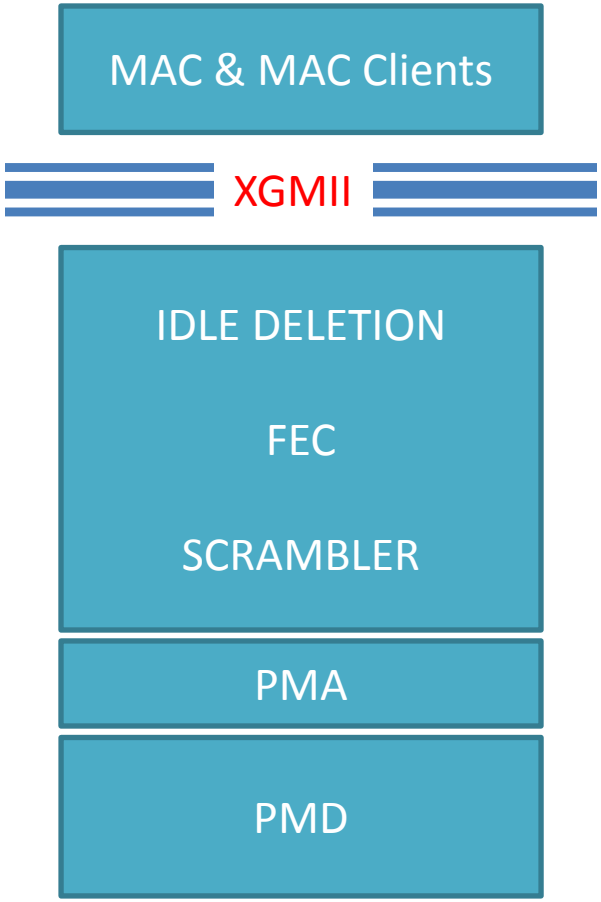
DRA in 10G-EPON - background

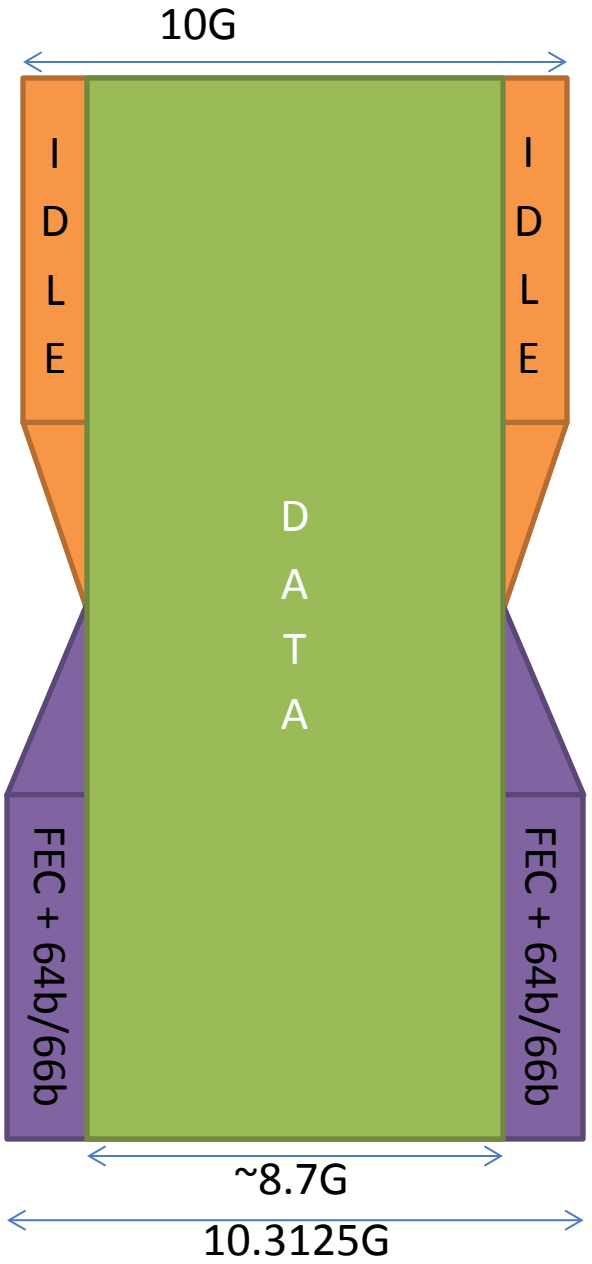
- At first glance, it seems much simpler to use 10G MAC rate and increase PMD rate to ~11.25G to transport FEC parity – RS(255,223) assumed
- However, concerns about technical feasibility of 10GE optics at ~11.25G were raised in 10G-EPON TF -> the group decided NOT to use super-rate PMD
- MAC rate had to remain fixed (10G) and under-rating effective data stream was the only way available to use FEC and reuse existing 10GE designs
- Data Rate Adaptation mechanism was developed to address XGMII signaling restrictions, avoid the use of real-time signaling and provide robust mechanism to lower effective data rate observed by MAC

How DRA works in 10G-EPON?

- In 10G-EPON, MAC rate and PMD rates were fixed at 10G and 10.3125G, respectively (64b/66b line encoding)
- To accommodate FEC parity in PCS, MPMC decreases the effective data rate to ~8.7G (~12.9% FEC overhead)
- MAC inserts extra IDLE characters between frames to keep data rate constant (10G) – IDLE Insertion process at TX side
- 10G data rate is maintained across XGMII and reaches top of PCS at the TX side
- Within PCS, IDLE Deletion process removes extra IDLE characters, leaving only IPGs and IDLE characters generated by MAC in absence of data
- Resulting ~8.7G data stream is 64b/66b encoded and then fed to FEC. FEC parity is then inserted, bringing data rate to 10.3125G which is fed into PMA / PMD.

DRA in 10G-EPON (in picture)



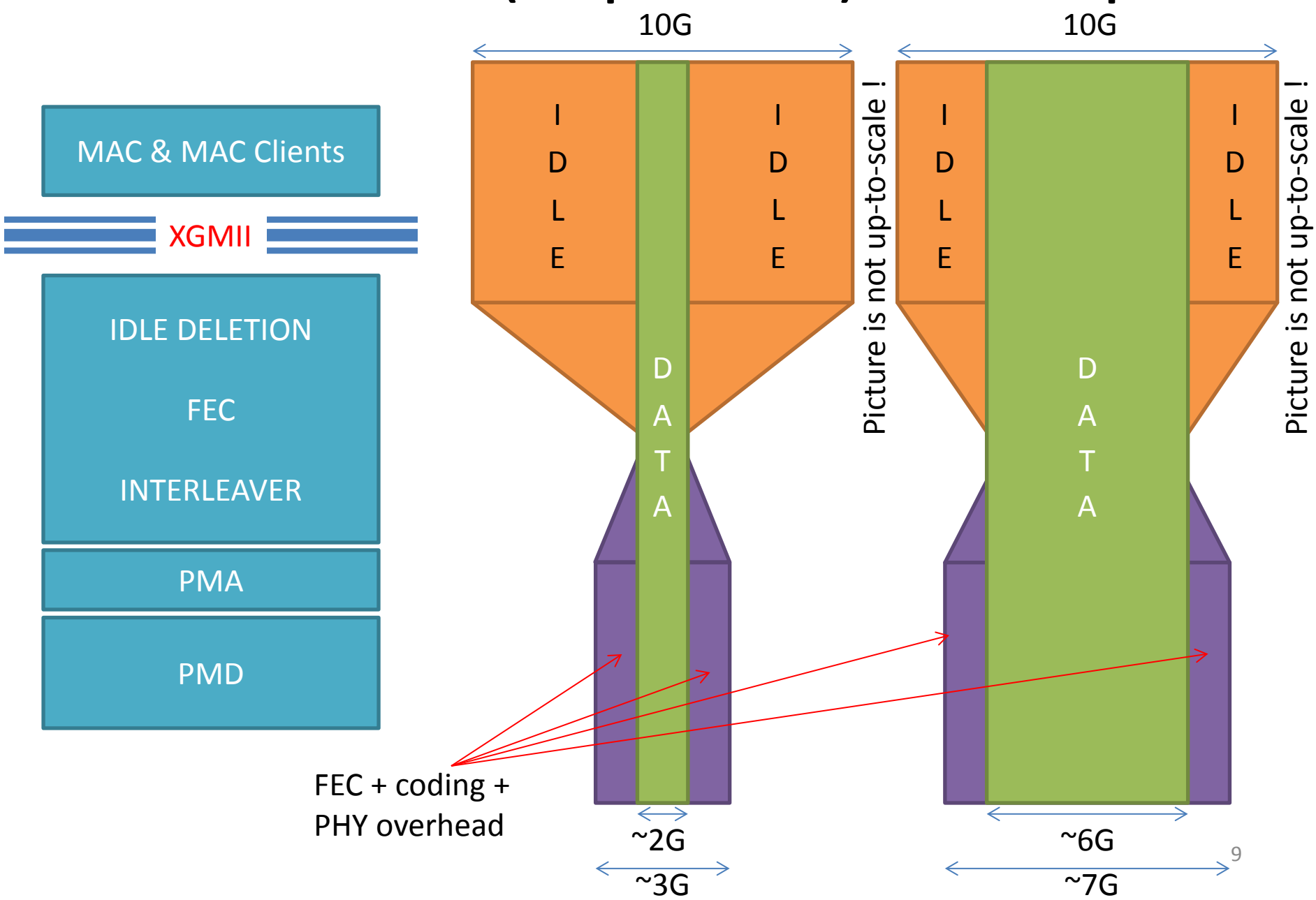


Picture is not up-to-scale !

Why DRA is needed in EPoC?

- There are three main reasons:
  - MAC / XGMII rate remains fixed at 10G (we want to support data rates up to 10G on coax)
  - We need to accommodate FEC parity interleaved in the data stream without pushing data rate above 10G – like in 10G-EPON today
  - We need to accommodate a number of possible PMD data rates (either fixed or dynamic) that are lower than 10G MAC rate.
- Effectively, in EPoC data rate at PMD is smaller (or much smaller) than MAC / XGMII rate

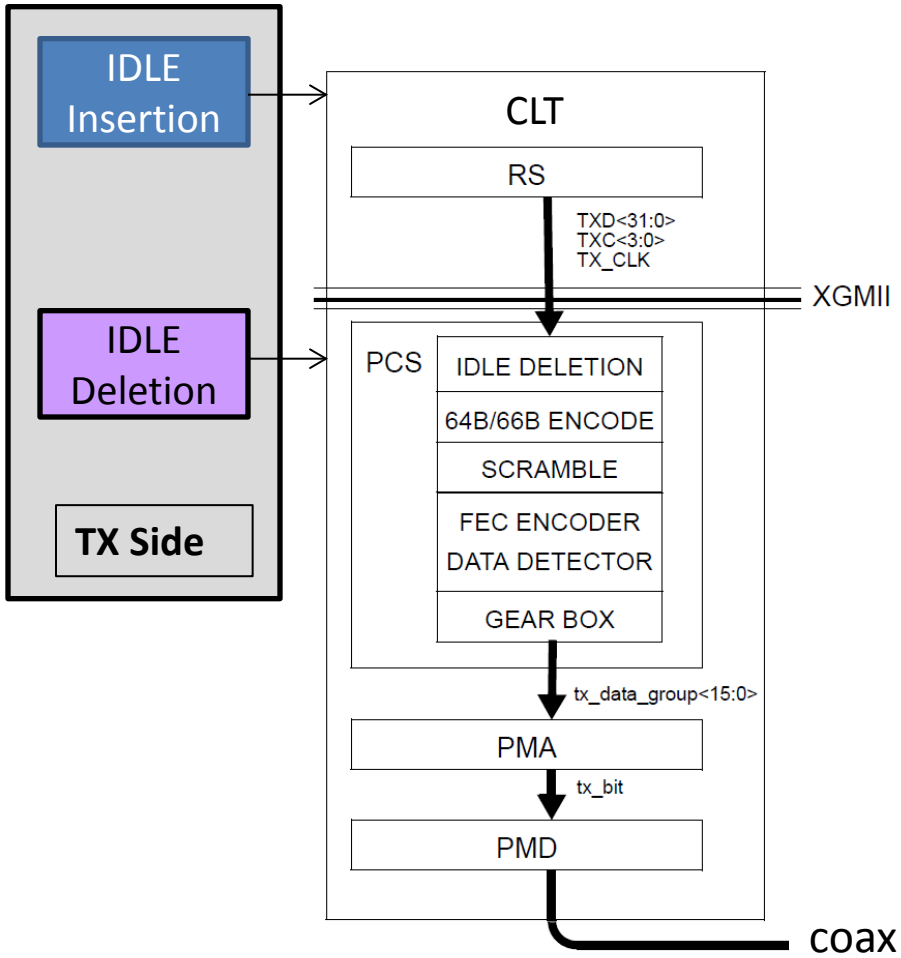
DRA in EPoC (in picture) - examples



DRA in EPoC

- In EPoC, given the range of possible (fixed / dynamic) PMD rates, DRA needs to:
  1. Accommodate insertion of FEC parity (like in 10G-EPON);
  2. Accommodate for any PMD overhead (CP, etc.) and PMD de-rating (PMD does not operate at full 10G due to limited availability of spectrum);
  3. Accommodate TDD switching (note: we do not focus on TDD switching in these slides)
- The second and third bullets above are new functions for DRA, not seen in 10G-EPON
  - Bullet 3) would be addressed by the TDD sub-taskforce
- Next slides outline DRA in EPoC and list challenge items
  - Assume R_{eff} is the effective data rate at PHY (actual data), R_{FEC} is the FEC overhead due to insertion of parity
  - R_{MAC} and R_{XGMII} are both set to 10G and referred to as R_{MX}

Downstream in CLT (TX side)



IDLE Insertion process

- Packets are properly inserted (by the Multipoint Transmission Control) and filled with IDLEs by the MAC layer. MPMC keeps data rate at R_{eff}.
- In this way, a fixed rate of 10G is guaranteed by MAC for the XGMII interface (R_{MX}). Extra IDLEs inserted by MAC create space for FEC parity bits and all PHY overhead in the data stream

IDLE Deletion process

- Extra IDLEs are then removed by the IDLE Deletion process inside the PCS (upper PHY stack) to match with PMD rate and include FEC parity bits.
- At the output of IDLE Deletion process, data rate is equal to R_{eff}.

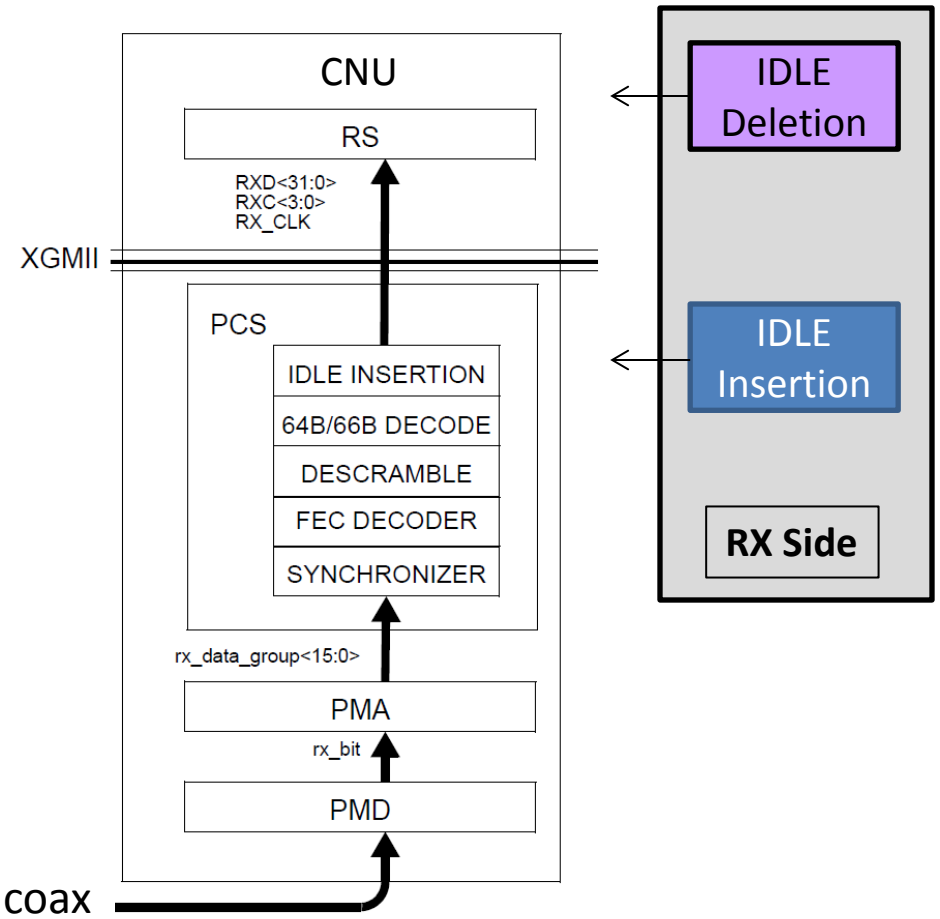
Downstream in CNU (RX side)

IDLE Deletion process

- Extra IDLEs are then removed above XGMII interface and complete Ethernet frames are then passed to MAC Clients.
- Data rate above MAC is equal to R_{eff}.

IDLE Insertion process:

- FEC encoded packets arrive at PCS at the PMD rate and are fed into the FEC decoder. After removal of FEC parity, data rate becomes R_{eff}.
- Gaps between frames are filled with IDLEs to achieve data rate of R_{MX} and match XGMII data rate.



Upstream direction

- In the upstream direction
  - CNU transmits and behaves like CLT in downstream, adding only the burst mode transmission capabilities
  - CLT receives and behaves like CNU in downstream direction, adding only the burst mode reception capability

- Conclusion: the same functionalities illustrated on three previous slides is also applicable to the upstream direction.

Conclusion and Recommendation

- In this presentation Data Rate Adaptation (DRA) function and the need for it in EPoC are illustrated
  - DRA in 10G-EPON is needed to account for FEC parity and it is based on IDLE insertion/deletion across XGMII interface
  - EPoC and 10G-EPON share the FEC-parity-related need for DRA. However, EPoC will also need to use DRA to adapt between R_{MX} and R_{eff} (PMD de-rating) and account for TDD switching (not covered in the slides)
  - EPoC DRA can be based on the same principles and on the same mechanisms used in 10G-EPON
  - DRA is applicable to both DS and US directions in EPoC
- It is therefore recommended to include DRA function in EPoC spec, reusing mechanisms defined in 10G-EPON