

EPOC DATA DETECTOR

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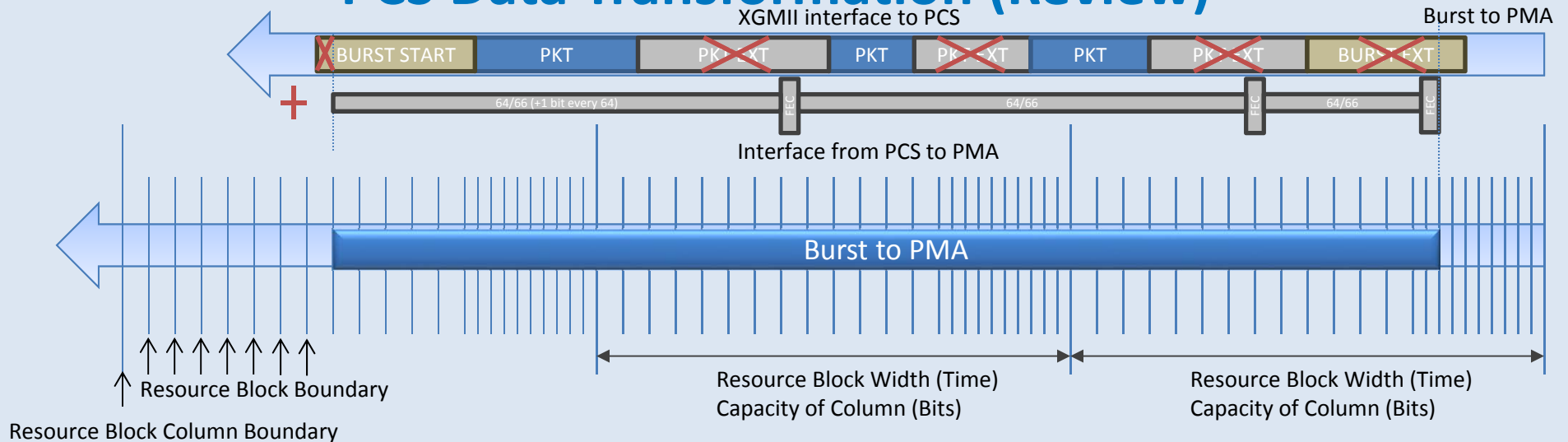
Overview

- This presentation is a continuation of the EPoC Upstream Presentation (motioned as starting point) from Indian Wells.
 - The PCS/PMA interface definition is assumed.
- The Downstream Rate Control functions for the Idle Deletion and Gearbox are also assumed.
- This presentation attempts to define the data detector function for the upstream PCS.

Disclaimers

- **This presentation shows a solution for any of 3 possible parity endings.**
 - Medium-only, Long-Short, or Long-Medium-Short could be used.
 - The same block diagram and state machine can be used.
 - This presentation doesn't require a specific method.
- **This presentation assumes no K/2**
 - K/2 requires an addition buffer before or after the data detector that significantly complicates the fixed delay requirement.
- **This presentation assumes a single CRC-40 and all parity at the end of burst.**
 - Multiple Parity/CRC-40 requires an addition buffer before or after the data detector that significantly complicates the fixed delay requirement.
 - Addition states are also needed in state machine.
- **This presentation shows a bit wide description since decisions are made on a bit boundary.**
 - This method provides the cleanest and clearest description of the expected behavior.
 - Obviously, a real implementation would make decisions on blocks of bits.

PCS Data Transformation (Review)



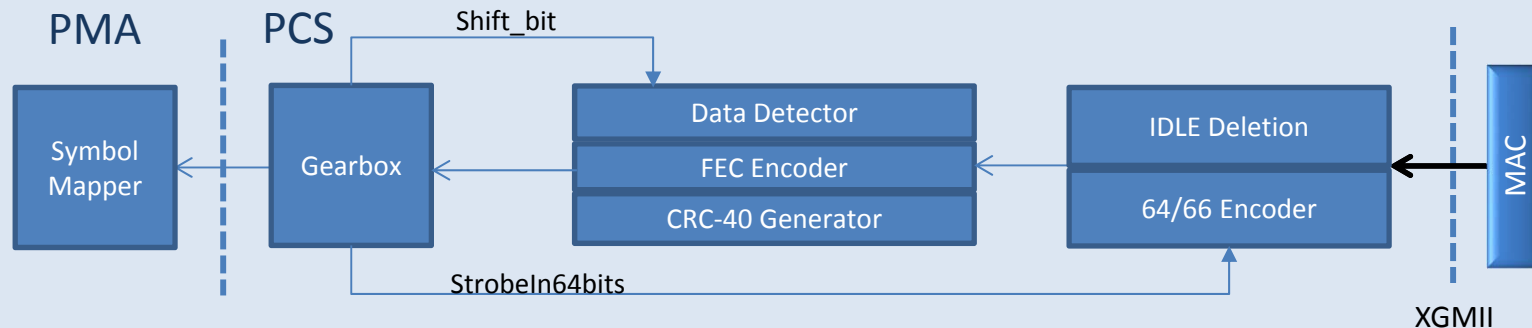
- **PCS to PMA**

- The PCS provides a constant data rate stream of data to the PMA (for a configuration)
- The PCS identifies the bits in a burst and out side of burst (a laser enable equivalent)
- The PCS/PMA are aware of the Resource Boundaries and Resource Block Boundaries in the data stream.
- The data rate is determined by the Resource Block Column Capacity (total bits) over the width of a Resource Block (time).

- **PCS Data Transformation**

- Bits from a burst start are discarded until a Resource Block Boundary is reached.
- Bits for Start Marker are discarded.
- 64/66 encoding and FEC encoding starts on data stream.
- IDLE deletion occurs on the data stream.
- At the end of burst, bits from the burst extension are taken until a Resource block boundary is reached after FEC has been inserted.

Upstream & Rate Control Review



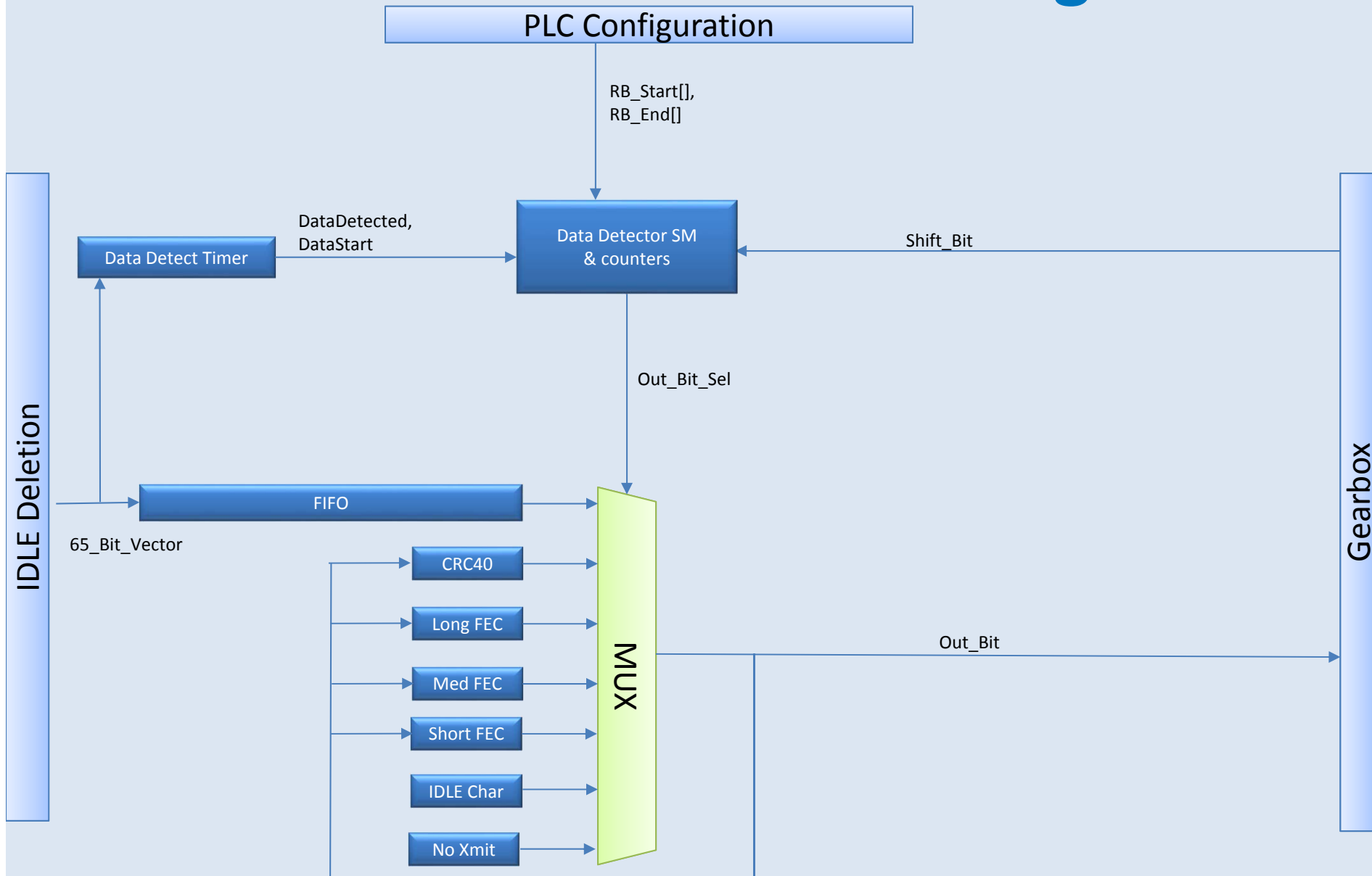
- **IDLE Deletion**

- XGMII will stream packets at 10Gbps.
- IDLEs will be inserted in the MAC between packets to guarantee MAC rate is less than PHY rate.
- The IDLE Deletion block will encode 64 bits into 65 bits and remove excess IDLE characters based on the Gearbox rate control reference.

- **Gearbox**

- The Gearbox will control the data rate through the PCS by a reference signal from the IDLE Deletion.
- The Gearbox will shift out bits for the PMA .

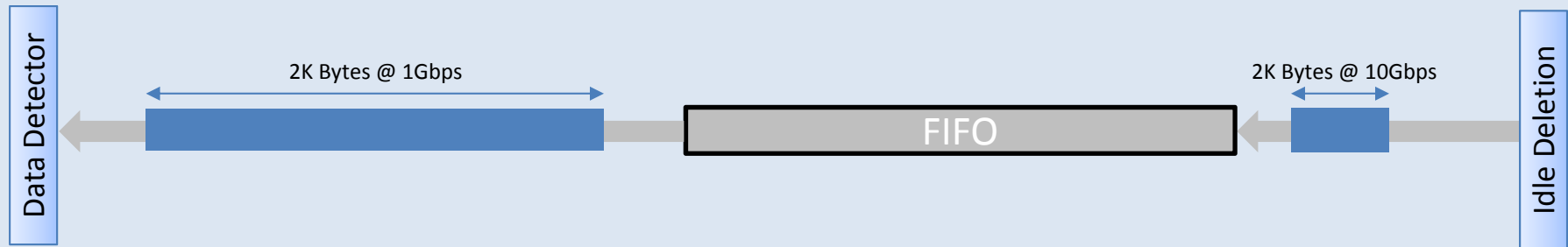
Data Detector Block Diagram



Data Detect Timer

- The Data Detect Timer generates the DataDetected and DataStart signals for the Data Detector SM.
- DataDetected
 - DataDetected is asserted when a data 65-bit vector is passed to or stored in the FIFO.
 - After DataDetected, the SM will begin to put out idle bits at the Resource Block Boundary until the DataStart is asserted and data is released from the FIFO.
 - DataDetected is deasserted a configured time after the last data has been removed from the FIFO. The configured time should be greater than the IPG at the sustained data rate.
- DataStart
 - DataStart is asserted a fixed time delay [10.24MHz clocks] from DataDetected.
 - This delay must be configured to be longer than largest RB capacity divided by the data rate. (A couple of hundred bits, a few 65 bit symbols).

FIFO



- The FIFO provides the rate adaption between the XGMII and the PMA.
- Since the PMA rate is matched by deleting idles between packets, this FIFO will always be empty at the start of burst. (The SM holds it in reset)
- It will be near empty at the start of a packet and near full at the end of a long packet.
- It provides buffer to handle delay for start of burst and insertion of FEC/CRC40.
- FIFO size can be safely sized at 2K Bytes (maximum packet size).

Counters

- **All counters are incremented by Shift_Bit from Gearbox**
 - Shift_Bit exactly aligns with the PMA input data rate.
- **65BitCnt**
 - Counts to 65 to identify 64/66 Vector Boundary
- **ParityBitCnt**
 - Counts to the size of the FEC parity size.
- **CrcBitCnt**
 - Counts to 40 bits to identify the end of the CRC40 checksum.
- **BlkBitCnt**
 - Counts the bits in a FEC Block payload.
- **ColBitCnt**
 - Counts the bits in a Resource Block Column.

RB_Start and RB_End Arrays

- Resource Block Start and End Arrays contain the valid start and end bit positions for any burst.
- RB_Start and RB_End are generated in the PHY based on the configuration of the Resource Blocks (bit capacity).
- The RB_Start/RB_End size matches the total capacity of a RB Column. (1 bit for every bit in the array).
- RB_Start
 - Indexed by the ColBitCnt to determine when to switch from “NO XMIT” to “IDLE”s at the start of a burst. (“0” continue NOXMIT, “1” start IDLEs)
- RB_End
 - Indexed by the ColBitCnt plus the CRC40 and amount of parity to determine if IDLE insertion can stop at the end of the burst.
 - The amount of parity is determined by the ParityLen() function on the BlkBitCnt.

NOTE: RB_Start and RB_End must be generated for both Odd and Even configuration to support hitless switchover.

TAIL Functions

- **ParityLen(BlkBitCnt)**
 - This function returns the length of the parity (in bits) at the end of the burst. ParityLen is based on the number of bits in the block in the tail of the burst.
 - Medium Only
 - Any size of payload (900 bits of parity)
 - Long-Short
 - 1-800 bits of payload (280 bits of parity); 801-1640 (560); 1641-2480 (840); 2481-3320 (1120); 3321-4160 (1400); 4161-5000 (1680); 5001-14300 (1800)
 - Long-Medium-Short
 - See Table on next slide.
- **ParityType(BlkBitCnt, ParityBitCnt)**
 - This function selects the parity encoder to unload based on the number of bits in the tail block (BlkBitCnt) and the parity bit number to be unloaded (ParityBitCnt).
 - Medium Only
 - Always returns Medium.
 - Long-Short
 - BlkBitCnt < 5001: Short. BlkBitCnt > 5000: Long.
 - Long-Medium-Short
 - See Table on next slide

LMS Parity Calculation

- Long-Medium-Short has multiple parity output options based on the amount of data at the end of burst.
- The table defines the range of bits for calculation of the FEC parity.

ParityType Output	BlkBitCnt + CrcBitCnt (Min)	BlkBitCnt + CrcBitCnt (Max)
SHORT1	1	840
SHORT2	841	1680
SHORT3	1681	2480
MEDIUM	1	5040
SHORT4	5040	5880
SHORT5	5881	6720
SHORT6	5001	5840
LONG	1	14340

LMS ParityLen()/ParityType()

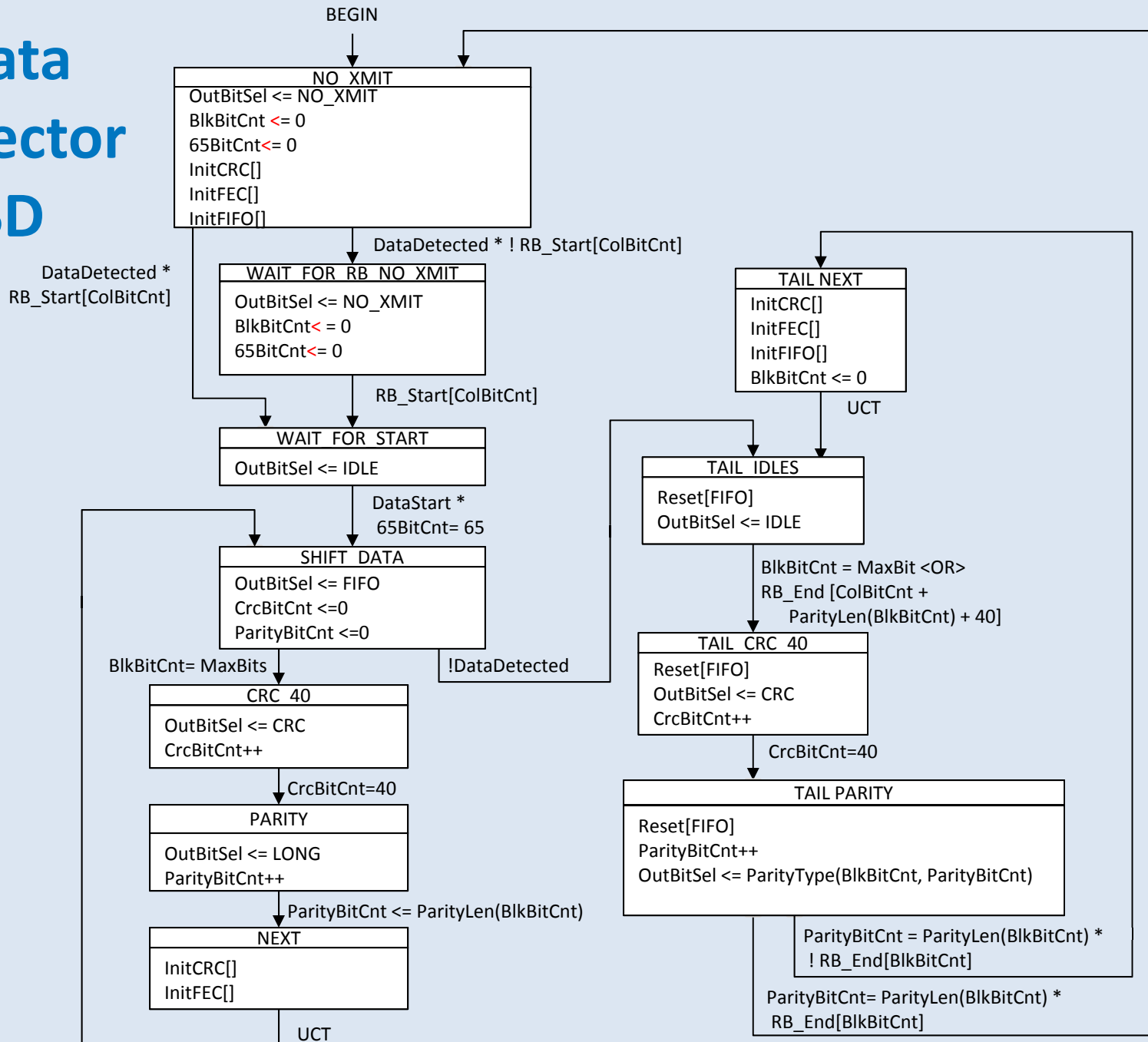
- This table defines the functions for calculating the length of parity and the parity to output.

BlkBitCnt (Min)	BlkBitCnt (Max)	ParityLen output	ParityBitCnt (Min)	ParityBitCnt (Min)	ParityType output [drives OutMuxSel]
1	800	280	1	280	SHORT1
801	1640	560	1	280	SHORT1
			281	560	SHORT2
1641	2480	840	1	280	SHORT1
			281	560	SHORT2
			561	840	SHORT3
2481	5000	900	1	900	MEDIUM
5001	5840	1180	1	900	MEDIUM
			901	1180	SHORT4
5841	6680	1460	1	900	MEDIUM
			901	1180	SHORT4
			1181	1460	SHORT5
6681	7520	1740	1	900	MEDIUM
			901	1180	SHORT4
			1181	1460	SHORT5
			1461	1740	SHORT6
7521	14300	1800	1	1800	LONG

SM Overview

- **NO_XMIT**
 - The State Machine sends “no xmit” bits to the PMA
 - After “DataDetected” is asserted, the RB_Start array is checked for a starting bit position.
- **WAIT_FOR_START**
 - FEC and CRC40 calculation start on the Data.
 - IDLE vectors are transmitted until the DataStart (fixed delay from data detected) is asserted.
- **SHIFT_DATA**
 - Data bits from the FIFO are shifted out to the PMA.
 - CRC-40 and Parity are inserted for the Long code word size when the block size limit is reached.
 - When DataDetected is deasserted, the FIFO is cleared for the end of burst.
- **TAIL_IDLE**
 - Idles are inserted until the RB_End array for the current position plus the CRC-40 & Parity Bits indicates a valid ending bit.
 - CRC40 and FEC Parity are added to the end of the burst.
 - SM returns to NO_XMIT

Data Detector SD



Configuration Switchover

- **Upstream Configuration Switchovers will happen between or during bursts.**
 - Bit Loading changes should be hitless. Data Rate could go up or down.
 - Changes to the RB width (time) by changing the number of symbols or CP will require re-registration.
- **Start of Burst Timing**
 - A Laser ON time that is a fixed number of Bytes will not work for EPoC.
 - A fixed number of bytes will be a different delay for different data rates.
 - DataStart is a fixed time delay from DataDetected to eliminate jitter due to data rate changes.
- **RB_Start & RB_End Arrays**
 - The RB_Start and RB_End arrays must be re-generated for new bit-loading configurations.
 - RB_End must account for blocks that span configuration changes.
- **Gearbox Control**
 - Since the Gearbox controls the switchover, a data rate change will be communicated to the Data Detector by adjusting the Shift_Bit period.

Conclusion

- This presentation provides a description for the data detector that could be converted into text for the standard.
- The design supports hitless switchover and aligns with the Downstream Rate Control and Upstream starting point architectures.
- The Data Detector is complicated enough without functionality that requires a delay buffer (K/2 and Scattered Parity/CRC40).
- More work is needed to define the Grant Length and Grant Slot Size equations for the state machine.