Upstream FEC Structure Discussion

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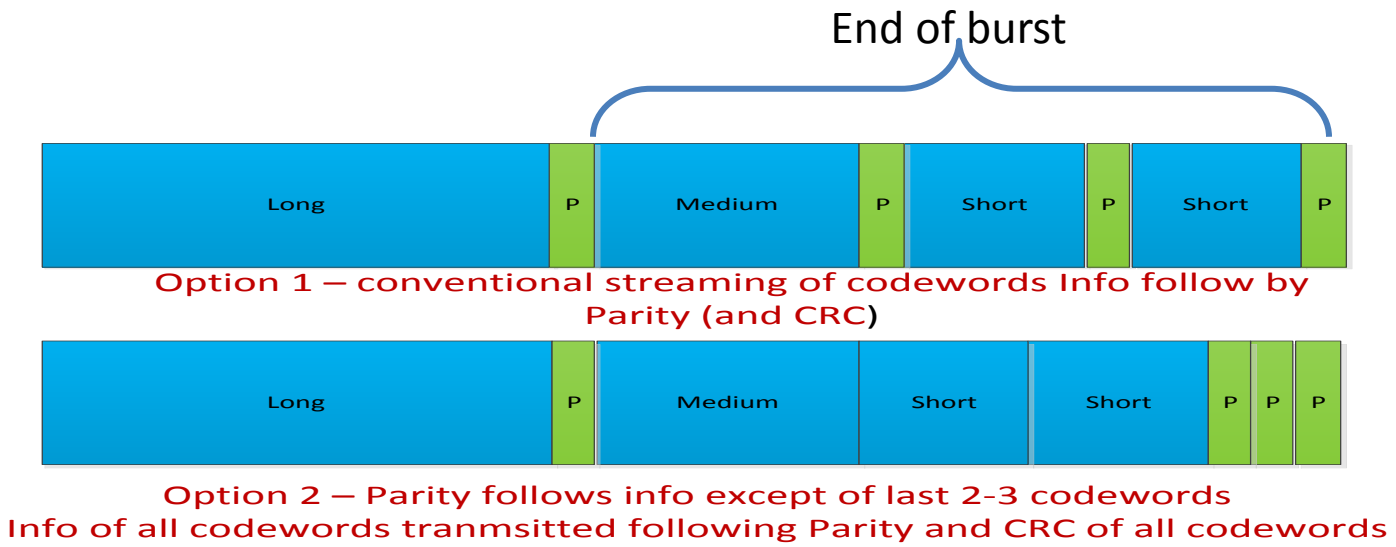
Two options for Data Transmission



- Option 1 – Conventional streaming of CWs info followed by parity, CW by CW
- Option 2 – Same as #1, info followed by parity except for last 2-3 CWs , all info is transmitted first, followed by parity of all three CWs

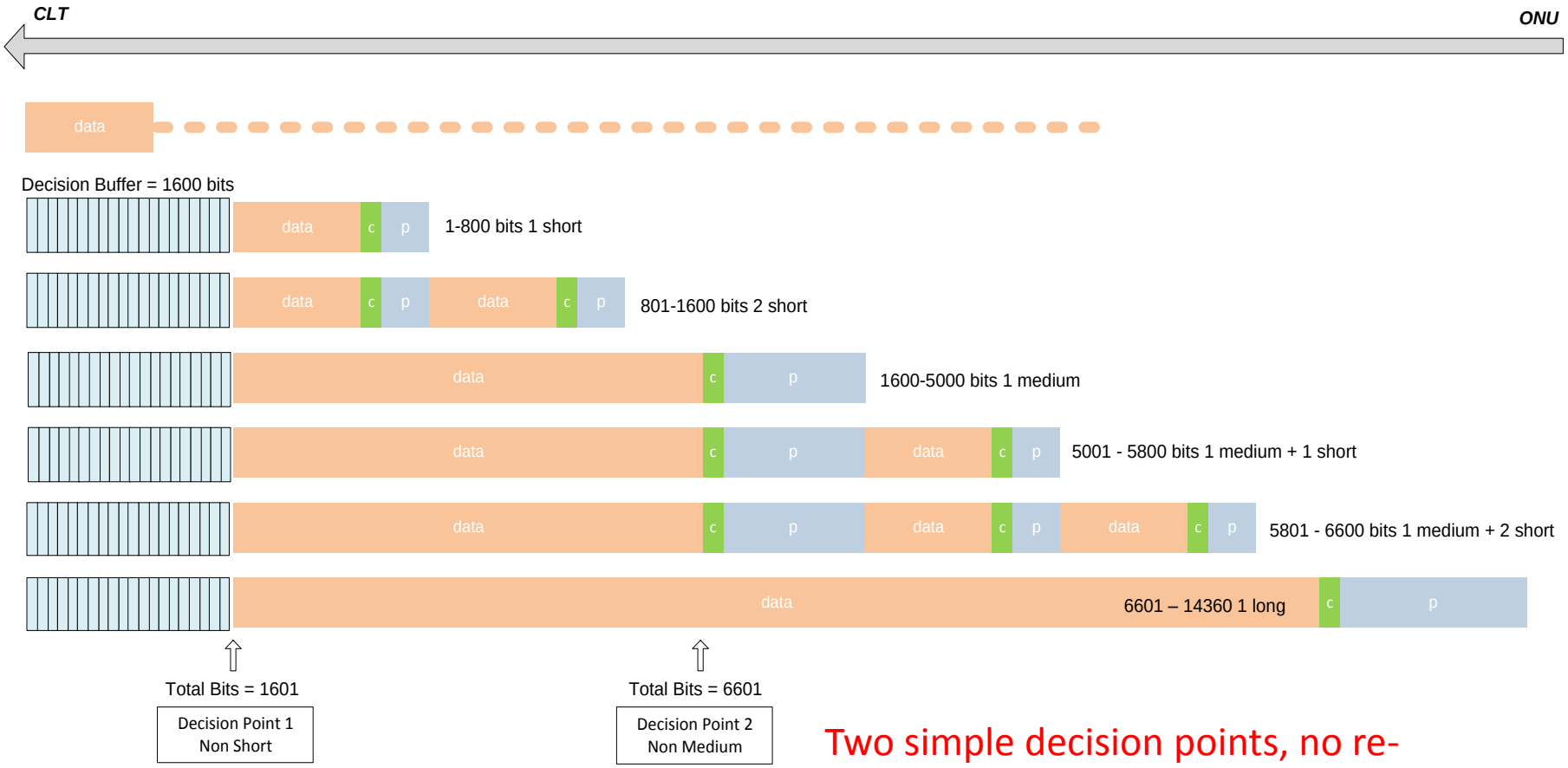
Discussion on Comparison

- Claimed advantages by proponents of Option #2
  - More efficient (a single CRC vs. three CRCs)
  - Lower latency, buffer avoided at the transmitter
  - Lower complexity at the receiver
- We found:
  - Most of the claims are not correct
  - Only advantage is lower latency but by a small/ insignificant amount
  - But, with option #2 implementation is more complex
  - No sufficient motivation for changing what has been already been adopted

Advantages of Option #2 are Insignificant

- Buffer saving at the transmitter
  - 1600 bits (200 Bytes!) only are required
  - Option 2 requires a buffer larger than buffer required for option #1
  - Will be shown later
- Latency reduction
  - with lower rate 1600/250M = 6.4 uSec
  - Latency with higher rate 1600/1G = 1.6 uSec
  - Latency reduction is not significant compared to inherent latency in the upstream, which is hundreds of uSec (1% or less)
- CRC saving
  - Saving 40-80 bits of CRC is insignificant compared to long packet sizes (~ 14000 bits)
  - Will anyhow be lost due to RB alignment in the PMA
- **But it adds complexity to both transmitter and receiver**
  - Additional re-ordering buffers and management is required

Option 1 - FEC Transmitter Delay is 1600 Bits



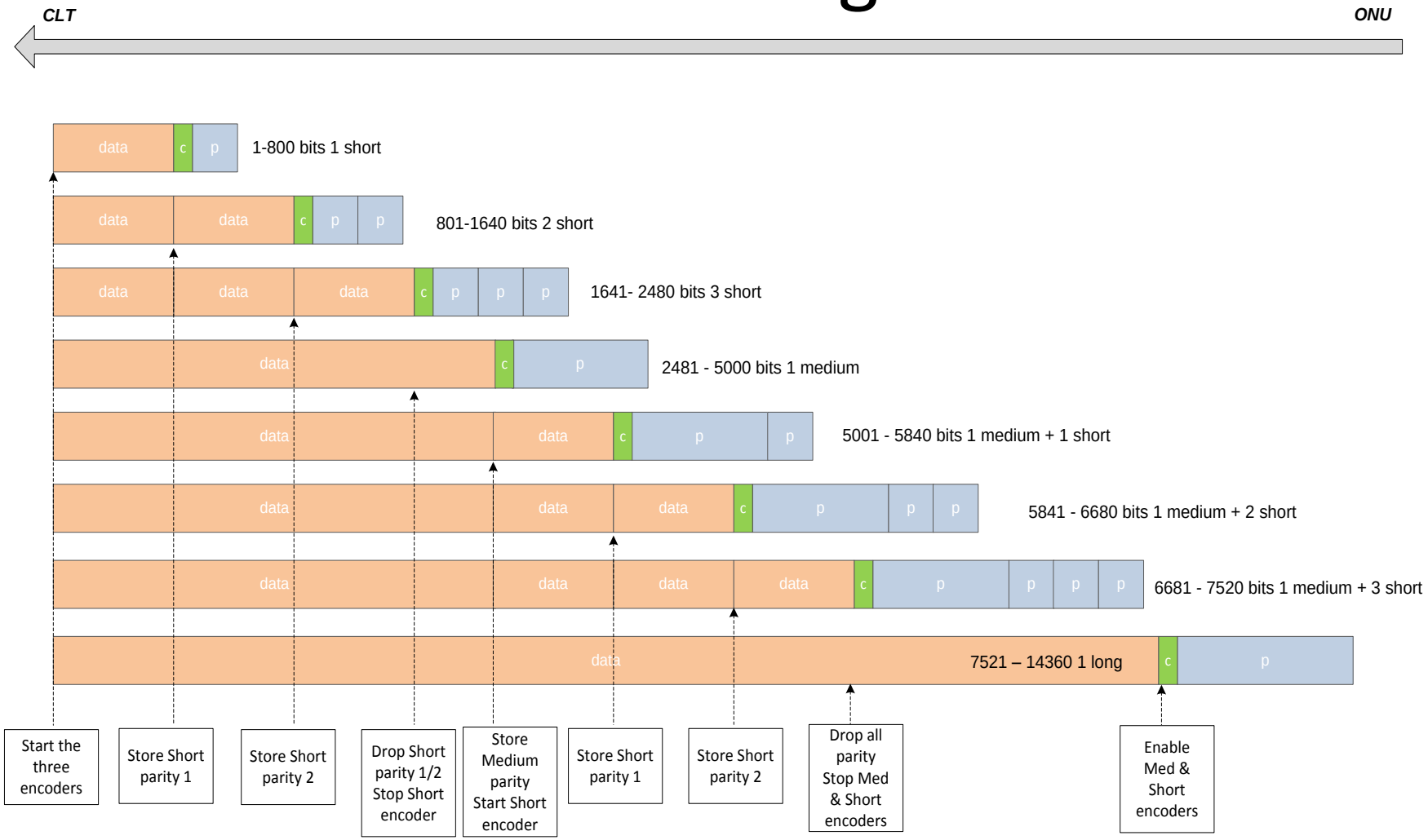
Two simple decision points, no re-ordering is required

A single 1600 bits FIFO is required

Transmitter FEC Decision Buffer

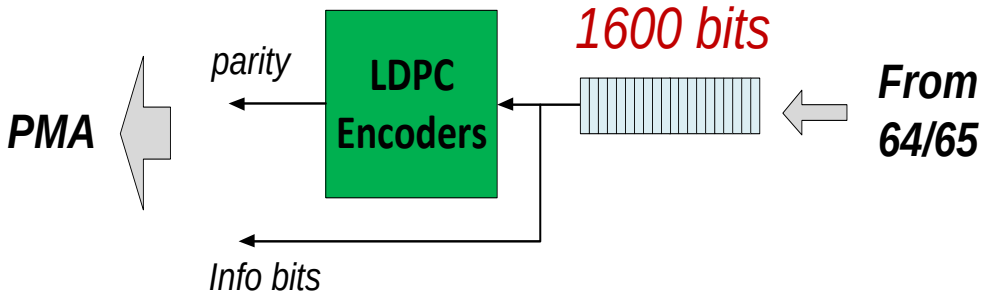
- A FIFO allows the FEC encoder to know where to put the CRC-40 and parity
  - A single and simple decision point
- The size of the Decision Buffer is 1600 bits for any upstream rate
- Decision Buffer add latency of 1.6 – 6.4 us
  - 1,600 bits @ 1Gbps = 1.6us
  - 1,600 bits @ 250Mbps = 6.4us
- Single CRC-40 generator

Option 2 – Complex Flow and Decision Making

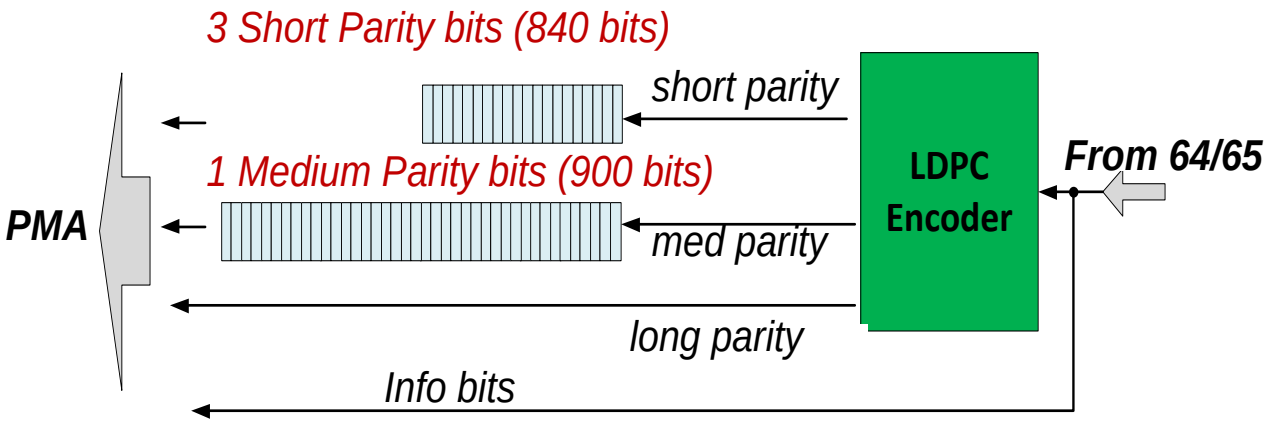


Buffers at the Transmitter

- Option 1
  - 1600 bit additional buffer is required
  - Streaming, simple management

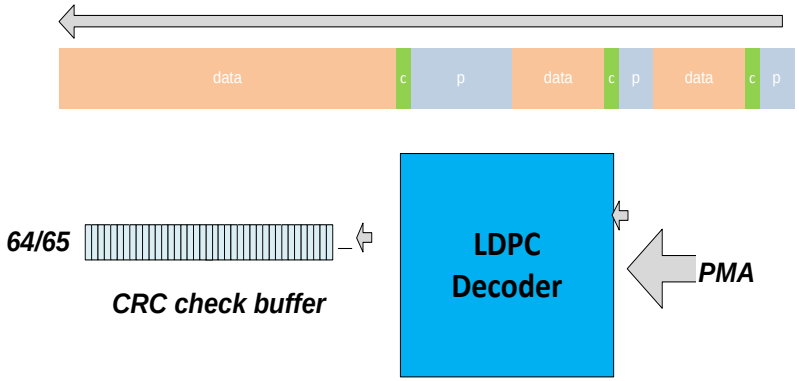


- Option 2
  - Two buffers with total 1740 bits are required
  - More complex management

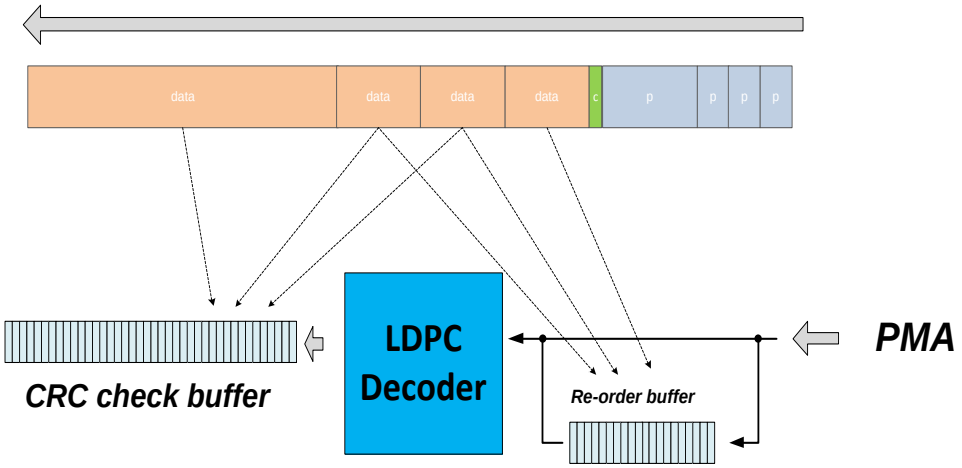


Buffers and Reordering at the Receiver

- Option 1
  - Simple no buffers no special management



- Option 2
  - Large buffers required to store intermediate info bits before and after decoding
  - Reordering buffer measurement



size = 3 * short info = 2520 bits

Summary

- Option #1 – FEC and CRC per block
  - Simple streaming data
  - 1600 bits buffer at the transmitter, no buffers at the receiver
  - Additional delay of max 6.4 uSec
  - Insignificant compared to overall upstream latency (upto ~ 1% and usually much less)
- Option #2 – FEC and CRC at the end
  - Reduced latency
  - Requires larger buffers at the transmitter and receiver
  - Required buffer management for re-ordering
- Latency gain of option #2 is insignificant and does not justify the additional complexity to the straight forward, conventional design of Option #1

Conclusion

- Current baseline text specifies FEC structure with parity and CRC at the end of each codeword (“Option 1”)
- There is no need to change the existing baseline text