

802.3bn Link Ad Hoc Status Update

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Review of Ad Hoc Calls

- Presentations on calls
 - MDIO registers for downstream hunting - Bill Keasler, Ikanos
 - PLC for TDD Mode – Nicola Varanese, Qualcomm
 - Downstream Framing – Ed Boyd, Broadcom & Marek Hajduczenia
 - Downstream Register Instruction – Ed Boyd, Broadcom & Hesham ElBakoury, Huawei & Duane Remein, Huawei
- 8 Straw Polls Taken (see next slides)
- Downstream PLC Baseline Proposal Created

Straw Poll #12

- The 8 (4K FFT) or 16 (8K FTT) sub-carriers for the downstream PLC will be adjacent carriers.
- Yes: 11
- No: 0
- Abstain: 2

Straw Poll #13

- The downstream PLC must be placed within the minimum EPoC spectrum block (currently 24MHz)
- Yes: 12
- No: 0
- Abstain: 0

Straw Poll #14

- The downstream PLC locations will be on a 1MHz grid (interval).
- Yes: 8
- No: 0
- Abstain: 4

Straw Poll #15

The PLC preamble will repeat on a configured PLC Cycle Time.

In FDD mode, the PHY Cycle Time will be time aligned with the staggered pilot pattern.

- Yes: 10
- No: 0
- Abstain: 2

Straw Poll #16

In TDD mode, the PHY Cycle Time will be time aligned with the TDD Cycle. The PHY Cycle Time may be multiples of the TDD Cycle.

- Yes: 10
- No: 0
- Abstain: 2

Straw Poll #17

- PLC Preamble Symbols will have a single fixed pattern & modulation order.
 - The PLC Preamble will not have error correction for burst noise.
 - Infrequent errors in the preamble shouldn't prevent decoding of the PLC after locking onto the PLC cycle.
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- Yes: 9
 - No: 0
 - Abstain: 0

Straw Poll #18

- In the EPoC continuous downstream PHY, the FEC codeword will be of a fixed size, that is an integer multiple of 65 bits (shortened 64b/66b encoded vector).
- Yes: 11
- No: 0
- Abstain: 0

Straw Poll #19

- In the EPoC Continuous downstream PHY, the PLC shall transmit (either in all or some PLC frames) a pointer in bits to identify the start of the first FEC complete codeword in the following PLC frame.
- Yes: 11
- No: 0
- Abstain: 0

THANK YOU