Downstream PHY Link Channel Baseline Proposal

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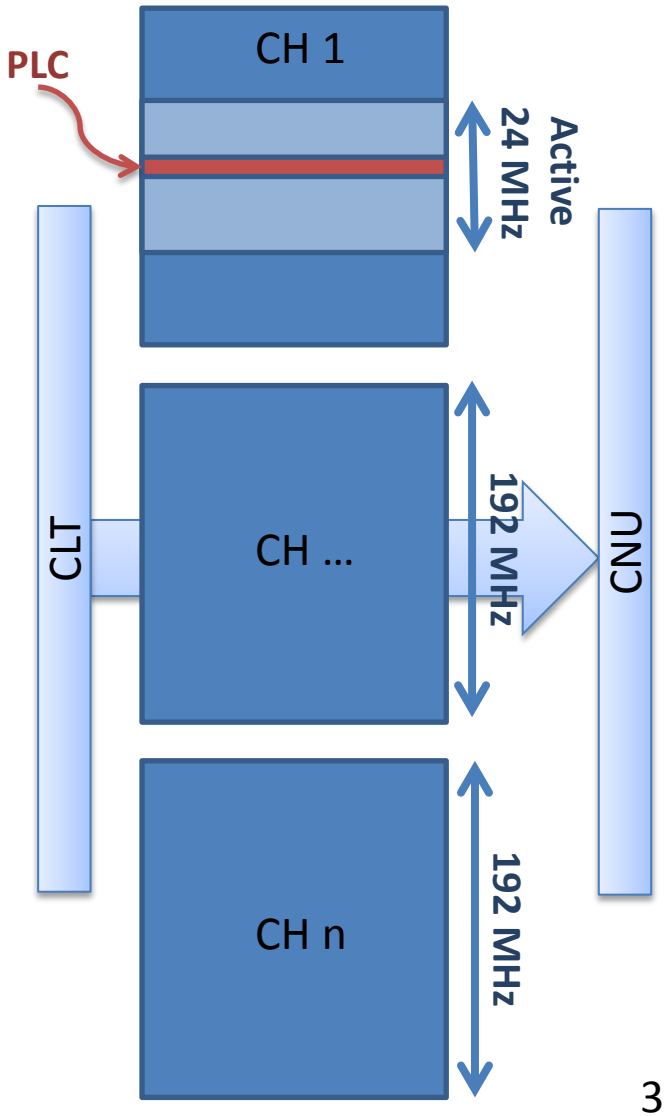
Overview

- Objective
  - The PHY Link Channel (PLC) provides a physical layer management path for configuration and status monitoring outside of MAC layer (MPCP) messages or OAM messages.
  - The PLC can be used before or after MAC layer registration to communicate with a remote PHY.
  - The PLC allows for adapting the PHY configuration to coax conditions.
  - The PLC allows for hitless configuration switch over. *(SP#10)*
  - The PLC allows for feature detection and negotiation of features between the CLT PHY and CNU PHY.

Downstream PHY Link Channel Location

- CLT Location Configuration
  - The PLC location will be configured via MDIO on the CLT PHY.
  - Support for Multiple PLCs is for further study. (i.e. redundancy or channel limited CNUs)
  - PLC must be placed on a 1MHz grid between (x MHz and y MHz based spectrum Ad Hoc) (SP #14)
  - PLC must be placed in a minimum continuous spectrum of 24MHz wide. (SP #13)
- CNU Location Detection
  - The PLC location will be detected by the CNU PHY using a vendor specific search algorithm. (last location, carrier configuration information, etc)
  - MDIO registers are defined to enable hunting.

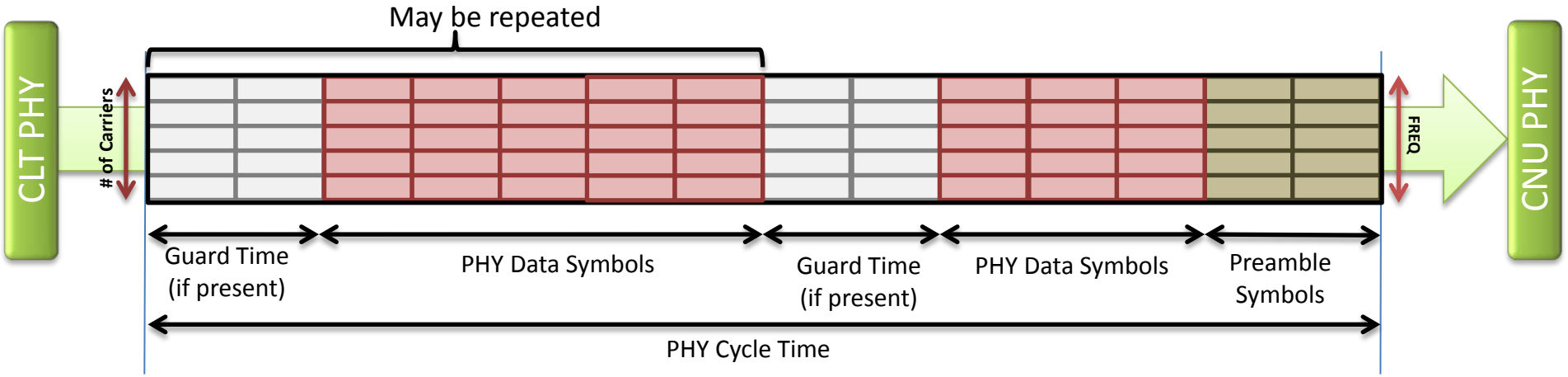


Downstream PLC Hunting

- MDIO Registers will be defined to control the Downstream PLC Hunting in the CNU PHY.

- MDIO register definition
  - PLC_SRCH_ FREQ_ START (R/W) [13 bits]
    - 1 MHz units (range of 0 to 8 GHz)
  - PLC_SRCH_ FREQ_ STEP (R/W) [8 bits]
    - 1 MHz units (range of 0 to 255MHz)
  - PLC_SRCH_CNT (R/W) [13 bits]
    - Number of steps to take (range of 0 to 8K-1)
  - PLC_SRCH_ CNTRL (R/W) [1 bit]
    - Start and Stop a search
  - PLC_SRCH_ STATUS (RO) [2 bit]
    - Indicates a search in progress
    - Indicates a completed search as successful or unsuccessful.

Downstream PHY Link Channel Definition (1)

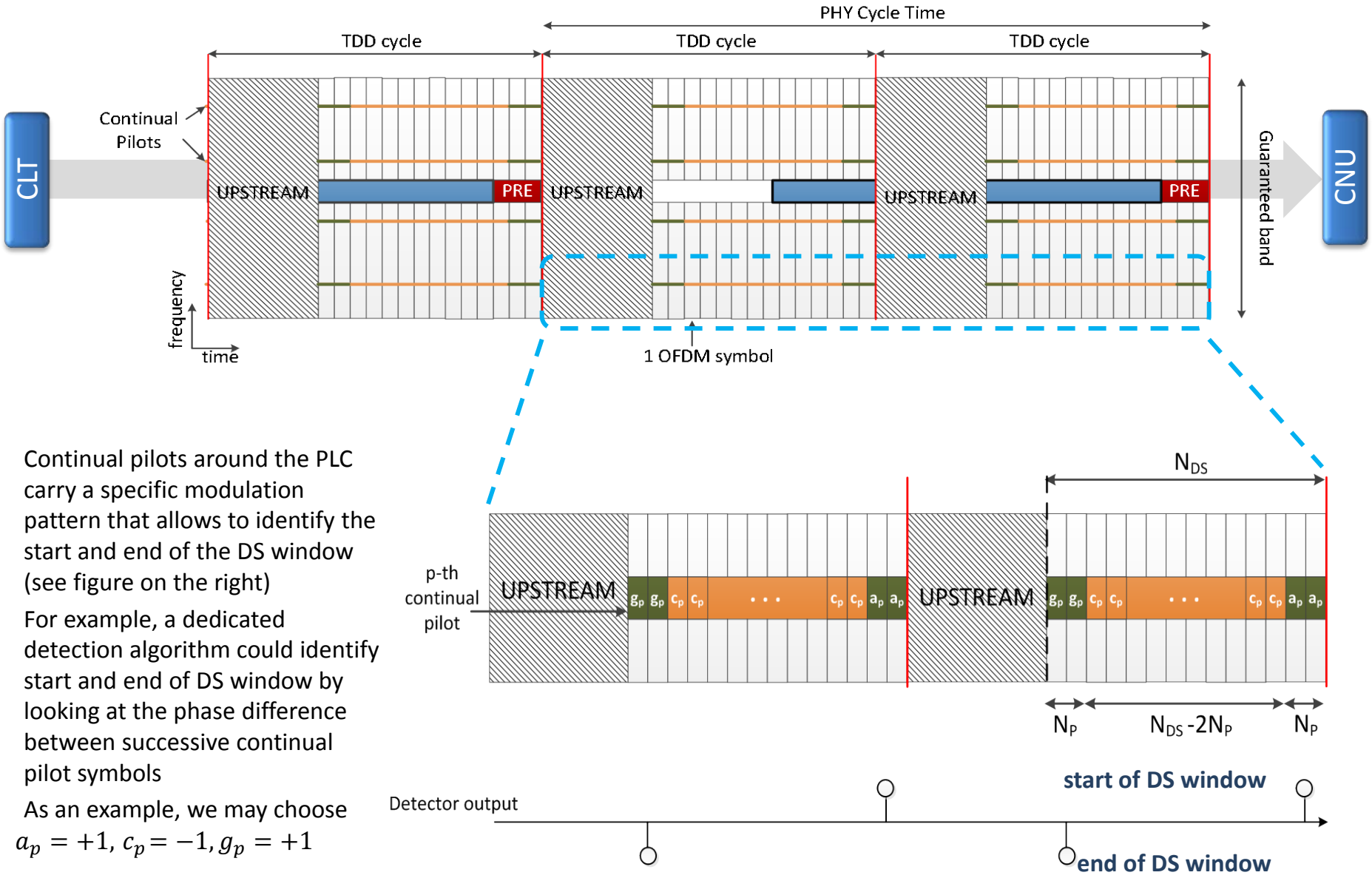


- The PHY Link Channel occupies 400KHz of spectrum. *(M#26)*
  - The PLC will be composed of 8 adjacent sub-carriers with the 4K FFT and 16 adjacent sub-carriers with the 8K FFT. *(M#26) (SP #12)*
- The PHY Link Channel is isolated in frequency from the MAC layer data. *(M#25)*
- The PHY Link Channel will use the same cyclic prefix (CP) and symbol duration as the MAC data channel. *(M#5)*
- The PHY Link Channel will consist of Preamble Symbols and PHY Data Symbols. Guard Time or Empty symbols maybe included. *(M#25)*
- The PHY Link Channel will use 16-QAM for all PHY Data Symbols. *(M#3)*

Downstream PHY Link Channel Definition (2)

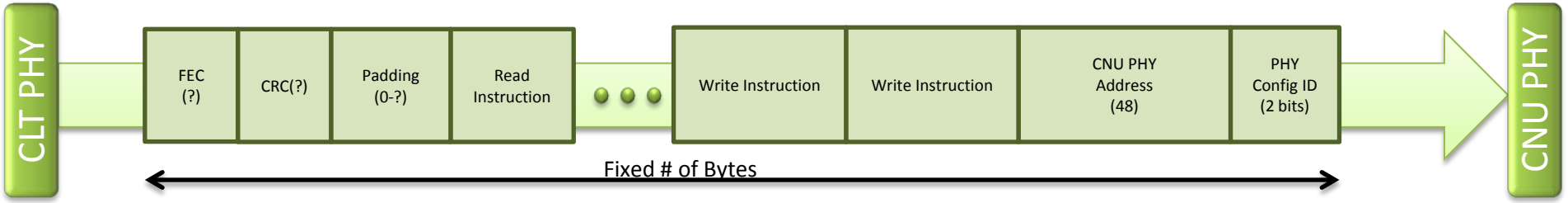
- The PHY Link Channel will be a repeated cycle. (SP #15)
- The PHY Cycle time will be aligned with the MAC data channel.
  - In TDD mode, the PHY Cycle Time will be time aligned with the TDD Cycle Time (maybe multiple). (SP #16)
  - In FDD mode, the PHY Cycle Time will be time aligned with the staggered pilot pattern. (SP#16)
  - The minimum and maximum PHY Cycle Time will be TBD
- The PHY Link Channel cycle will contain TBD preamble symbols.
- Preamble Symbols will have a single fixed pattern & modulation order (SP #17)
  - Preamble pattern is TBD.
- The Preamble will not have error correction for burst noise. (SP #17)
- Infrequent errors in the preamble shouldn't prevent decoding of the PLC after locking onto cycle. (SP #17)

Detecting start and end of DS window in TDD Downstream PLC



- Continual pilots around the PLC carry a specific modulation pattern that allows to identify the start and end of the DS window (see figure on the right)
- For example, a dedicated detection algorithm could identify start and end of DS window by looking at the phase difference between successive continual pilot symbols
- As an example, we may choose $a_p = +1, c_p = -1, g_p = +1$

Downstream PHY Link Frame



- A PHY Link Cycle will have one or more Downstream PHY Link Frames
- The PHY Link Frame will be a fixed size
- PHY Link Frame will contain a PHY Destination Address.
  - The MAC Address of the CNU maybe used as a PHY address.
  - CNU PHYs will receive instructions from the Broadcast Address or Unicast Address.
- The PHY Link Frame will contain a 2-bit PHY Configuration Identifier to allow for hitless switchover of select PHY configurations. *(SP#10-11)*
- The PHY Link Frame will contain one or more instructions to a remote PHY's registers.
- The PHY Link Frame may contain a CRC-? for error detection (TBD)
- The PHY Link Frame will contain forward error correction. *(M#23)*

Proposed Motion

Use boyd_3bn_02_0513.pdf slides 2-8 as starting point for the development of the PHY Link baseline.

Moved:

Seconded:

THANK YOU