Framing for EPoC Continuous Downstream

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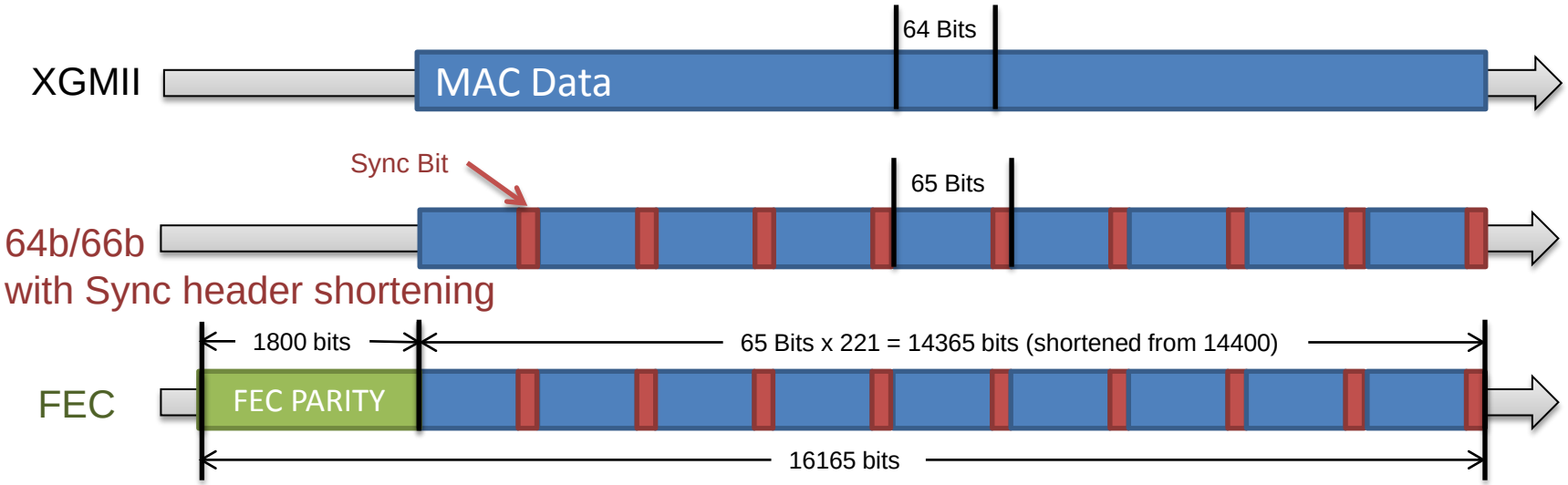
Overview

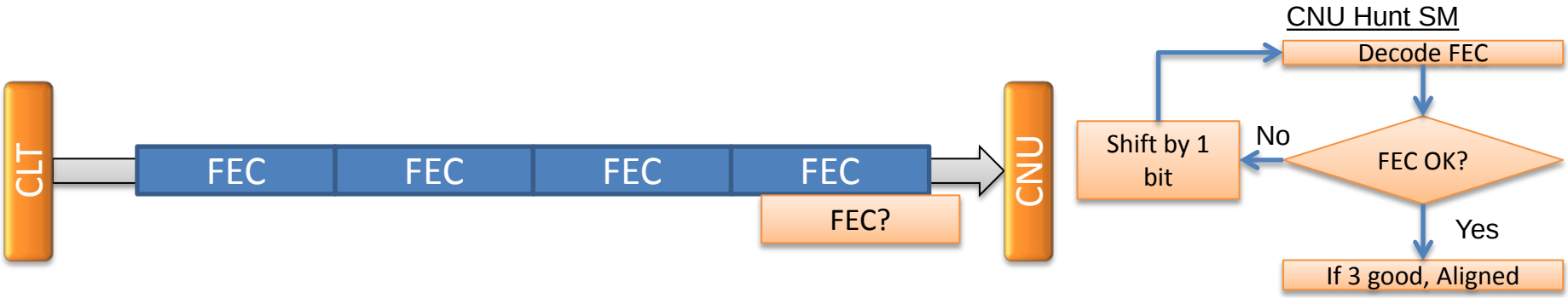
- At the last meeting, we approved a motion to use 64b/66b encoding with a single sync bit (65 bits).
- The 64b/66b encoding provides a simple method to find packet starts and ends.
- This presentation shows a simple method for aligning 66-bit vectors with FEC codewords in the continuous downstream PHY.
- This presentation shows options for aligning the FEC codewords to the PLC framing in the continuous downstream PHY. (It does not suggest the selection of a specific FEC)

XGMII to 64b/66b to FEC



- XGMII data stream is encoded with 64b/66b.
  - Only 1 of 2 sync bits are added. (~1.5% of overhead vs ~3% of overhead)
- 65 bit code is aligned to fixed codeword size.
  - Simplifies alignment to 65 bit vector (No need to hunt for vectors)
- For an example code of 8/9 with 14400 data, 1800 parity, and 16200 total bits…
  - Shortening to 14365 bits (221x65) is an even 65 bit boundary.
  - EPoC fills 14365 bits with actual useful data, adds 35 bits of zeros, and computes 1800 bits of parity. The zeros added are not transmitted over the channel.
  - Cost of FEC codeword size alignment is (14400/16200) – (14365/16165) =.024%.

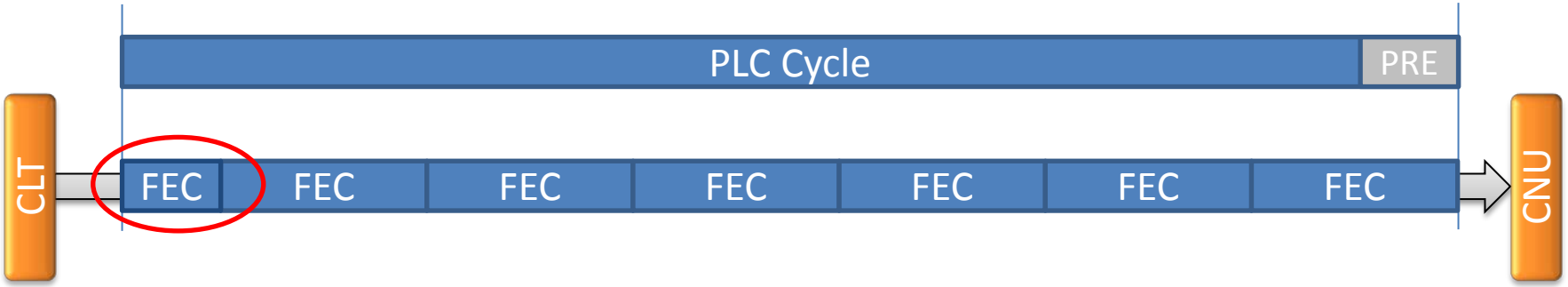
Finding FEC codeword boundaries



- The continuous downstream receiver needs to determine the start and the end of FEC code words.
- The receiver could hunt for the FEC codeword start and end by trying to decode at different bit offsets.
- Hunting for the FEC codeword will be slow and challenging if the link has high BER, certain data patterns, or long codewords (16,200 bits has been proposed).
- Methods for aligning the FEC codeword with the PLC framing will be explored to simplify and speed up alignment.

Position-based hunting for alignment will be too slow

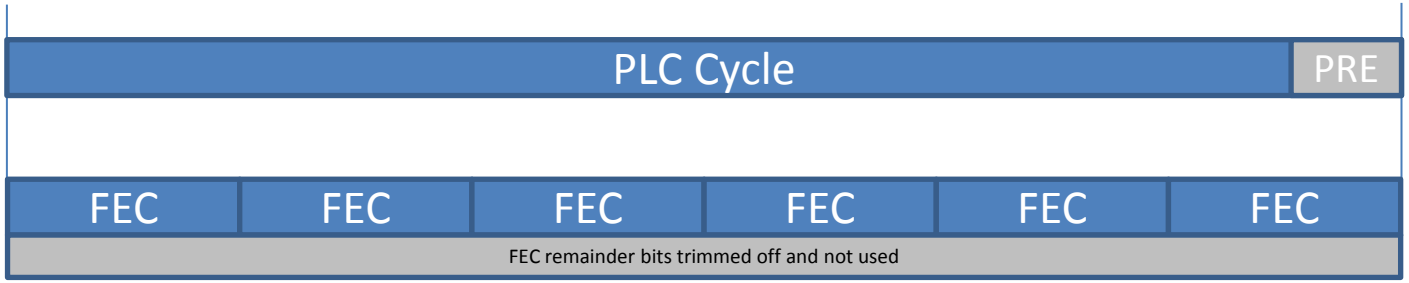
PLC Cycle Aligned with Shortening



- The PLC provides a fixed periodic cycle in the downstream.
- The start of the PLC cycle could be aligned to the start of the FEC codeword.
- Since the size of the PLC Cycle may not align with a multiple of FEC codewords, the final codeword in the PLC cycle needs to be shortened.
- The shortened codeword will cause a increase rate into the FEC decoder (codewords per second is increased)
- The shortened codeword will cause additional overhead (lower MAC rate) in the last symbol of the PLC cycle. This change in data rate is a problem for a fixed delay and rate Ethernet PHY.

PLC Aligned with Shortening doesn't work easily with the EPON MAC

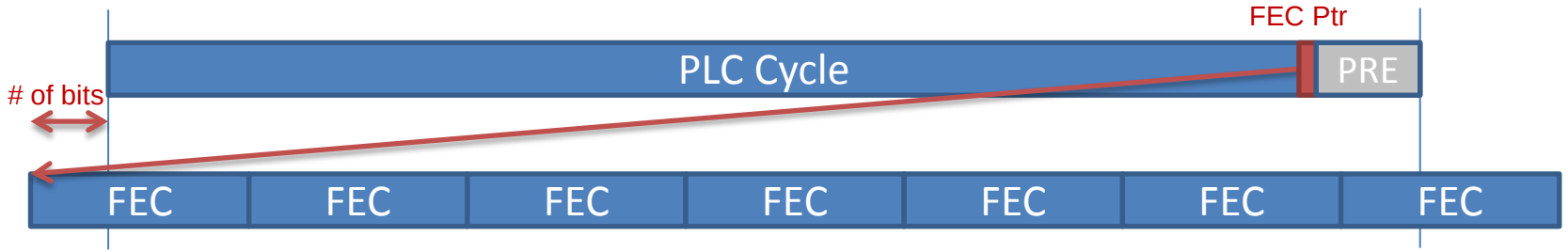
PLC Aligned with Fixed Size



- The PHY capacity could be reduced so the number of bits in the PLC cycle is an even multiple of the FEC codeword size.
- If we assume a FEC codeword of 16,165 bits and PLC cycle of 2.5ms. The worst case waste is 16,164 bits/2.5ms=6.466Mbps

Simple solution but significant waste on smaller channels.

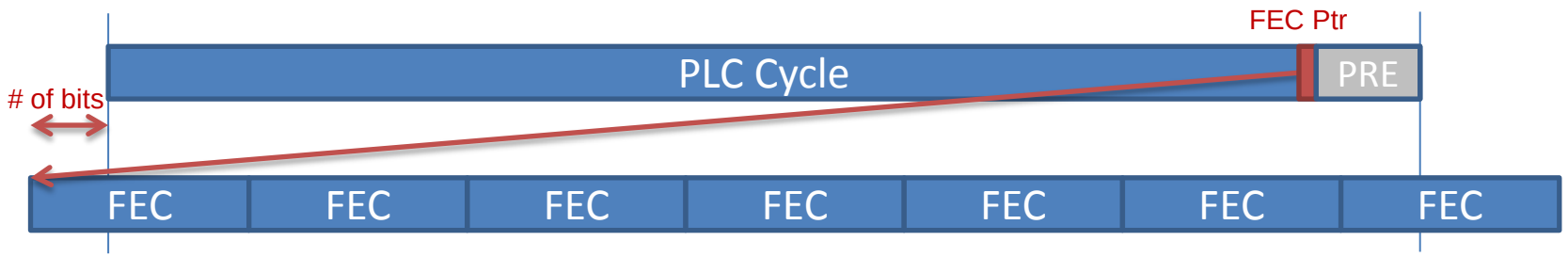
PLC FEC Pointer



- PLC contains a 16 bit pointer field to identify start of the FEC codeword in the next PLC cycle.
- CNU PHY would have MDIO Register Address for FEC start bit number that can be set by PLC and automatically updated on every PLC cycle.
- Alignment takes one PLC cycle, roughly 2.5ms.
- MAC Data Channel is fully utilized.
- Constant MAC Data Rate and no need for shortened codewords.
- Once aligned, receiver counts bits to find codeword boundaries so the FEC pointer is not required on all PLC cycles.
- CLT PHY can transmit FEC Pointer in some or all PLC frames.

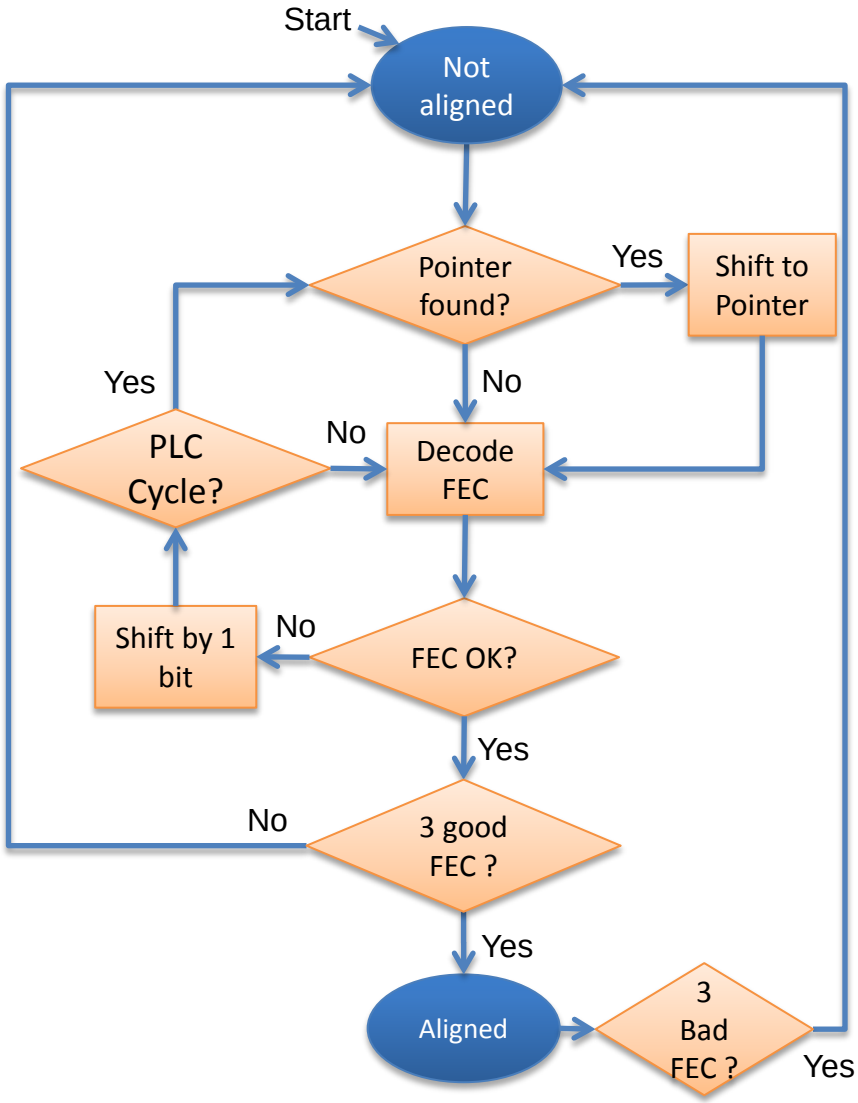
EPoC should support a PLC based FEC Pointer for FEC alignment

PLC FEC Pointer (cont)



- The PLC pointer contains the number of bits left in the FEC code word at the end of the PLC Cycle.
- The next PLC pointer can be easily calculated by the CLT/CNU PHY
  - Calculate the remainder for the PLC cycle configuration (# of bits per PLC cycle divided by the FEC Codeword size).
  - Add the remainder to the last FEC Ptr to get the next FEC pointer.
  - When the sum exceeds the codeword size, subtract the codeword size.
- A “Bit count” is preferred over sub-carrier number since it easily handles configuration changes on the next PLC cycle, handles FEC codewords sharing a sub-carrier symbol, and it is a simple calculation for the next pointer.

Integrating the FEC Pointer & Hunting



- The addition of a pointer does not exclude hunting.
- The pointer only accelerates the search process.
- This example flow chart shows a modified hunting approach that is assisted by the addition of the FEC pointer from the PLC.
- The hunting process will jump to a position when it is unaligned and the PLC contains a valid FEC pointer.
- If a FEC pointer is not present, the hunting process will continue to hunt by shifting bits.
- The FEC pointer is not required after alignment.

Conclusions

- Aligning the 64b/66b vectors to the FEC codeword simplifies alignment and costs very little bandwidth.

- Four options were considered for easy alignment to FEC codewords.
  - Hunting is too slow.
  - PLC Cycle Alignment with Shortened codewords adds complexity and fluctuates the MAC data rate.
  - PLC Cycle Alignment with fixed codewords costs too much bandwidth
  - PLC FEC pointer has good utilization and quick alignment.

64b/66b codeword alignment and FEC pointer alignment should be adopted for EPoC downstream framing.

Straw Poll #TBD

- In the EPoC continuous downstream PHY, the FEC codeword will be of a fixed size, that is an integer multiple of 65 bits (shortened 64b/66b encoded vector).

- Yes:
- No:
- Abstain:

Straw Poll #TBD

- In the EPoC Continuous downstream PHY, the PLC shall transmit (either in all or some PLC frames) a pointer in bits to identify the start of the first FEC complete codeword in the following PLC frame.

- Yes:
- No:
- Abstain: