EPoC TDD – Data Detector and Downstream PCS Considerations

Andrea Garavaglia and Patrick Stupar
(Qualcomm)

Background and Scope

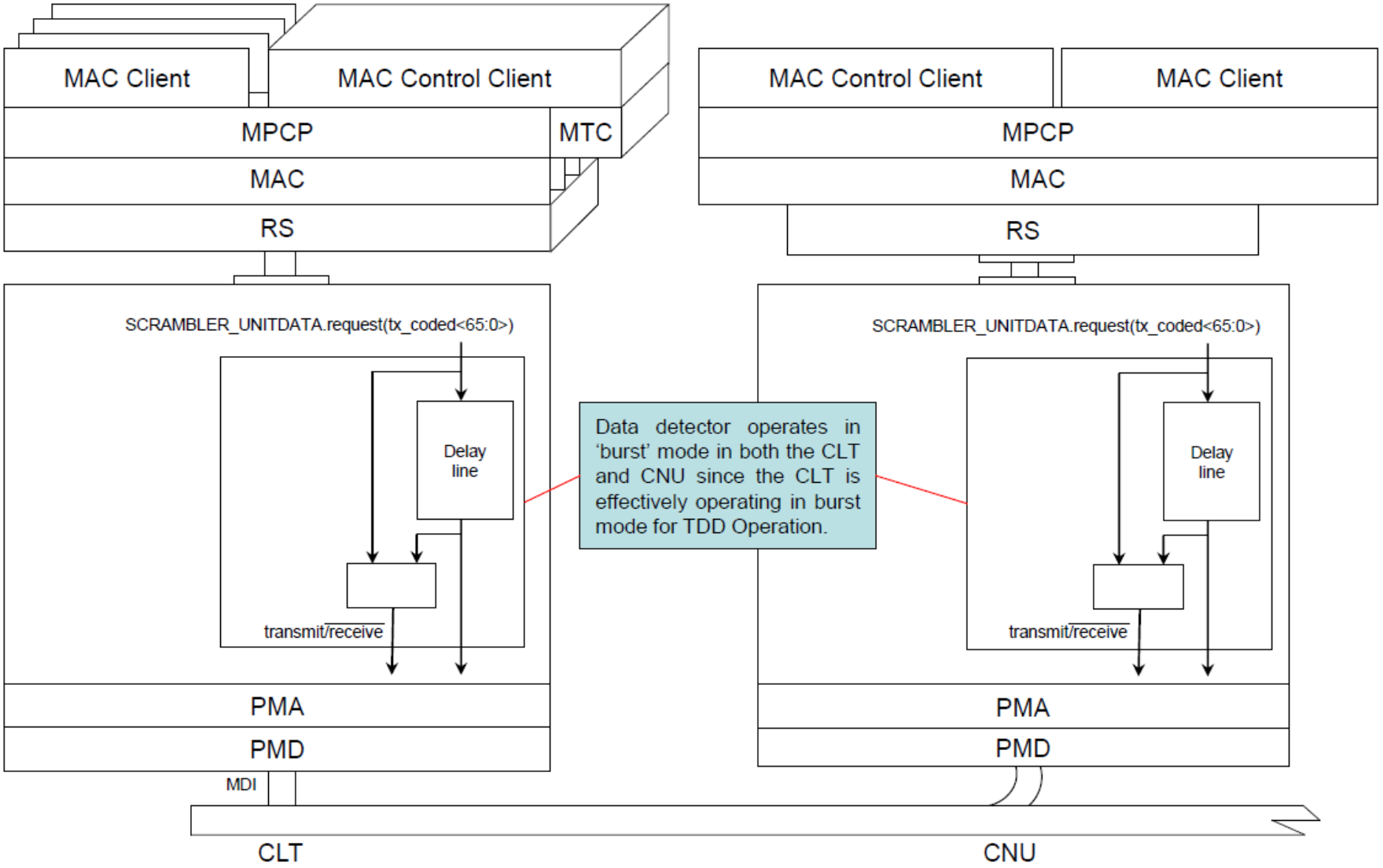
- During the last IEEE 802.3bn meeting, the first baseline proposal for EPoC has been approved by the Task Force, covering MPCP aspects for TDD mode operations

- Contributions presented in San Antonio (see law_01a_1112.pdf in [1]) and Phoenix (garavaglia_02a_0113.pdf in [3]) also highlighted that TDD has also impacts on the PCS aspects of EPoC, more in particular for the signaling to the PMD layer of transmission/reception bursts
  - *"Data detector operates in 'burst' mode in both the CLT and CNU since the CLT is effectively operating in burst mode for TDD Operation" – [1]*
  - *"CLT PCS needs to be modified to accommodate switching between transmit and receive in CLT" – [3]*

- This presentation illustrates how this can be achieved in EPoC, within the scope of the PCS sub-layer Clause, focusing on the TDD DS aspects
  - For upstream, some issues are common to FDD and TDD

TDD DS aspects for PCS – Clause 101

TDD Transmission – PCS Impact



Multipoint MAC Control – from [1] "IEEE 802.3 Architecture" – law_01a_1112.pdf

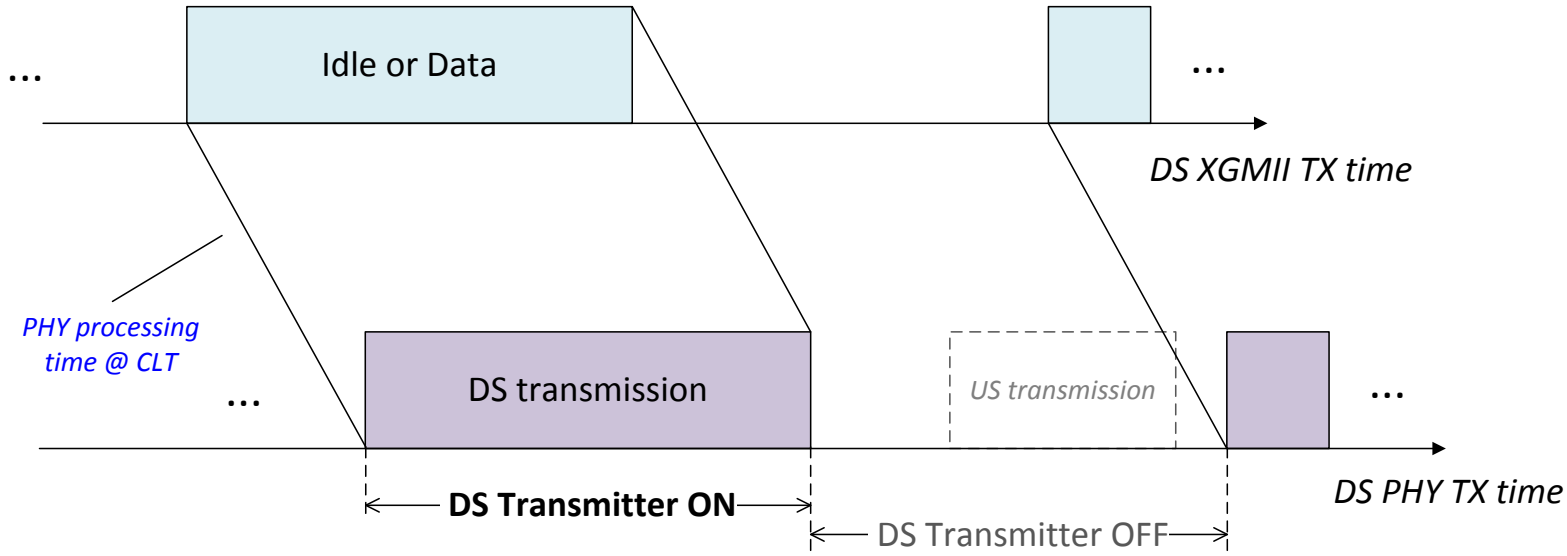
TDD DS Transmission – CLT PCS Impact

- The CLT PCS needs to trigger the switch between DS (TX) to US (RX) mode (and vice versa) of the PMD
  - When the DS window is open the PHY layer can transmit
  - When the US window is open the PHY layer shall not transmit

- Data detector in the PCS needs to identify the DS and US windows and provide signal to PMA for switching between TX/RX
  - Can be derived from 10G-EPON specification, Clause 76.3.2.5, applying to the CLT in DS the same principles applied for US burst in ONU
  - Input process for data detector derived from figure 76-16
  - Output process for data detector derived from figure 76-17, in particular from 76-17(a) for FDD and 76-17(b) for TDD

TDD DS Transmission – Timeline

- TDD configuration is established (e.g. via OAM) in the CLT and indicated to the MAC Control agent
- The CLT MAC Control can start transmission according to the configured TDD cycle, which propagates to the CLT PCS
- Data Detector in the CLT commands the switch between TX and RX at PMA via signaling, similar to what done in ONU for 10G-EPON



TDD Downstream – PCS Layer View (see [4])

- In TDD mode, the CLT transmitter includes a signal from the PCS data detector to the PMD to switch between transmit (DS) and receive (US) operations
- The signal is similar to what done in the US direction bursts and can be derived in similar way

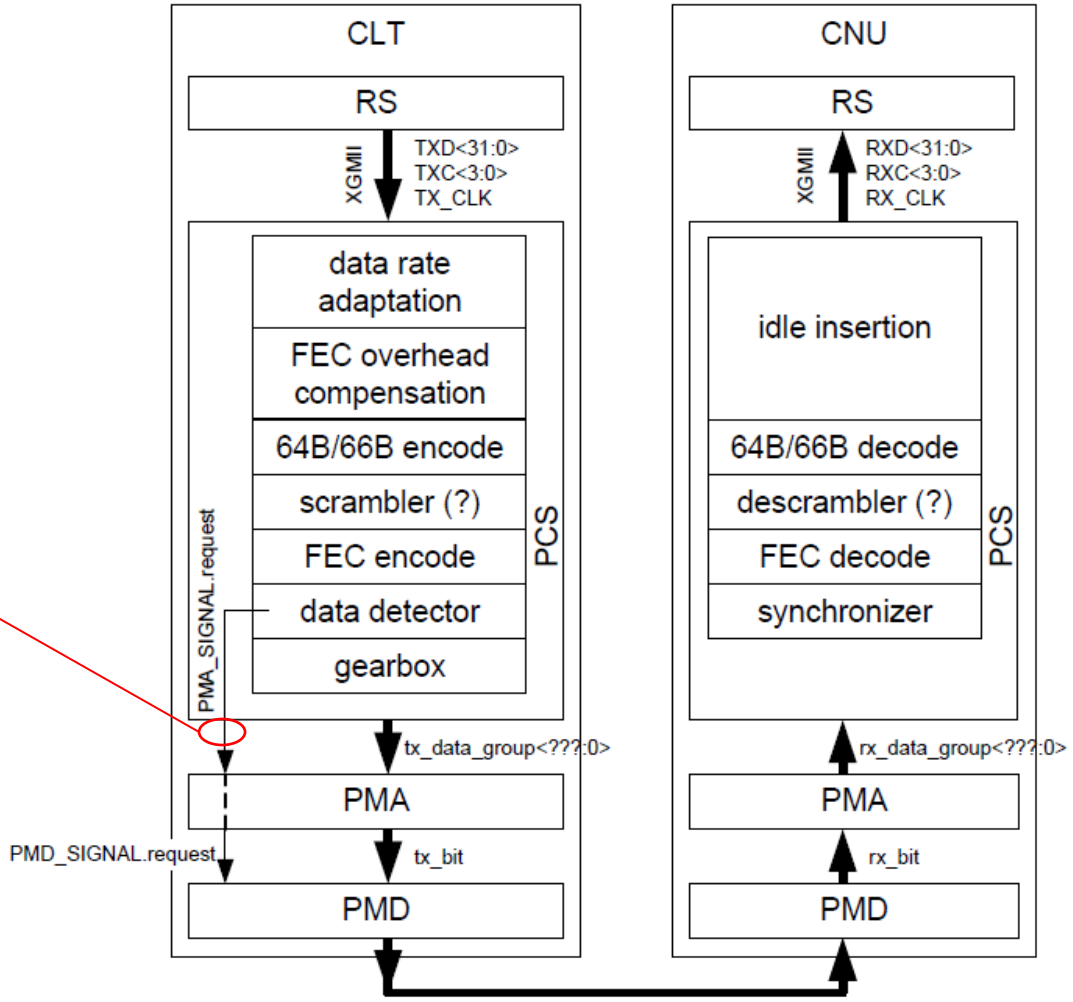
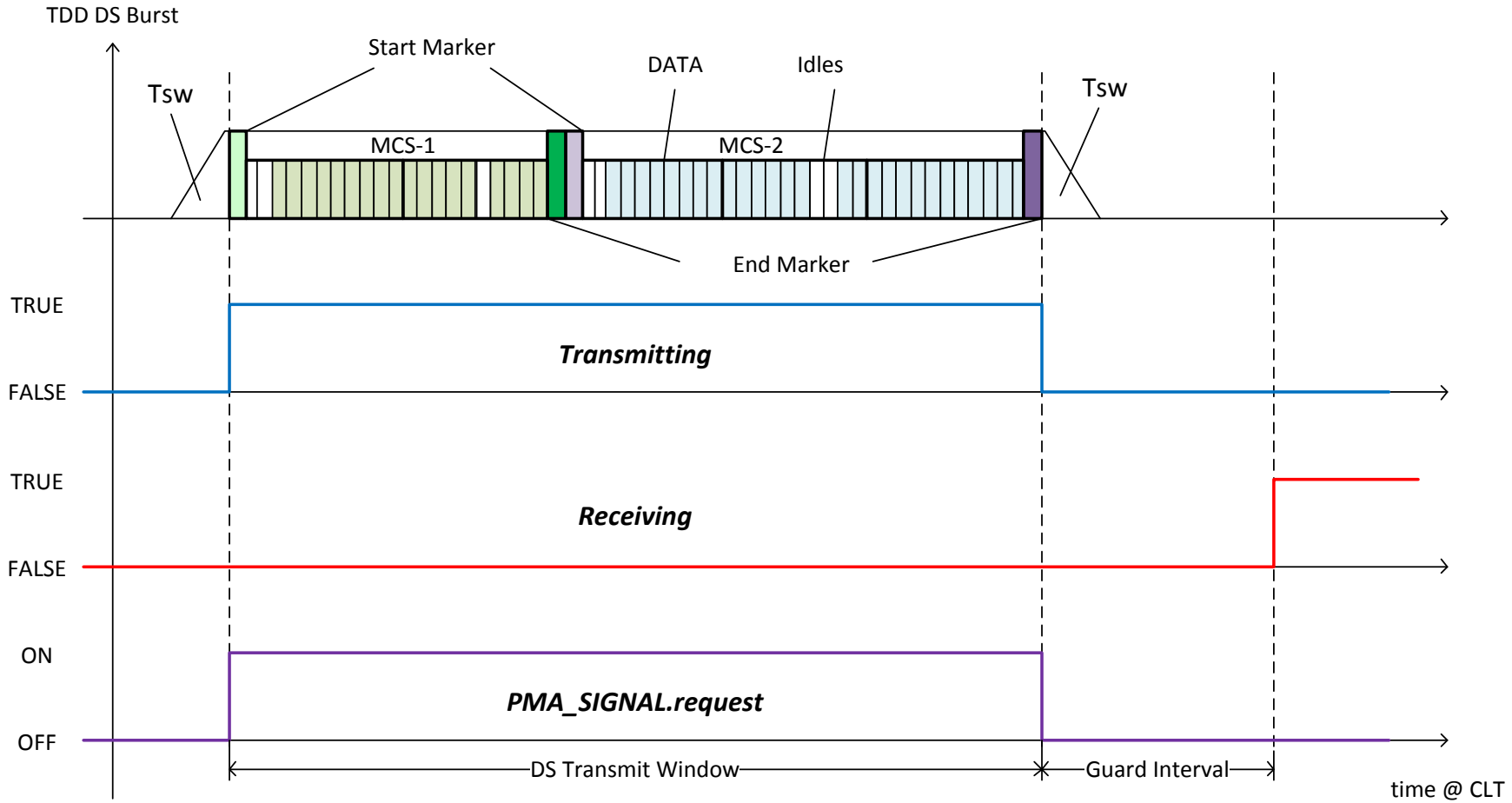


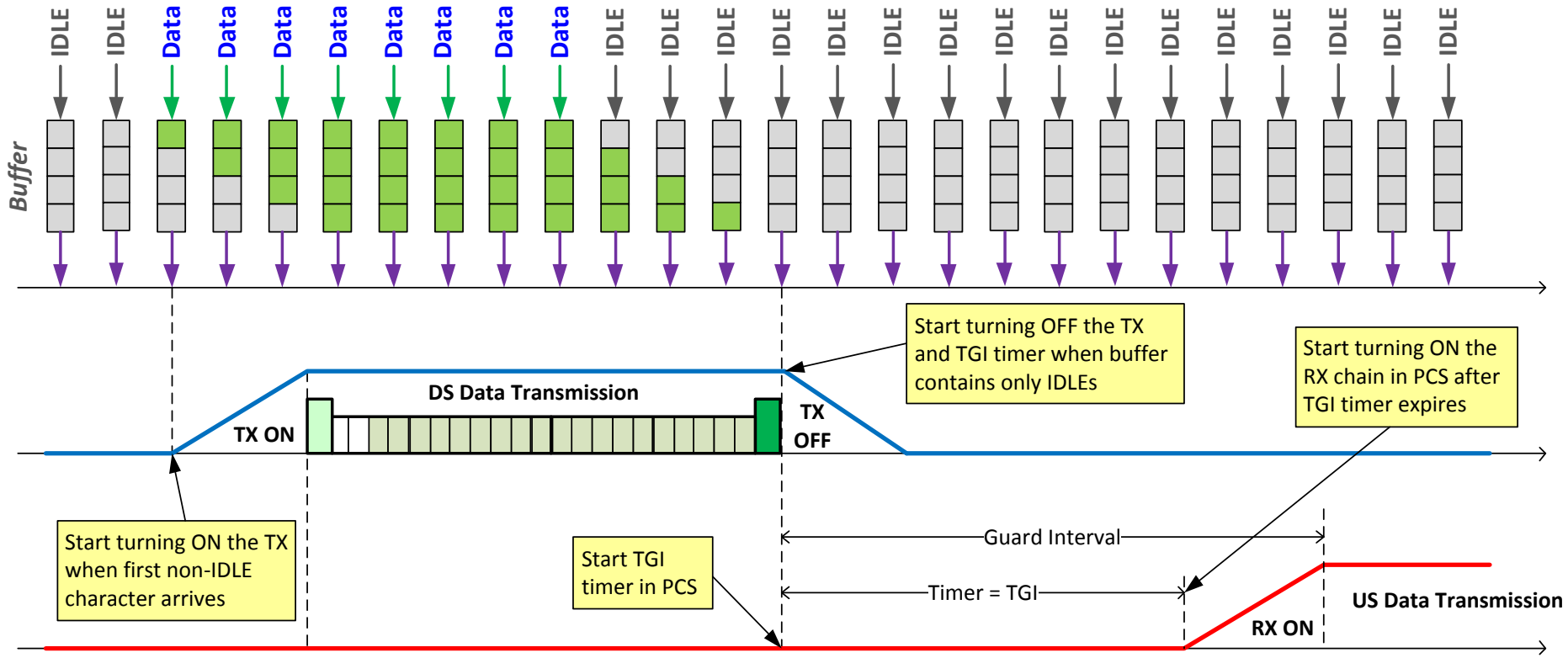
Figure 101–2—EPoC PCS functional block diagram, downstream path for TDD mode

TDD Downstream – Signals



- Clock recovery and gain control achieved via OFDM pilots – no Sync Pattern
- Burst delimiter and EOB replaced by Start and End markers

TDD Downstream – Data Detector approach

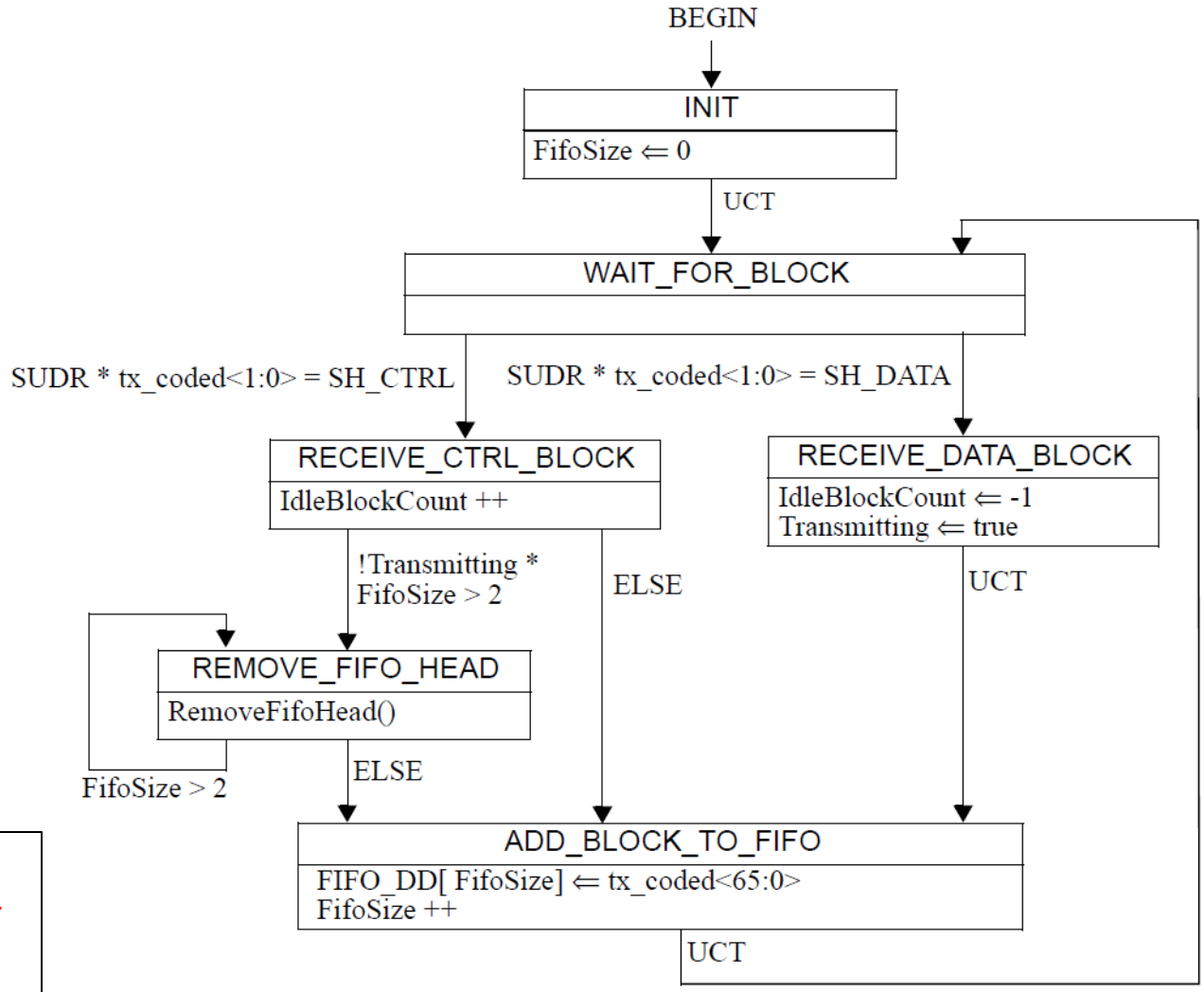


- Data detector to command TX ON and OFF at the CLT – RX starts with configured delay after the transmitter is OFF (TDD Guard interval, depending on max RTT)

Data Detector – see also kramer_1_0903.pdf [5]

TDD DS Data Detector – Input Process

- Reuse input process as in 10G-EPON, some parameters may need to be adjusted once TDD configuration and PHY decisions are finalized
- Define new variable *Receiving,* which is set to TRUE during reception time



IEEE 802.3-2012, Clause 76, Section 76.3.2.5, Figure 76-16

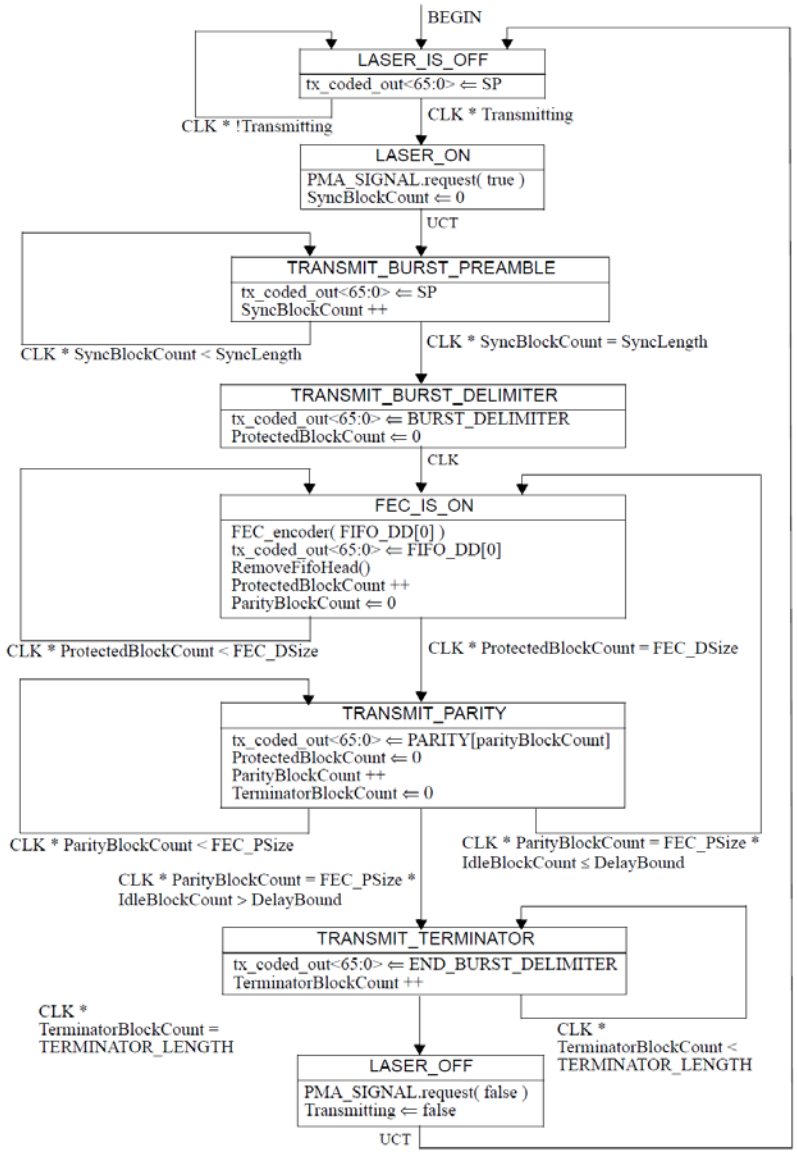
Note: the diagram will be updated once decision about burst structure and TDD parameters are finalized

TDD DS Data Detector – Output Process

Reuse output process of 10G-EPON ONU for the TDD CLT, with changes:

- *PMA_SIGNAL.request* signals switch between transmission and reception, toggling the PMD
- Define new variable *Receiving*, which is set to TRUE during reception time – triggered by configured timer after TX gets OFF
- Burst preamble/delimiter may be different or may not exist - to be adjusted once TDD configuration and PHY decisions are finalized
- FEC parameters, *SyncLength* and *DelayBound* to be defined once TDD configuration and PHY decisions are finalized
- Rename LASER -> RF

Note: the diagram will be updated once decision about burst structure and TDD parameters are finalized



IEEE 802.3-2012, Clause 76, Section 76.3.2.5, Figure 76-17b

Issues with data detector in TDD DS

- The TDD cycle is configured and therefore the transmitter in the CLT shall remain ON all the time during the DS Transmit Window
  - In case of no data, this may not happen as the data detector can misinterpret that and wrongly trigger the PMD signal
  - Can happen at the beginning, middle and end of burst

- In all cases, it may cause malfunctioning of the OFDM PHY, which remains aligned with OFDM symbols/time interleaving
  - For example, sequence of idles in the middle of a DS burst triggers TX OFF earlier than configured window
  - The timer to activate RX will count down and RX will be not aligned with the US transmit window
  - In addition, CLT MAC can still provide data for DS as part of the TDD window, which will potentially turn ON the transmitter

Possible solutions

To prevent these issues, some additional mechanisms can be considered when finalizing the data detector for TDD DS

- The TDD DS burst always starts and fills up gaps with a known packet or known character, so that the lack of data never delay the TX ON or anticipate TX OFF signal respect to the TDD configured timeline
  - As packet, one could consider a GATE message with no grant, as done in 10G-EPON for synchronization (see Clause 77.3.6.1, first paragraph)
  - As character, one could define a special IDLE, which does not get deleted by the Idle deletion process and fills up all gaps during the TDD DS transmit window
  - Similarly to the Guard Interval, also the DS Transmit window is aligned with a configured timer (certain number of OFDM symbols) triggered by the first special character/message

The 802.3bn TF is invited to look at these options for the TDD design

References

[1] **law_01a_1112**: “IEEE P802.3bn Architecture” – Juan Montojo (Qualcomm), David Law (HP), Marek Hajduczenia (ZTE), Ed Boyd (Broadcom)

[2] **garavaglia_02a_1112**: “Further Details on TDD” – Andrea Garavaglia (Qualcomm)

[3] **garavaglia_02a_0113**: “ EPoC TDD (baseline proposal)”, Andrea Garavaglia and Patrick Stupar (Qualcomm)

[4] **hajduczenia_3bn_01_0513**: “ IEEE Draft P802.3bn / D0.10 – Clause 101”, Marek Hajduczenia (ZTE)

[5] **kramer_1_0903**: “Data Detector”, Glen Kramer