# Baseline Proposal for technical decision #20

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# Summary

- 1 technical decision passed in associated with line coding for EPoC at the last meeting (#20)
- This slide deck summarizes the baseline proposal addressing technical decision #20, affecting the operation of PCS:
  - Line encoding process in Tx direction
  - Line decoding process in Rx direction
- Contribution hajduczenia_3bn_04_0513.pdf provides further detail associated with the line encode/decode operations in Tx/Rx directions (respectively), included in PCS clause outline presented at the last meeting

# Technical decision

- Technical decision: “EPoC PHY shall use the 64b/66b line coding (as defined in IEEE Standard 802.3-2012, Clause 49) with shortened Sync header (1 bit as in 10G-EPON)”
- Implications on the EPoC PCS draft:
  - Reuse 64b/66b encoder process as defined in Clause 49 (specifically, in 49.2.4 and in Figure 49-14);
  - Reuse 64b/66b decoder process as defined in Clause 49 (specifically, in 49.2.11 and in Figure 49-15);
  - No changes to the way line encoding/decoding works for simpler development

# What about shortened Sync Header?

- Sync Header shortening will take place within the FEC encoder. FEC encoder will aggregate a number of 66-bit vectors and truncate their Sync Headers by one bit prior to encoding and then transmission.
- In this way, we keep 64b/66b decoding process as defined in Clause 49 (fewer changes) and implement Sync Header truncation within new process, designed specifically for EPoC (FEC Encoder).
- The same is true in the receive direction, where FEC decoder recreates the full Sync Header after decoding is done

# Motion #

- Adopt hajduczenia_3bn_04_0513.pdf (content of subclauses 101.3.2.2 and 101.3.3.6) as baseline for draft D1.0 for 64b/66b encoder and decoder processes, respectively.
- Sync Header truncation/expansion will be handled within the FEC encoder/decoder.

- Moved by: Marek Hajduczenia
- Seconded by: Ed Boyd

- Technical motion (≥75%)