Multiple Downstream Profile Implications

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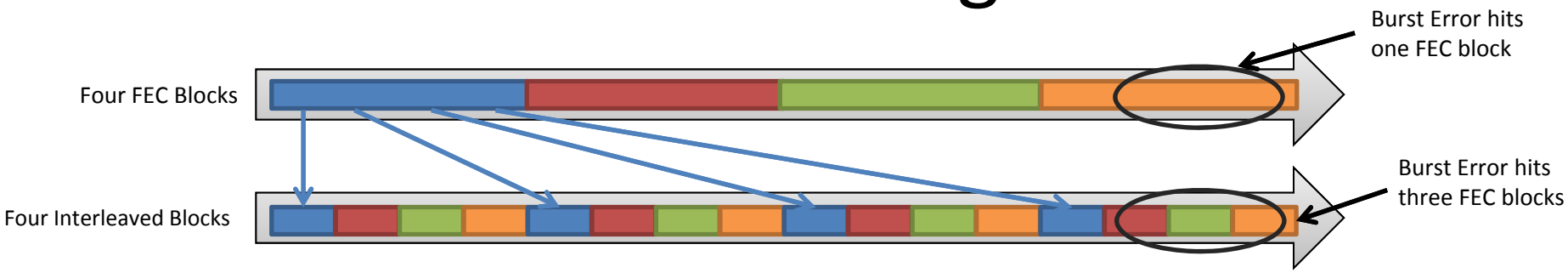
Overview

- EPON is a broadcast downstream with a constant data rate.
- Using Multiple Modulation profiles for groups of CNUs will be considered in this presentation.
- This presentation focuses on the required elements for an EPoC standard but many of the aspects maybe common with a DOCSIS 3.1 implementation.
- The reliability, delay, efficiency, and compatibility with 1G/10G EPON are the key criteria for evaluation.

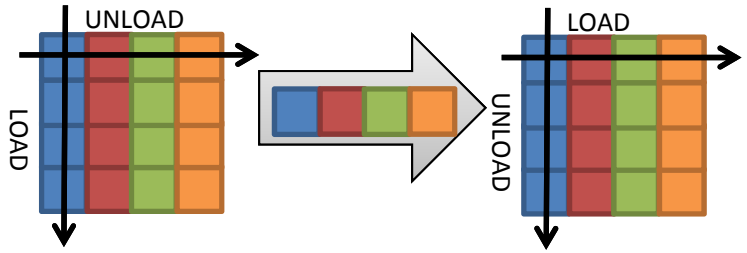
NOTE: I will use MMP (multiple modulation profiles) and SMP (single modulation profile) in this presentation.

Interleaver Background



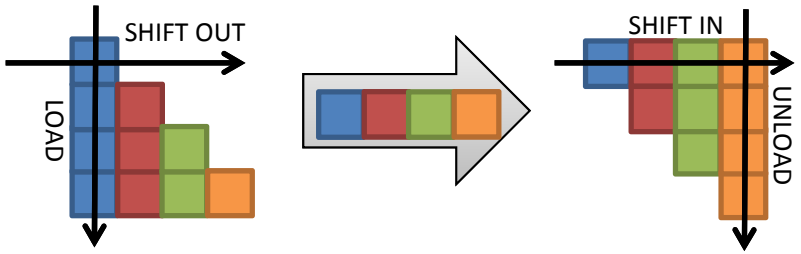
- FEC Blocks are split into chunks and spread over time to allow for burst error protection.
- Interleaving doesn't change efficiency but delay is added to spread code words.
- Minimum interleaver delay required is based on error correction capability and size of burst error protection. MinIntTimeReq = BurstErrorProtection*CodeWordSize/NumErrors
- Example: RS 239/255 corrects 8 bytes. For 20us of burst protection: MinIntTimeReq=20us*255/8=638us

Block Interleaver



- Loaded by columns and unloaded by rows.
- Starts and Stops on a block boundary.
- Full interleaver block time loaded and unloaded.
- Total Delay is double the interleaver spread time (block time) [1.2ms in example]
- Required for upstream.

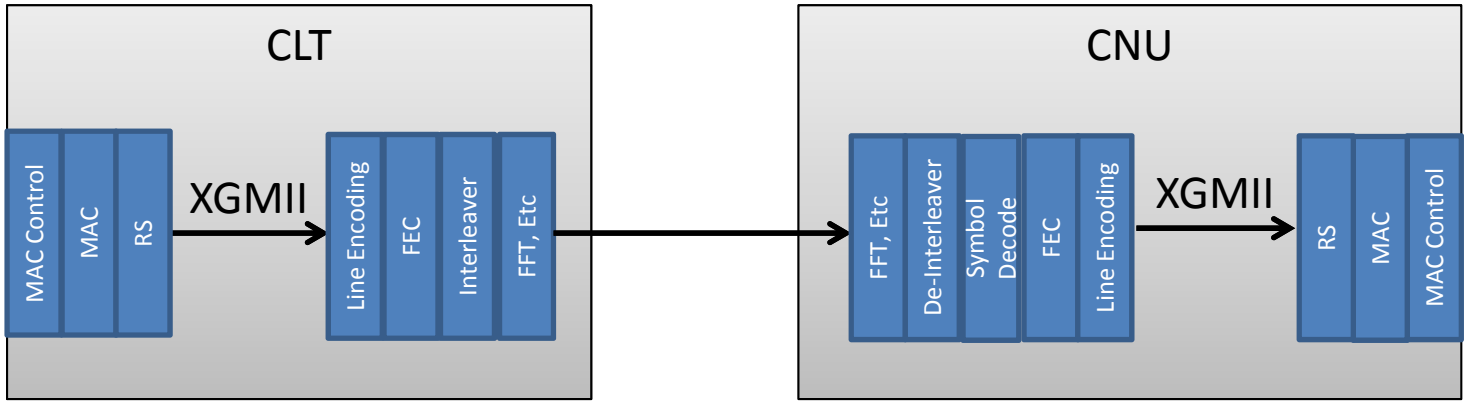
Convolutional Interleaver



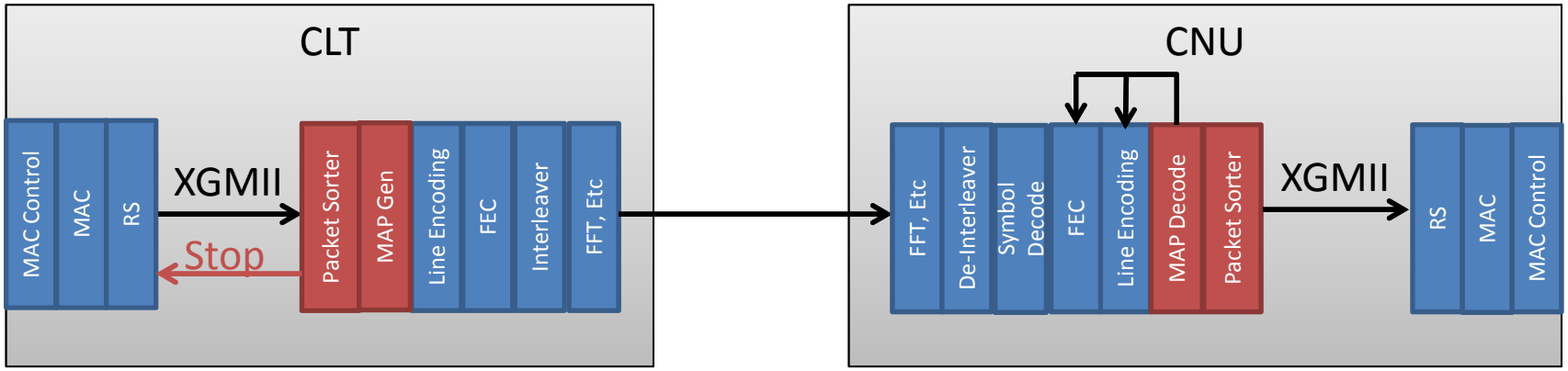
- Loaded by columns and unloaded by shifting out rows.
- Doesn't Start and Stop on block boundary.
- At reset, earlier blocks have invalid data since half of block is in receiver.
- Total Delay is the interleaver spread time (block time) [638us in example]
- Good for Single Broadcast Downstream.

Downstream Data Path

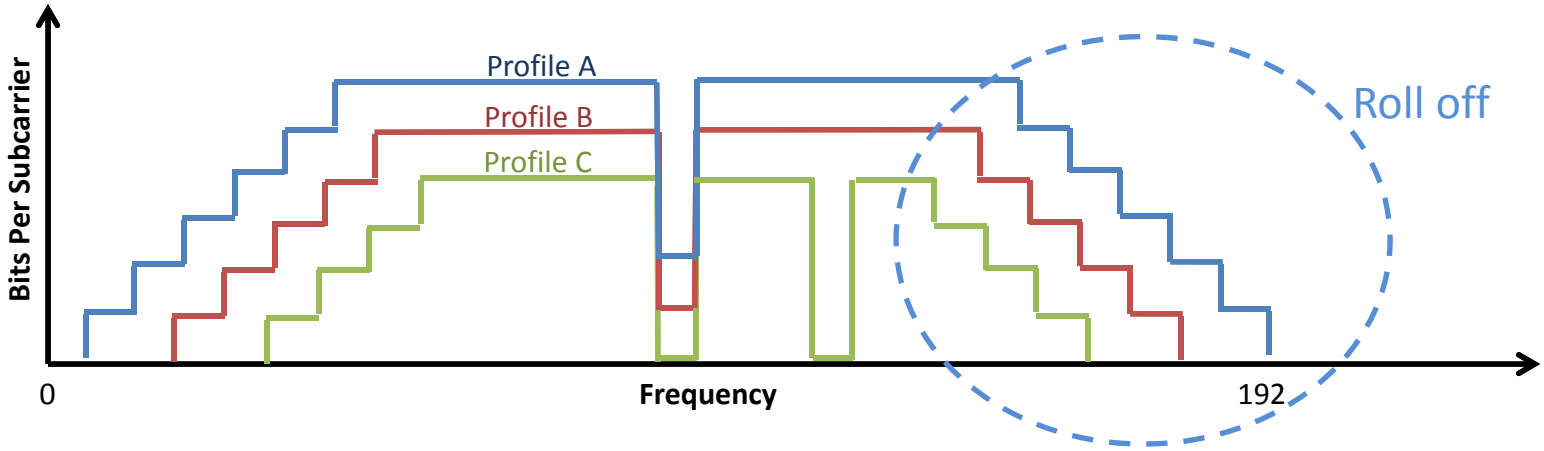
Single Modulation Profile Downstream



Multiple Profile Downstream



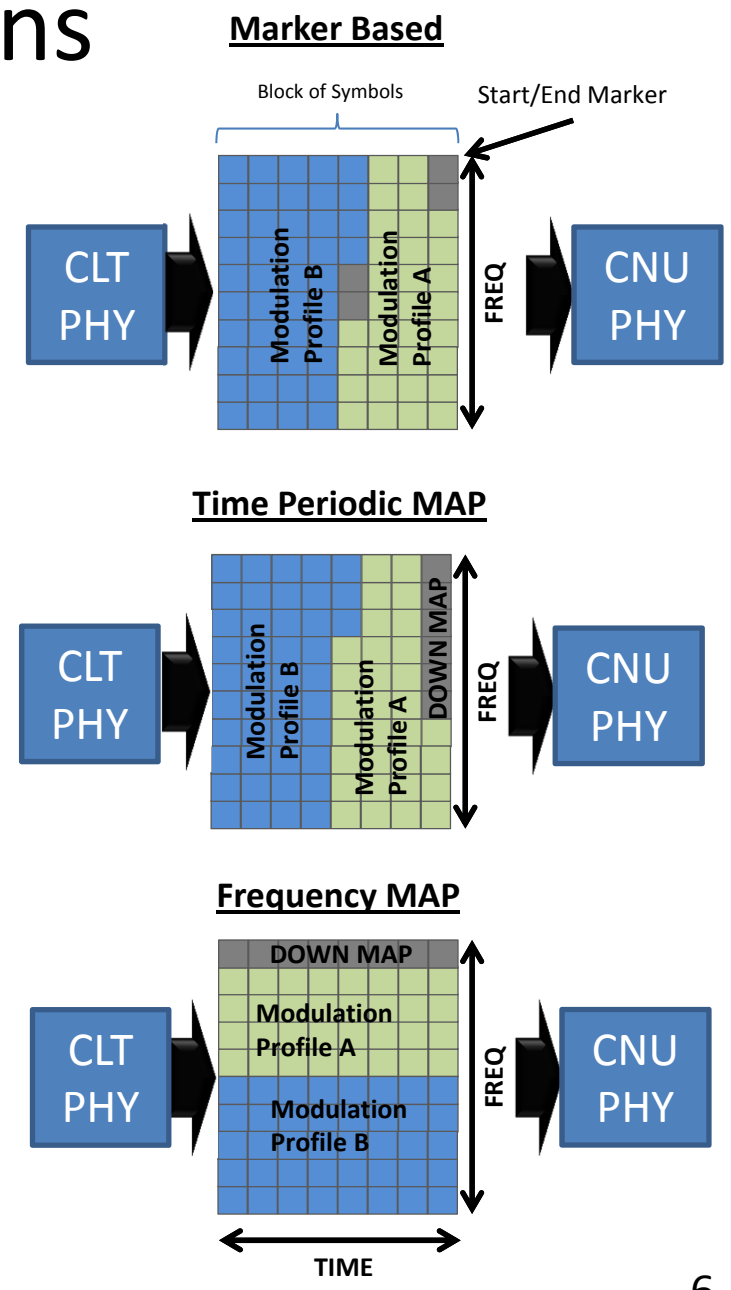
Downstream Profile



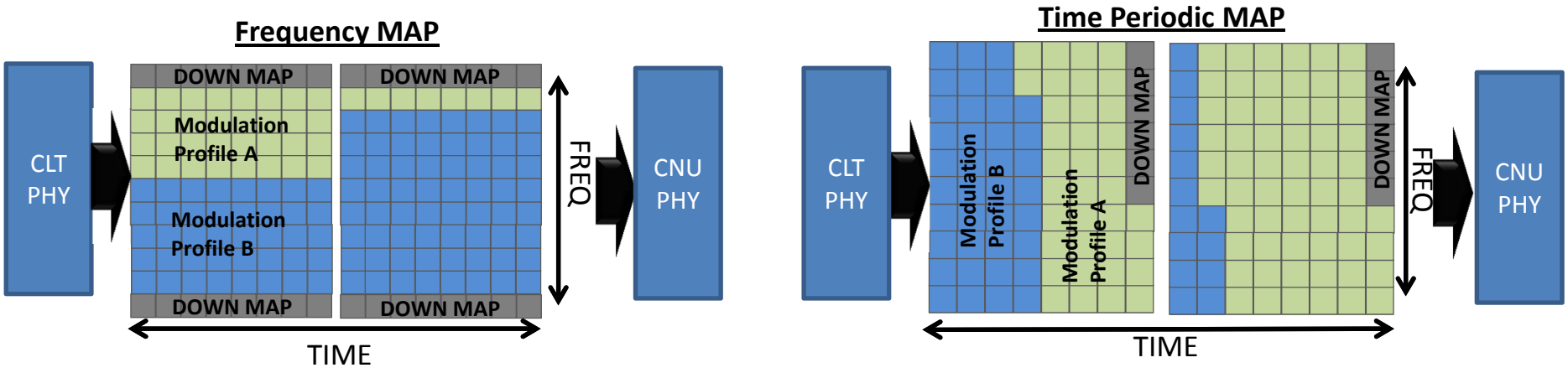
- Downstream Profiles define the bit carrying capacity of the individual sub-carriers.
- Sub-carriers are assumed to have different bit loading capacity for each frequency due to roll off, interference, and frequency attenuation.
- MMP assumes that CNUs on different coax segments will require significantly different profiles. Other presentations discuss this assumption.
- The graph shows 3 profiles for simplicity but 4 profiles are often discussed.
- CNUs would need to support 2 profiles. One for unicast traffic and one for multicast/broadcast traffic.
- Carriers could be shuffled (Frequency Interleaved) to balance out differences (see upstream presentation)

Downstream MAP Options

- Purpose of the MAP
  - CNU RX needs to know modulation order (profile) for each sub-carriers symbols.
  - CNU RX needs to know FEC block start and end.
- Marker Based
  - Fixed pattern at start/end of any profile boundary.
  - Low Modulation order marker followed by block information.
  - Not clear how interleaving or FEC(error correction works).
  - Finding a Marker over poor SNR bad is not reliable.
  - Hard to determine error rate of markers over poor SNR.
- Time Periodic MAP
  - MAP is inserted at fixed period of time.
  - Fixed period of MAP allows for easy recovery from errored MAP.
  - MAP describes upcoming data for receiver.
  - Data block determined and then MAP added to front.
  - Convolutional Symbol Interleaving is possible.
- Frequency MAP
  - Fixed Frequency or sub-carriers carry MAP
  - Provides a block interleaving function.
  - Narrowband interference sensitivity is a concern. Redundant MAP might be required.
  - Block Interleaving is possible.



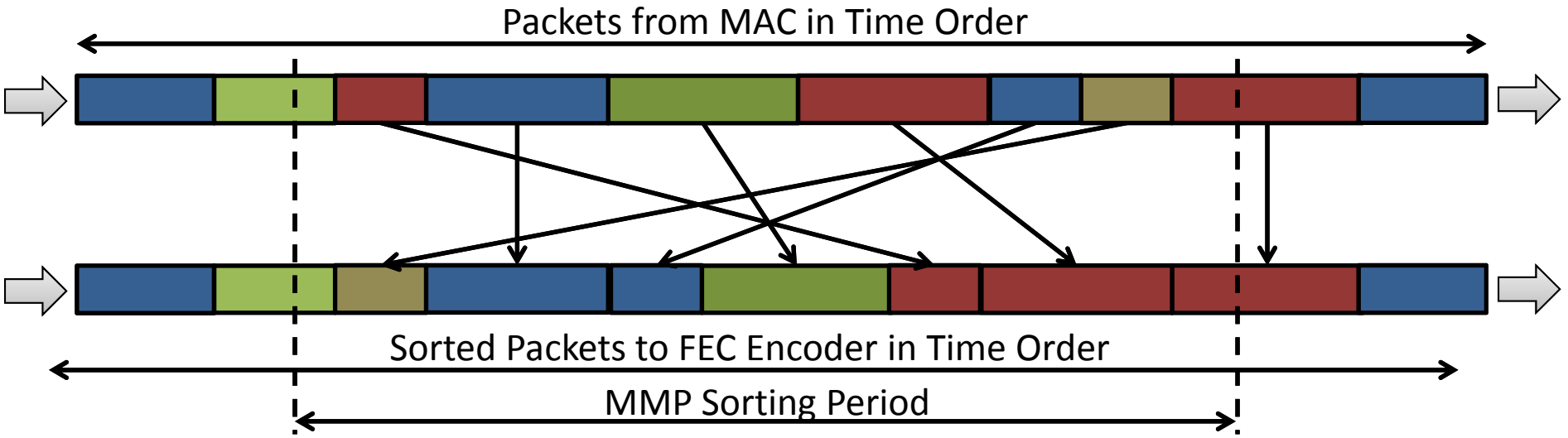
Downstream MAP



- MAP identify the modulation profiles for sub-carriers and symbols
  - Simplest MAP has start and stop carrier for each profile.
  - A more flexible and efficient mapping might require a profile ID for each carrier in each symbol.
- MAP must have equal or better error protection than data.
  - Bit Errors in the MAP will cause the loss of an entire symbol block. (Multiplication of errors).
  - FEC and Interleaver is needed if required in system
  - MAP would use lowest profile or possibly a fixed lower order modulation.
- Protection from narrow band interference is needed
  - Narrowband interference could take down entire downstream in Frequency MAP case.
  - A redundant MAP maybe needed. (Shown in drawing)
- MAPs should be generated and extracted by EPoC PHY.
  - Fixed location to carriers or symbol is only possible at PHY.
  - Not aligned to MAC layer packet boundaries.
  - Contents are from the PHY and to the PHY
  - Block interleaving time and MAP coverage should be aligned.

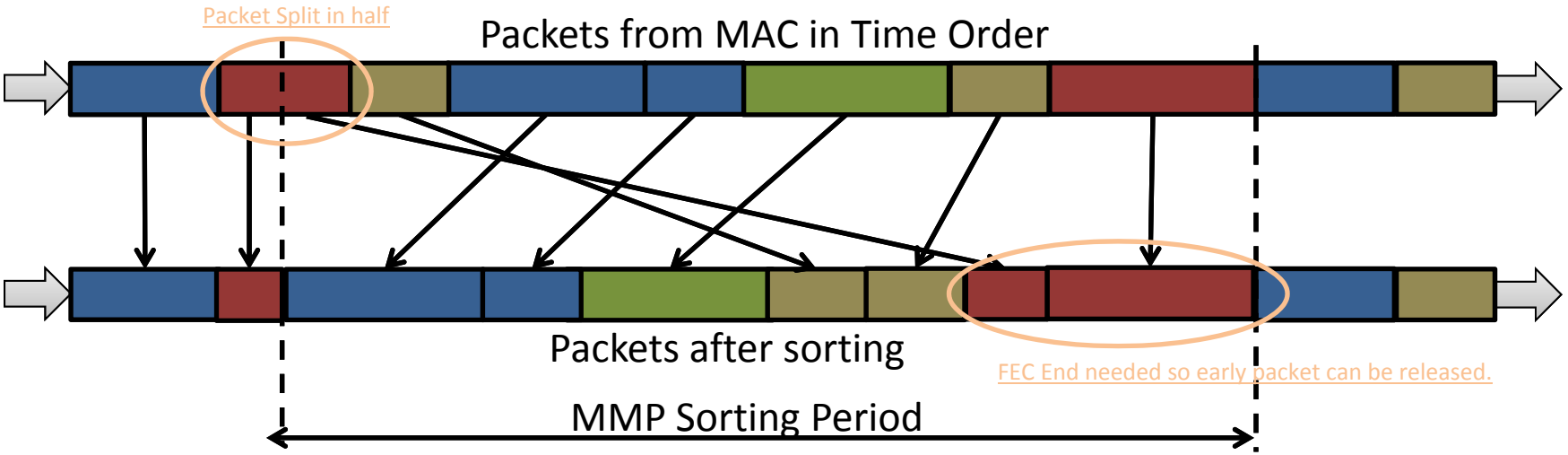
MAP selection needs more analysis but solutions exist

PHY Packet Sorting Overview



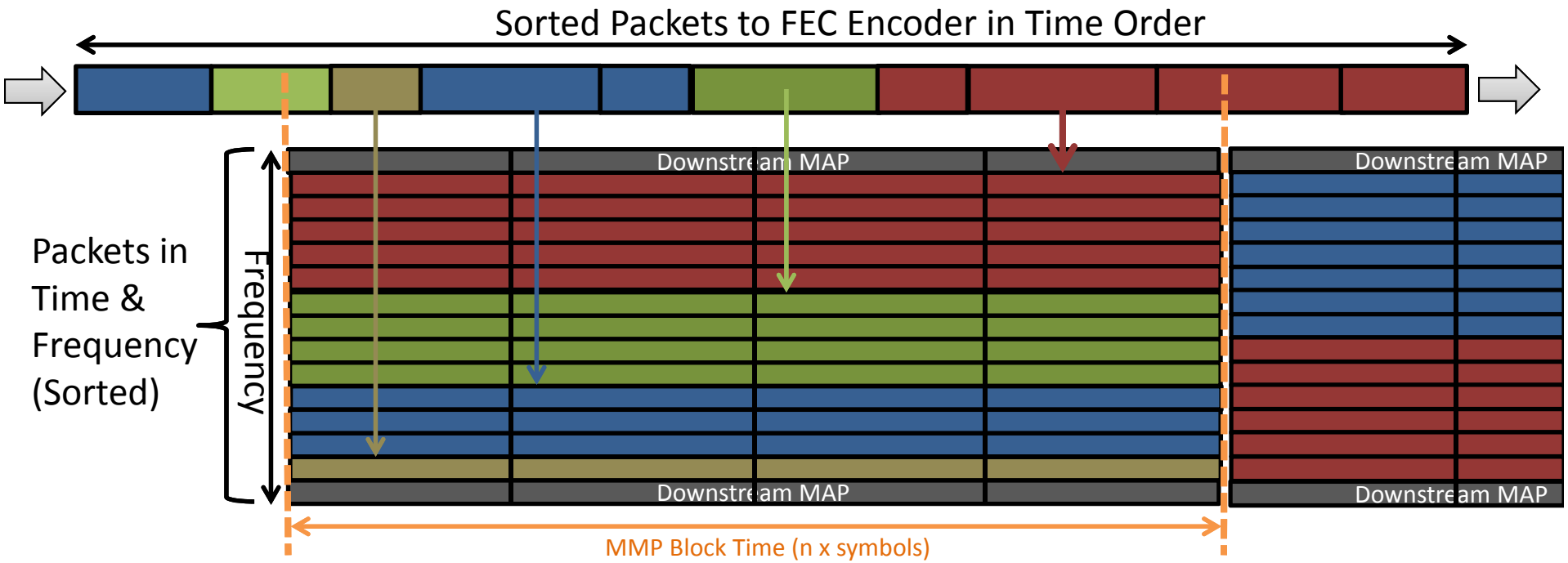
- Packets from the MAC will alternate between destinations for best QoS
- Alternating profiles will decrease efficiency as FEC parity becomes a larger percentage and short less efficient codes are used.
  - Alternating 64 Byte (84 Byte with IPG/Pre) packets.
    - 75% FEC Code: 432b/576b = 58% Efficient (This is not worst case)
- Packets over a fixed period of time are sorted by profile to minimize the FEC overhead of shortened code words.
- PHY Packet Sorting requires buffering packets at the transmitter for the sorting function.
- PHY Packet Sorting requires buffering packets at the receiver for fixed delay to the MAC.

PHY Sorter Boundaries



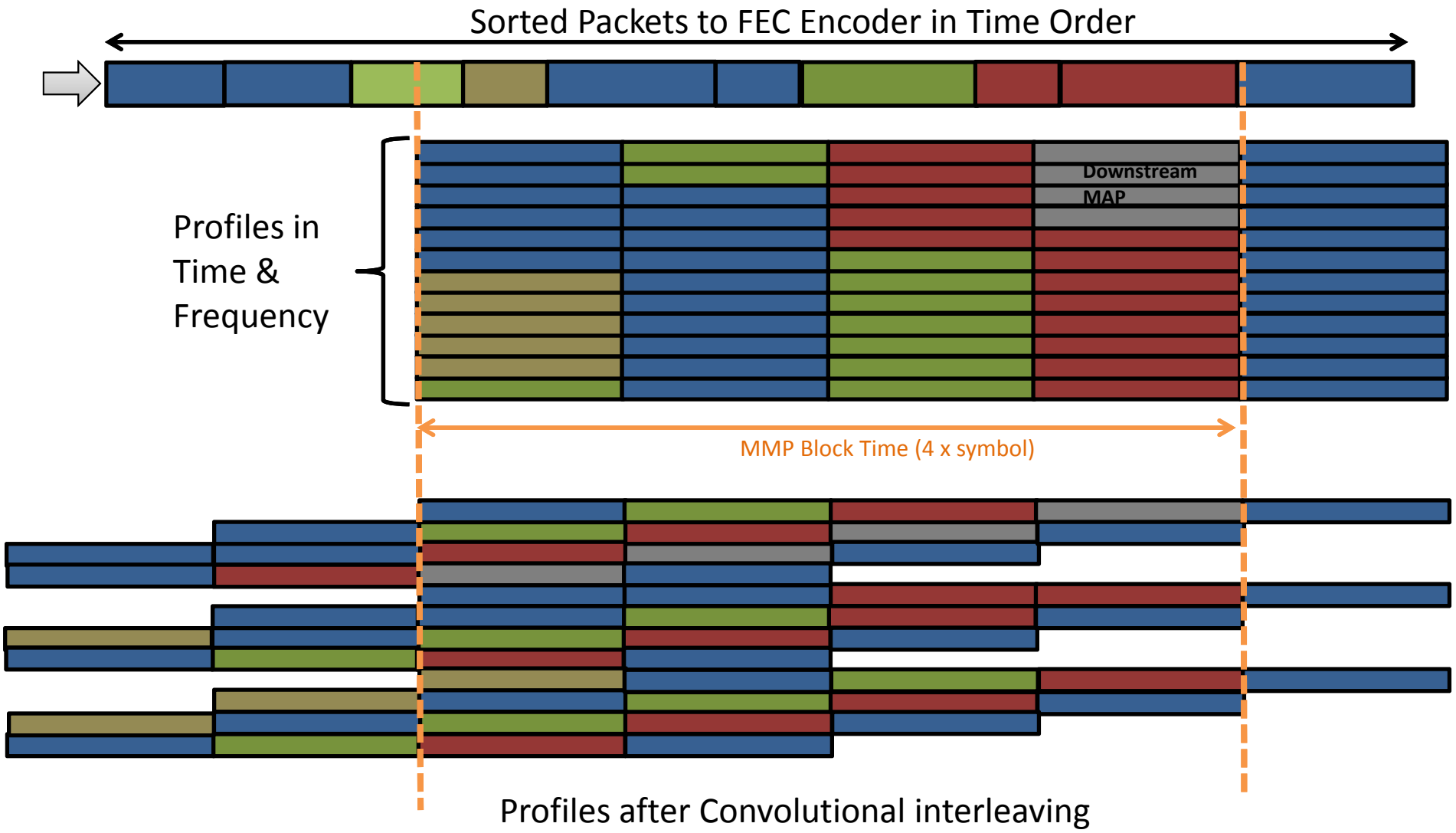
- Packets from the MAC won't align to the sorting period.
- Variable length sorting period wouldn't be aligned to the symbol/interleaver blocks.
  - Extending beyond the symbol/interleaver boundary could cause packet to wait for FEC end and double delay (Jitters)
  - In example above, red profile needs FEC end so first packet is ready to exit in the receiver.
- Fragmentation maybe required at sorting boundaries if period is short
  - e.g. 1000 Avg Byte boundary loss would be 5% loss @1Gbps & 200us
- Fragmentation would split last packet between symbol/interleaver block
- Map or timestamp could indicate fragmented packet.

PHY Packet Sorting After Block Interleaving

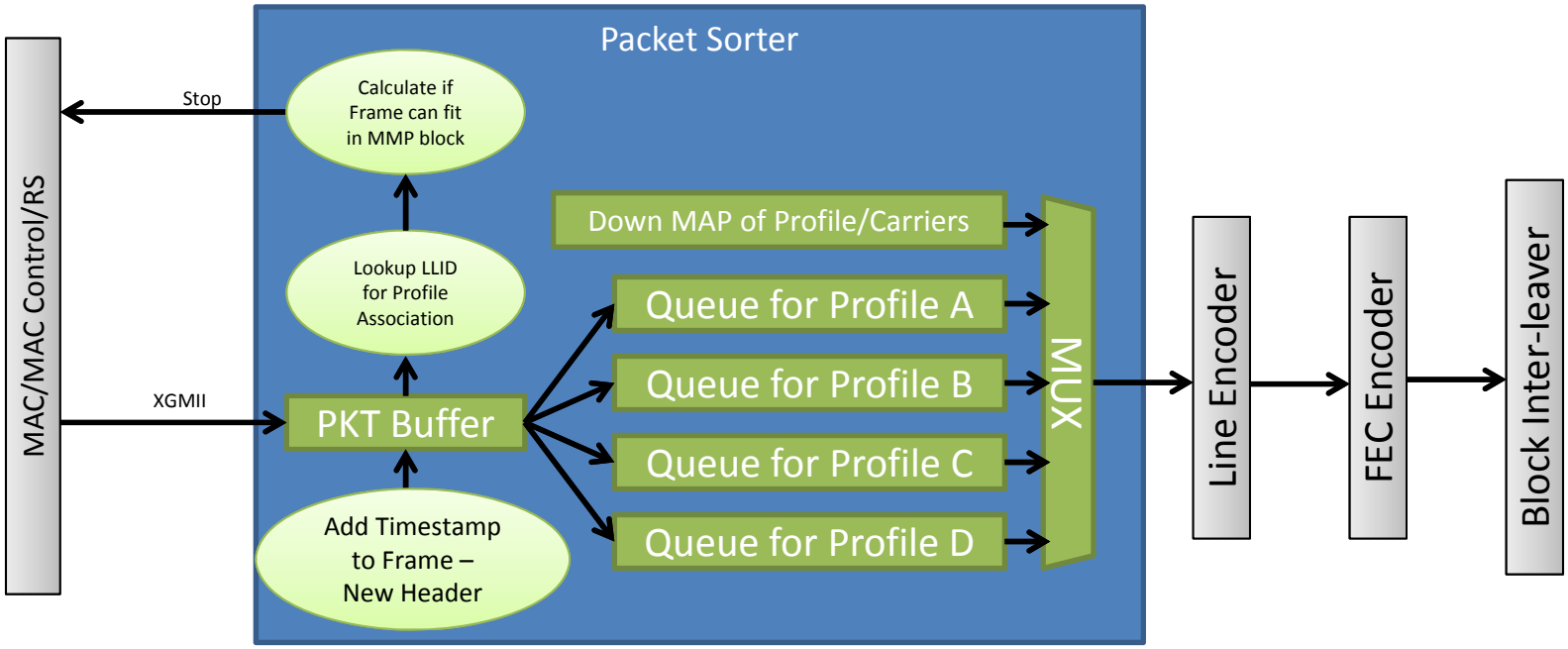


- MAP is added to define the profile boundaries.
- Packets are stretched in time over blocks of carriers.
  - Drawing shows profile grouped carriers for simplicity but it is not required.
- The MMP block time can span one or more symbols.
- The MMP block time could provide a block interleaving function if required.
- Aligning the MAP to the interleaver block allows for the transmitter to generate it last and the receiver to process it first.
- MMP block time, MAP coverage time, and interleaver time should align.

PHY Packet Sorting After Convolutional Interleaving

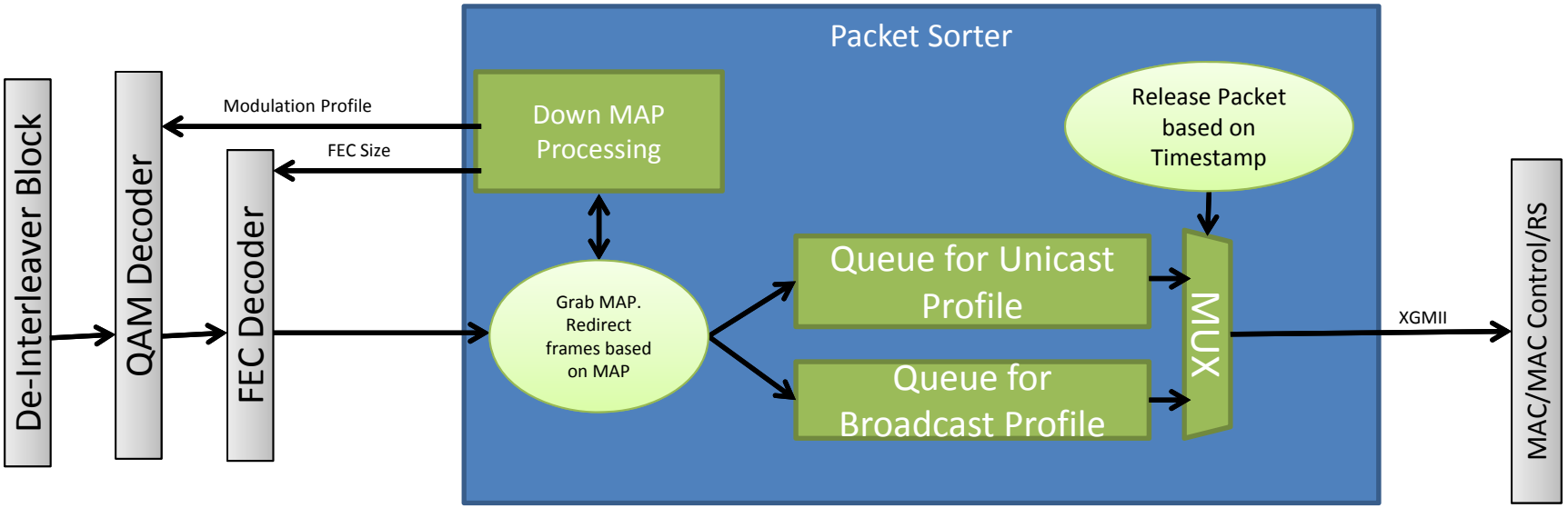


PHY Packet Sorter (CLT PHY TX)



- Packet are queued by profile to fill MMP block time of symbols.
- Packet from XGMII need LLID looked up to find profile association.
- Time Stamp with checksum allows for fixed delay
  - Timestamp could be offset relative to block start.
- Calculations will done to see if frame can fit in the MMP block.
  - FEC Encoding, Profile's bit loading, mapping to frequency
  - Backpressure to MAC is required when sorter has filled block.
- At MMP block interval, MAP is generated and packets are FEC encoded and placed into carriers.

PHY Packet Sorter (CNU PHY RX)

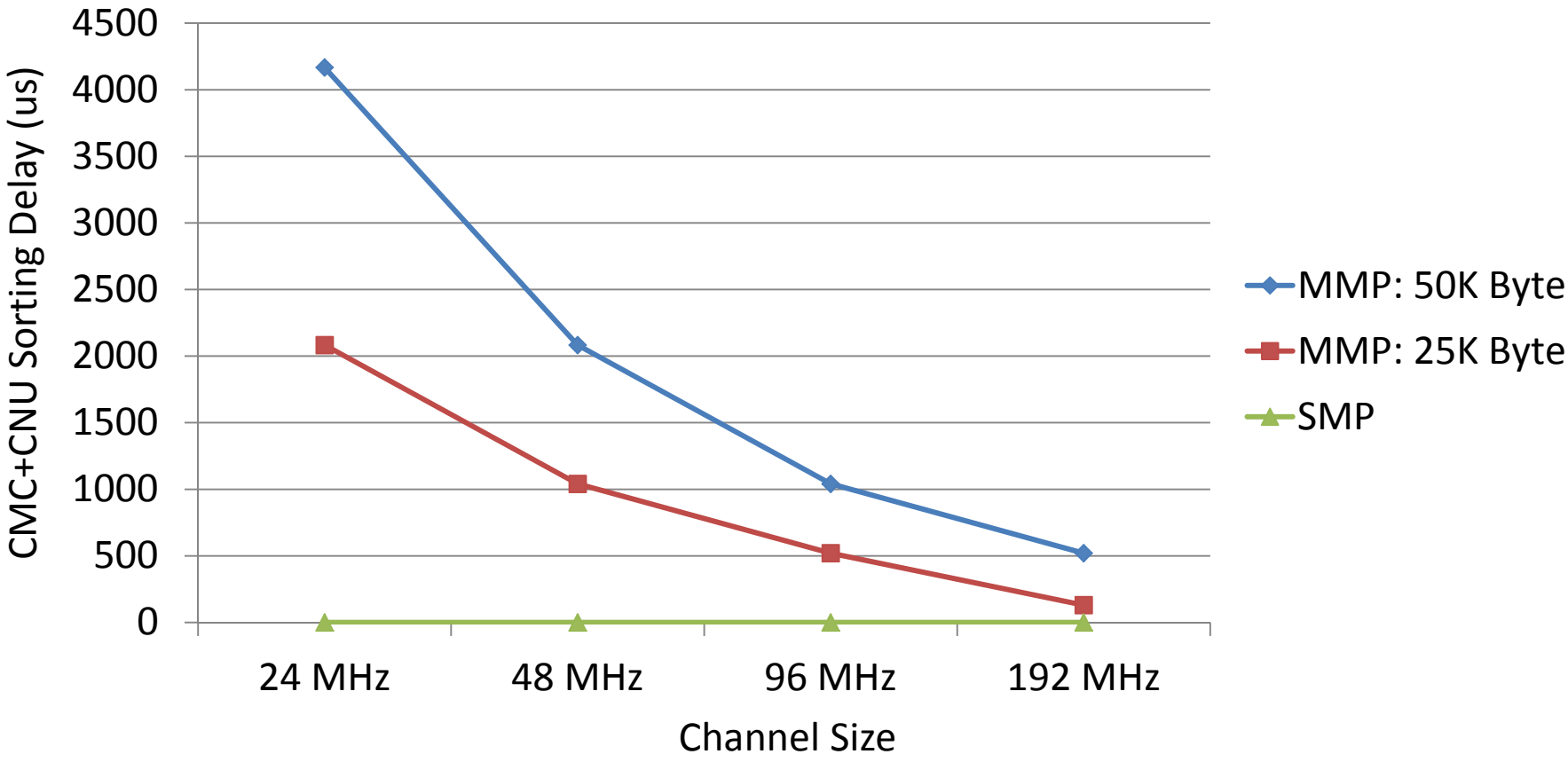


- MAP must be decoded before other MAC layer data is decoded.
- Fixed location, known profile, and known FEC block allow MAP to be decoded.
- From MAP, FEC block size, QAM carrier modulation, and Queue can be determined.
- Only codewords from Profile destined to the receiver are read from the Interleaver and are queued for decoding.
- Decoded Ethernet frames are forwarded to the XGMII by the packet timestamp
  - Since the second frame from decoder could be the last frame to exit, the Packet sorter must buffer for one MMP block time.

PHY Packet Sorter Notes

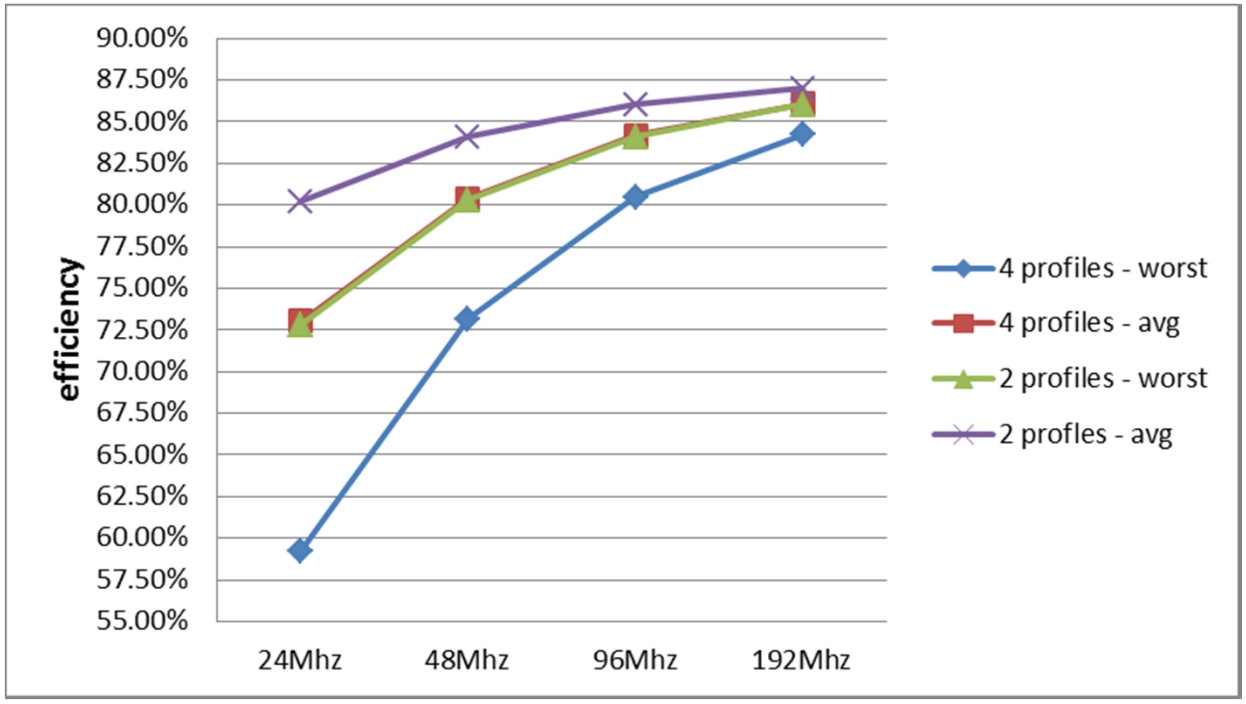
- Profile FEC blocks are also terminated at the end of MMP blocks.
  - FEC block into next MMP block could hold the first packet of the MMP block.
- Minimum MMP block size for Sorting
  - 2xSymbol size (Convolutional)
  - Interleaver delay (Block)
  - MAP coverage and MMP block size should match.
- Large MMP block size will improve efficiency.
  - The 4 possible shortened last codewords per MMP block will be minimized.
  - MAP with it's FEC overhead will minimized.
  - Packet Timestamp Overhead will be minimized
- Large MMP block size will add delay.
  - Double of the MMP block time is required for sorting on TX and unsorting on RX.
- Lower Downstream Data Rates will be less efficient (Delay is fixed).
  - MMP block size must decrease to limit delay.
- Lower Downstream Data Rates will have greater delay (Efficiency is fixed).
  - Fixed MMP block size has longer delay with lower data rate.

PHY Packet Sorting Delay



- 1K Byte of overhead is 4% of 25K Byte block
- 1K Byte of overhead is 2% of 50K Byte block
- Chart assumes 10bits/Hz Line & 8 bits/Hz Payload.

Efficiency with 24,48, 96 and 192Mhz

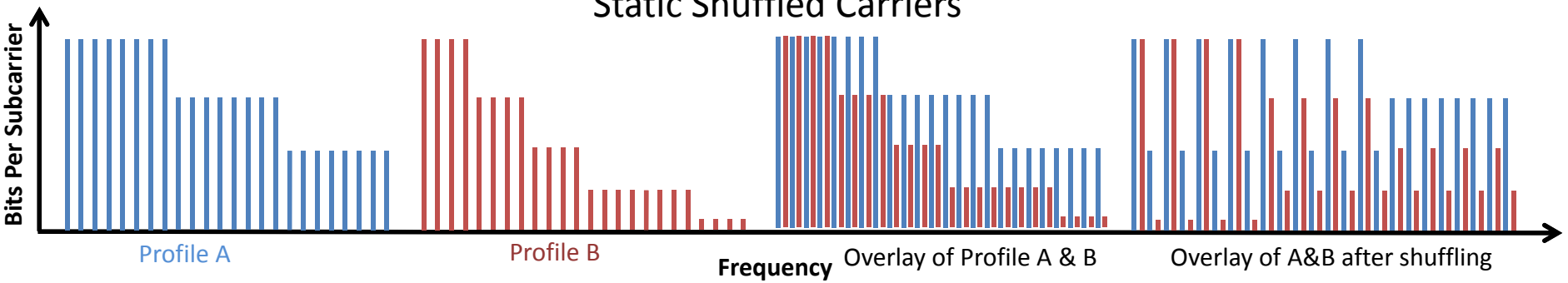


- With Broadcast code rate is 88% with 30 K code in all cases

- frame size 12 symbols (258us)
- Subgroup granularity 32 subcarriers
- Last codewords are Short Codes)

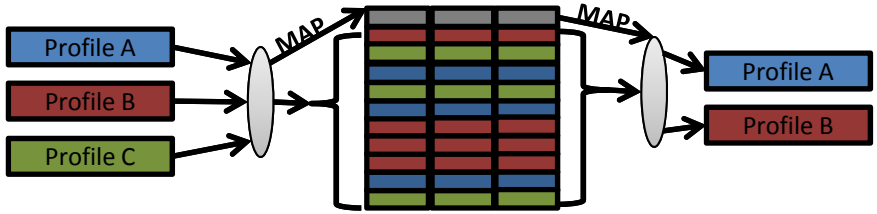
Carrier Selection

Static Shuffled Carriers



- Filling Carriers in order by Frequency will create make the bit capacity uneven for carrier loading.
- Carriers could be loaded/unloaded in a different order so the capacity is balance across the carriers.
- Static configuration based on analysis of profiles.
- Improves efficiency and predictability over straight mapping of MMP.
- More Analysis needed on the ability to align 4 profiles.

Dynamic Shuffled Carriers



- Carrier Mapping is dynamically optimized based on profile and packets in block.
- e.g. In profile above, Profile A packets would use higher frequency since Profile B can't use the carriers.
- MAP frame needs to define the profile association for all carriers. (Longer & more complex MAP frame)
- More complex calculations for determining if a packet fits and optimization.
- Better Efficiency than Shuffled Carriers but less predictable data rate.

Delay Impacts

- REPORT frame limited to 1ms of total upstream + downstream PHY delay.
  - With small Convolutional Upstream and SMP, EPoC is at 1ms limit for sum of PHY TX and RX path.
  - Additional delay requires new REPORT frame.
  - No compatibility with 1G or 10G EPON systems or devices.
- Upstream Buffering Increases on Low Priority Services
  - 1.2ms additional delay is an extra 150KB for 1Gbps upstream queue.
- Upstream efficiency is lowered on High Priority Services
  - Increasing polling rate will cost upstream efficiency
    - 1ms Polling BW Required: (128 LLIDs*2500 bits)/1ms = 320Mbps
    - 2ms Polling BW Required: (128 LLIDs*2500 bits)/2ms = 160Mbps
    - 3ms Polling BW Required: (128 LLIDs*2500 bits)/3ms = 107Mbps
    - 4ms Polling BW Required: (128 LLIDs*2500 bits)/4ms = 80Mbps
  - Polling bandwidth required is independent of upstream data rate.
    - Polling is very significant percentage for sub-1Gbps upstream.
    - EPON has 250us PHY delay so EPoC at 1ms PHY delay is already 4 times.

Increasing the delay beyond 1ms is not a good solution for EPoC

To interleave or not to interleave?

- Using Long Symbols instead of interleaving
  - Long symbols would reduce the sensitivity to burst noise.
  - Long symbols reduce CP overhead.
  - Short symbols with interleaving are more robust to burst noise.
- Delay Comparison
  - MMP requires sorting with or without interleaving
    - Sorting allows for a bounded limit on shortened FEC blocks.
  - Short Symbol Delay (without sorting delay)
    - 4xSymbol Size + Interleaving-Delay
    - e.g. 4x20us+400us=480us
  - Long Symbol Delay (without sorting delay)
    - 4xSymbol Size
    - e.g. 4x120us=480us
- Key Points
  - Sorting and MAP generation adds delay for MMP independent of interleaving
  - Interleaving or long symbols is an independent decision based on channel model.
  - TDD must use block interleaver but FDD can use block or convolutional interleaver.

MMP Implications

	Single Profile (SMP)	Multiple Profile (MMP)
Sorting Memory [8Gbps & 400us MMP block time]	0	800KB (½ CMC & ½ CNU)
Delay for Sorting (For CMC & CNU each)	0	Up to 4ms
Delay for Interleaving (Estimate – FEC decision needed)	400us (Convolutional)	400us (Convolutional) 800us (Block)
Downstream MAP	No	Yes
Profile Configurations for 4K or 16K carriers	1	4
LLID to Profile Lookup	No	Yes
New XGMII Interface (Variable Data Rate)	No	Yes
Packet Sorting	No	Yes
Carrier (Static or Dynamic) Shuffling	No	Yes
Packet Timestamp Header	No	Yes
Fragmentation	No	Yes
Shortened FEC and/or Multiple FEC Sizes	No	Yes
New REPORT & GATE frame	No	Yes

Conclusions

- MMP could be designed to be error tolerant with proper MAP methodology.
- MMP adds significant complexity, cost, and delay to the downstream.
  - Additional downstream delay impacts upstream efficiency.
- EPoC is EPON-over-Coax and should support allow 1G & 10G EPON devices and systems to work with the new EPoC PHY.
  - MMP will require a new interface and new REPORT/GATE frames.
  - Violates the objective of 1G EPON/10G EPON compatibility.
- Upper layers expect constant delay/rate from Ethernet MAC and PHY.
  - 1588, 802.1AS, Y.1731 are examples.
  - Provisioning/Operations are simpler without data capacity dependence based on frame size or frame destination.
- Longer FEC codes, Inner/Outer Codes, etc should be considered to increase efficiency.
- DOCSIS 3.1 can have options for SMP or MMP downstream but Ethernet should be simple.

Multiple Modulation Profiles doesn't make sense for EPoC