# DOWNSTREAM BASELINE PROPOSAL

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# SUPPORTERS

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# INTRODUCTION

- **We laubach_3bn_04_1113.docx (also as .pdf) for consideration as Baseline Proposal for the P802.3bn downstream.**

- **This contribution follows the spirit expressed at the York interim meeting of submitting elements for P802.3bn technical consideration from the DOCSIS 3.1 PHY with a goal to enable "common component architecture" in the industry:**
  - Downstream PHY data and PLC (portions of Section 7.5)
    - Note: some elements are shared with the D3.1 upstream PHY, those text subsections have been rolled into this baseline proposal for completeness
  - Downstream NCP (Section 8.3)
  - Only FDD mode is detailed at this time

- **Past P802.3bn Task Force decisions are represented in this baseline proposal**
  - One difference will be a proposal for changing the existing PLC Next Codeword Pointer (NCP) method to a different NCP approach

# OVERVIEW OF DIFFERENCES AND T.B.D.'S

- **Downstream PHY functional diagram as presented in** kliger_3bn_01_1113.vsd

- **Downstream line encoding and LDPC FEC**
  - Already in PCS work in progress in the Task Force

- **Scrambler / Randomizer and Frequency Interleaver**
  - T.B.D. next meeting pending coordination with individuals from other affiliations

- **Symbol Mapper**
  - Constellations as per prodan_3bn_02_1113.pdf to align with EPoC LDPC FEC decisions

- **Downstream Profiles**
  - Reduced to single profile for FDD

- **Windowing adds extra value as per** montreuil_01a_0113.pdf

- **Fidelity and Electrical requirements in progress by another proposal effort:** rahman_saif_3bn_01_1113.pdf

- **Proposal to use a new NCP architecture**
  - Moves data codeword processing within the demodulation processing pipeline of the system
  - Separation from PLC content
    - PLC remains as providing the configuration of "where/how to (de)modulate" and for downstream frame alignment, time stamp, etc.
  - EPoC FDD will use a single profile; i.e., Profile A
    - All other Profile ID values, as well as update functions will be reserved
    - NCP fields remains for alignment to "common component architecture"
  - Adds FEC and 24-bit CRC (to PMA)
    - Note: shares LDPC mother code with Initial Ranging

- **PLC channel structure details**
  - Preamble updated as per montreuil_3bn_01_0713.pdf
  - PLC FEC as per shen_3bn_01_0713.pdf
    - Note: shares LDPC mother code with Fine Ranging
  - PHY coding only and spectrum details.
    - No PLC content in this baseline proposal,

- **Move to the following NCP architecture:**
  - NCP located in data sub-carriers
  - Processed by data channel processing pipe-line
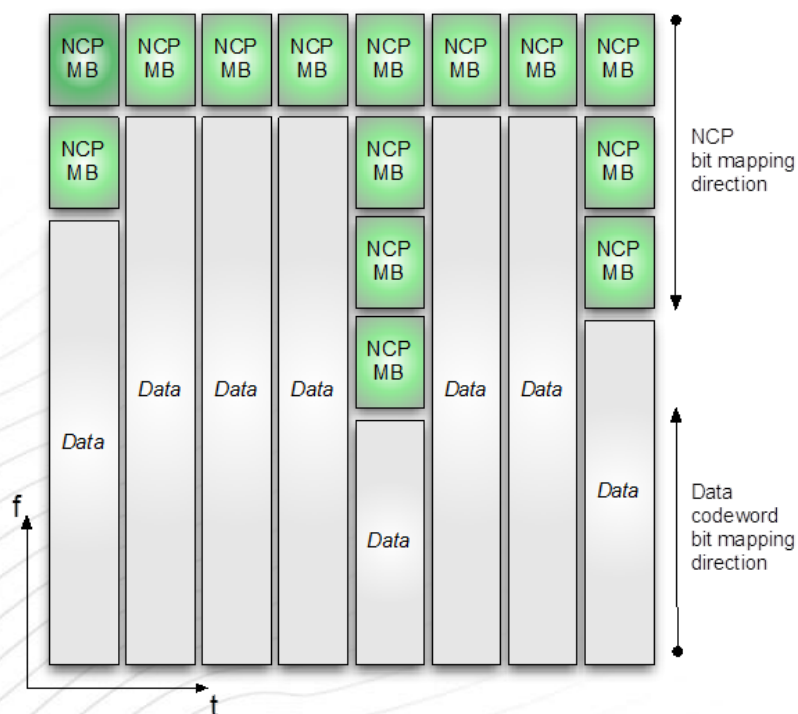  - NCP blocks start from "top down"
  - User data codewords from "bottom up"



*Figure 2–7 - Data and NCP Prior to Interleaving*

# NCP MESSAGE BLOCK STRUCTURE

- **NCP Message Block (MB) has two parts:**
  - 24-bit flag and pointer fields
  - 24-bit CRC

- **Each 24-bit sub-block is protected by an LDPC (48, 24) FEC**
  - Shares LDPC mother code with proposed upstream ranging FEC. See shen_3bn_01_1113.pdf
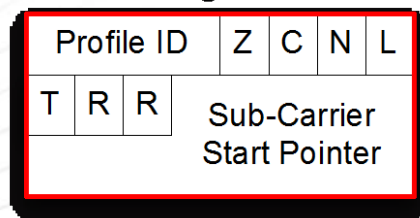
**Next Codeword Ptr (NCP)**
**Message Block**

| Profile ID | | Z | C | N | L |
|---|---|---|---|---|---|
| T | R | R | Sub-Carrier Start Pointer | | |

*Figure 2–8 - NCP Message Block*

# NCP MB FIELD DETAILS FOR EPOC

- **Profile ID – <u>Only value "0" Profile A</u> to support a single FDD profile, other values reserved**

- **Data Profile Update C-bit – set to "0", other value reserved**

- **Use of Z, N, T, and R fields for further study.**

| Field | Size | Description |
|---|---|---|
| Profile ID | 4 bits | Profile ID for the data channel<br><br>0 = Profile A        1 -15 = reserved |
| Z | 1 bit | Zero Bit Loading<br><br>0 = subcarriers follow profile    1 = subcarriers are all zero-bit-loaded |
| C | 1 bit | Data Profile Update<br><br>0 = set to 0      1 = reserved |
| N | 1 bit | NCP Update<br><br>0 = use even profile      1 = use odd profile<br><br>This bit is equal to the LSB of the NCP profile change count. This bit refers to the NCP profile usage for the next symbol rather than the current symbol. |
| L | 1 bit | Last NCP Block<br><br>0 = This NCP is followed by another NCP.<br>1 = This is the last NCP in the chain and is followed by a CRC. |
| T | 1 bit | Directed Test<br><br>0 = this codeword is not suitable for directed profile testing by CNUs<br><br>1 = this codeword is suitable for directed profile testing by CNUs |
| R | 1 bit | Reserved |
| Subcarrier pointer | 13 bits | This is the number assigned to the first subcarrier used by the codeword. The maximum value is 0x1FFE = 8190. The value 0x1FFF is reserved as a null pointer. |

# NCP PROPOSAL SUMMARY

- **Codeword alignment completely in data channel processing**
  - **Separation from PLC content**
  - **NCP Message Block is a PMA -> peer PMA  protocol element**
- **Supports TDD requirement for multiple profiles (TD #19) – if needed**
- **Lays groundwork for future proofing**
- **Aligns "common component architecture" element with D3.1 PHY**

Example:

- NCP moves as part of Symbol Mapper.  See kliger_3bn_02b_1113.vsd.
  - Calculates Subcarrier Pointer, L field, CRC-24, and NCP FECs
- Appropriate NCP flags/fields passed with codeword request and indication

**NOTE:**

- **Future work can investigate reducing overhead for FDD operation**

# NCP APPROACH COMPARISON

**[New Slide]**

- **NCP in the PLC**
  - Appears once every PLC frame (2.5-5 mSec)
  - Points to the next codeword in next frame
  - Low overhead
  - Doesn't affect data throughput

- **NCP in the Data path**
  - A pointer per CW
  - No layer mixing: Part of the data path, and interleave with data
    - Processing tight to data – simpler implementation
  - Fast recovery in case of symbol sync loss
  - "Common component architecture" with DOCSIS3.1
  - Overhead of 1% with 192 MHz
  - Fixed averaged overhead over a number of CWs.
  - Provides flags for future use:
    - Zero Bit Loading, Directed Test, Profile Update/Change

**[New Slide]**

| CW pointer carried by | PLC | NCP |
|---|---|---|
| Overhead | ~0 | 1% |
| Runs the data path (no layer mixing) | no | yes |
| Recovery time (uSec) | 2800 | 22 |
| Common Architecture | no | yes |
| Fixed data rate | yes | yes |
| Trigger to profile switching | no | yes |

- **The attached baseline proposal contains functional descriptions for aspects of the downstream EPoC PHY and an NCP update proposal**
  - Uses past P802.3bn technical decisions
  - Leverages "common component architecture" where possible
  - Includes detailed NCP description that is a change from previous technical decision
    - Asking that the TF adopt this proposed NCP approach
    - Can look at efficiency improvements going forward
  - Ongoing updates and modifications via the comment process and/or other proposals
  - Informational text and stylistic differences can be "expunged" and/or copy-edited by the Editors, different subsections will move to different IEEE normalized sections.

# PROPOSED MOTION

- **Adopt laubach_3bn_04b_1113.docx as a starting point for the downstream baseline for P802.3bn downstream PHY.**
  - NOTE: PLC (sections 1.2.12.x) removed: will be in the PLC baseline proposal

- **Moved:  Avi Kliger**
- **Second: Richard Prodan**

# Thank you