EPoC Scrambler

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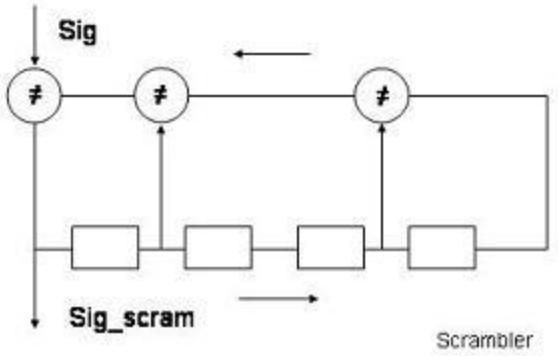
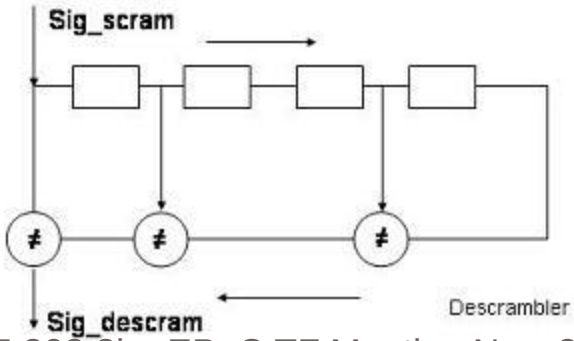
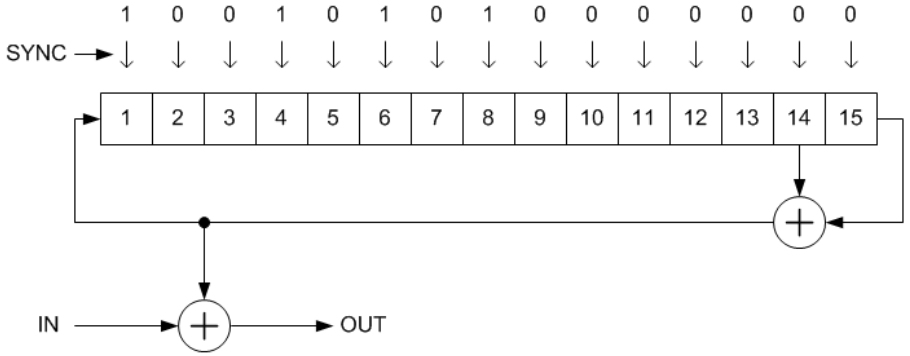
Scrambler Overview

- Multiplicative (self-synchronizing) scrambler





- Additive (synchronous) scrambler



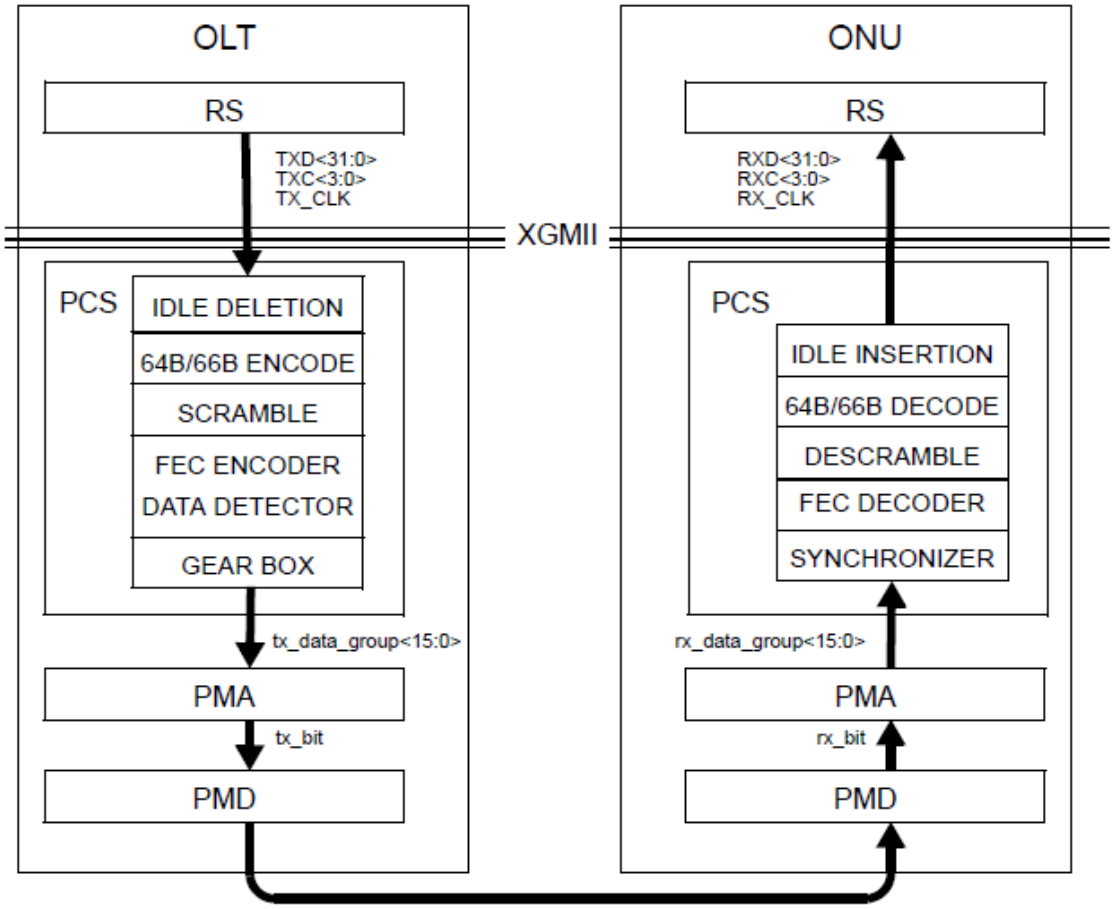
Scrambler Overview

- Self-synchronizing scrambler
  - No need to load the same seed at the receiver
  - Usually at the Tx before FEC, because it will propagate one error into several errors.
  - Can be very long, better randomization and DC balance. For example, in EPON, $g(x) = x^{58}+x^{39}+1$.
  - Data bit loss during synchronization.
- Synchronous scrambler
  - Set/reset seed to synchronize the state at certain point.
  - The effective length of the random sequence of an additive scrambler is limited by the frame length, which is normally much shorter than the period of the PRBS

Requirement of Scrambler for EPoC

- OFDM system does not have DC wander.
- Long runs of zeros and ones cause many carriers to map to same symbol in the constellation, then generate peaks after inverse FFT.
- PAPR or clipping rate in PMD output.

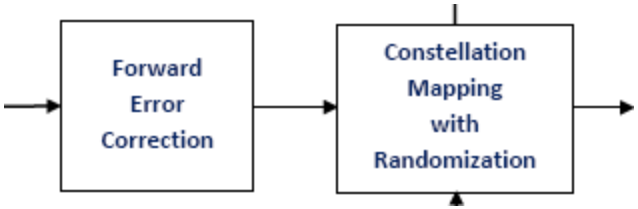
EPON Scrambler



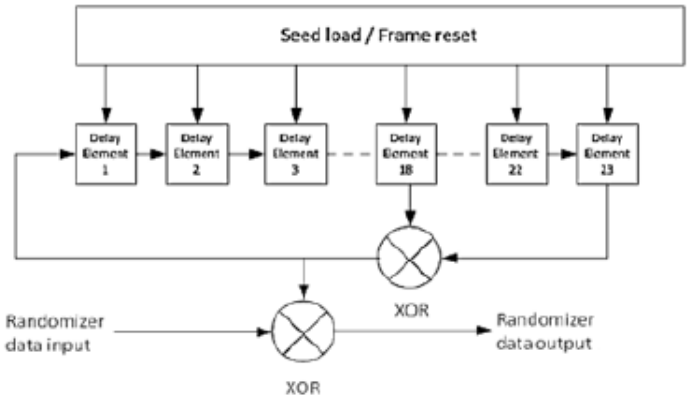
$g(x) = x^{58}+x^{39}+1$

DOCSIS 3.1 DS Randomizer

- Randomize the cell words before constellation mapping to symbols and after the FEC.
- GF(2^{12}) g(x) = $x^2+x+\alpha^{11}$. Equivalent period 2^24-1
- Synchronize to the PLC frame, 128 OFDM symbols.



DOCSIS 3.1 US Randomizer



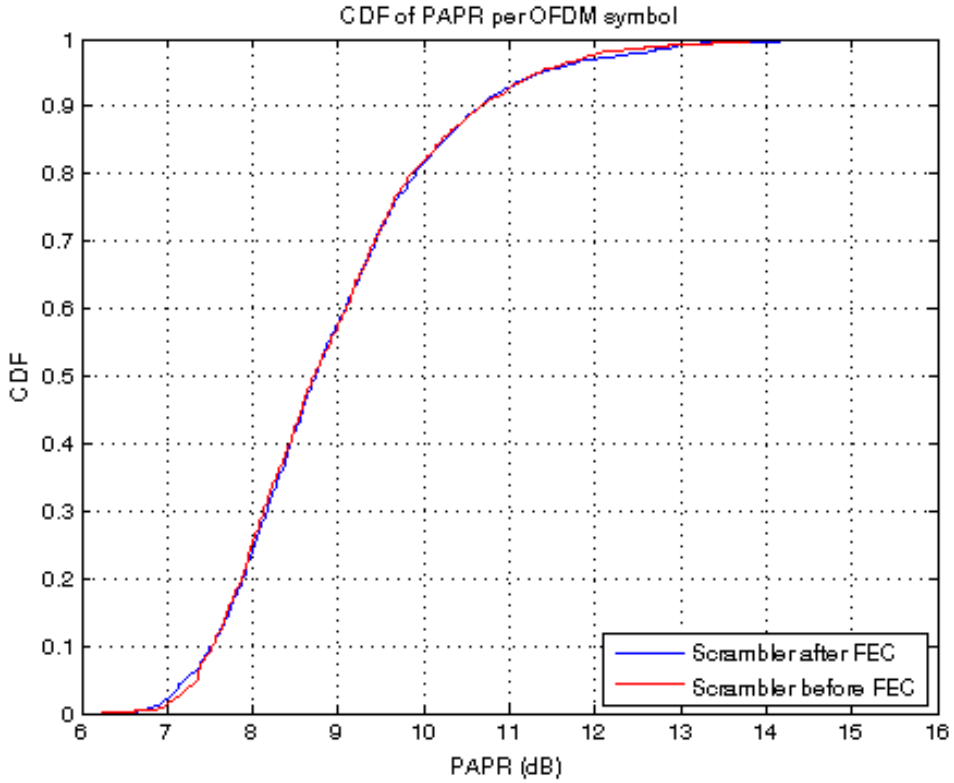
- After the FEC encoder.
- g(x)=x^23+x^18+1, period 2^23-1
- Synchronize to each burst
- Need to use MAC message to assign the seed.

Scrambler and FEC

- Usually scrambler is before FEC encoder.
  - Less error propagation for self-synchronizing scrambler
  - The parity of FEC is DC balanced, is usually not scrambled.
  - The interleaver after FEC could play a further role of randomization and reduce the PAPR.
- LDPC has long sets of parity bits, does it need to be scrambled?

Simulation

- 4096 FFT, 3840 subcarriers, 1024QAM, LDPC (16200, 14400)



Consideration of Scrambler

- Little difference on PAPR as to scramble or not to scramble the parity of the LDPC codeword.
- Time and frequency interleaver can further randomize the parity bit.
- Complexity wise:
  - Self-synchronizing scrambler, e.g. EPON scrambler, is simpler, stream based processing, no message exchange, no jitter, no uncertainty in latency.
  - Synchronous scrambler, e.g. DOCSIS 3.1 randomizer: need set/reset seed, message for exchange of seed, block based processing, latency is implementation dependent.

Decisions to Make

- 1. DS and US both use self-synchronizing scrambler
- 2. DS uses self-synchronizing scrambler, US uses synchronous scrambler. The location of synchronous scrambler is after the FEC.
- 3. DS and US both use synchronous scrambler. The location of synchronous scrambler is after the FEC