EPON Protocol over Coax

Data Detector for TDD Downstream

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Abstract

- In the upstream there needs to be a data detector for the burst mode PHY
  - For both FDD and TDD
- Since the TDD downstream will also use the burst mode PHY there also needs to be a data detector in the TDD downstream
  - Data detector in the PCS needs to identify the downstream and upstream windows and provide signal to PMA for switching between TX/RX
- This presentation provides a proposal for the TDD downstream data detector

TDD Cycle Technical Decisions

- In July the Task Force made two technical decisions regarding the TDD Cycle

Number	Technical Decision
83	The standard shall support a TDD Guard Time in positive integer multiples of 1.25 µs, starting at 1.25 µs to at least 10 µs
84	The TDD downstream and upstream time windows will be characterized by an integer multiple of the symbol duration, which is equal to the inverse of the sub-carrier spacing plus the cyclic prefix duration

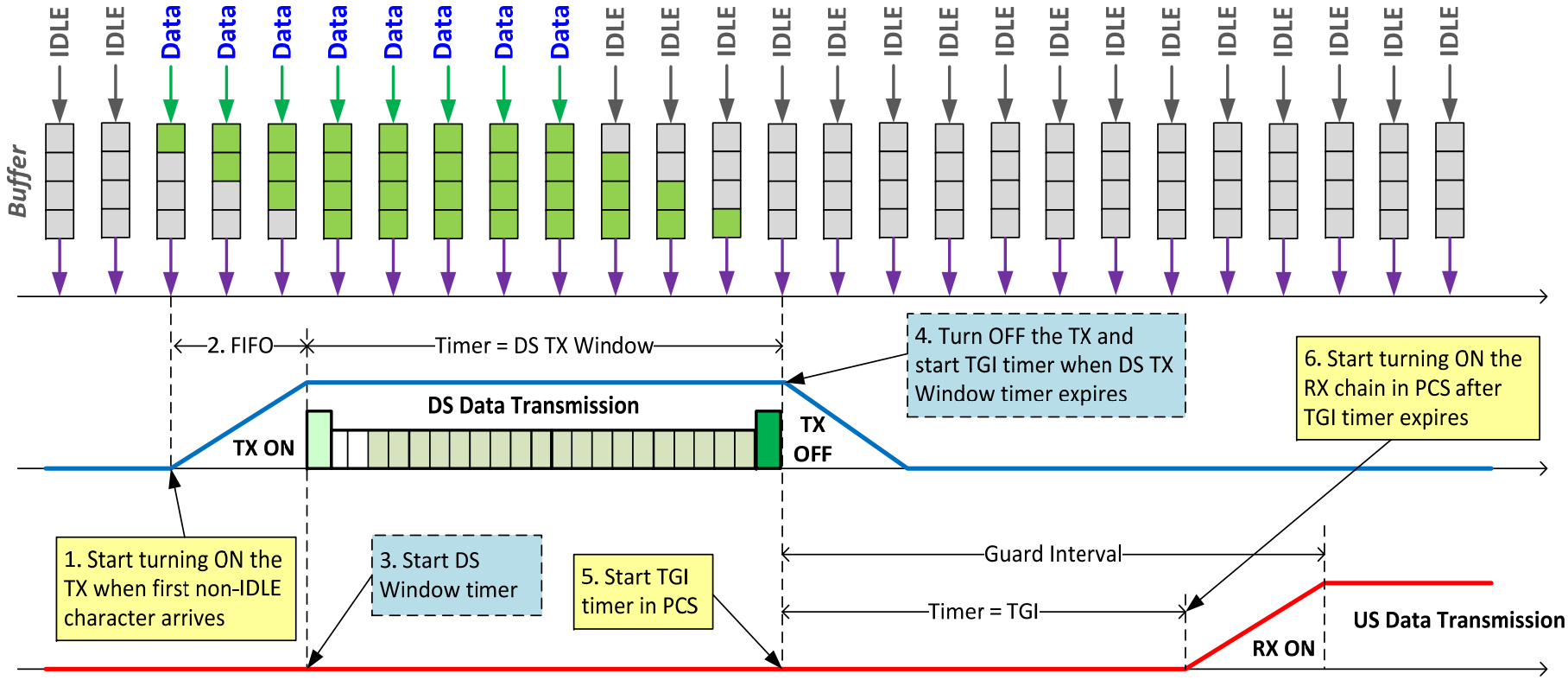
Downstream Transmission

- In TDD mode, the downstream transmission remains "ON" during the full downstream time window [2]
- This provides several benefits
  - It enables the CNU to receive the downstream PLC even when there is no MAC data to send. This makes it possible for new CNUs to join the network
  - All CNUs can continue the PHY-layer time and frequency synchronization loops during the downstream time window
- Several methods were considered for triggering the downstream time window [2]
- The preferred method for triggering the downstream time window is reception of a non-Idle character [3]
  - Same principle as in EPON for burst transmission

Functions of the TDD DS Data Detector

1. Upon detection of a non-Idle character *TX_ON* is set to True
2. Provide necessary delay between *TX_ON* and physical transmission on the medium
   - This is the same as the FIFO delay in EPON
   - This delay may end up being the same as the delay on the upstream (PHY issue common to FDD and TDD)
3. Maintain downstream transmission during the TDD downstream time window
4. Set *TX_ON* to False and cease downstream transmission during TDD guard times and upstream transmission window
5. Keep all RF off during guard interval time
6. After guard time is elapsed, set *RX_ON* to True for upstream operations in the CLT during upstream transmission window

TDD DS Data Detector – Overview



Data detector to command *TX_ON* at the CLT – TX ends with configured delay after TX gets ON (DS TX Window, configured) and then RX starts with configured delay after the transmitter is OFF (TDD Guard interval, configured)

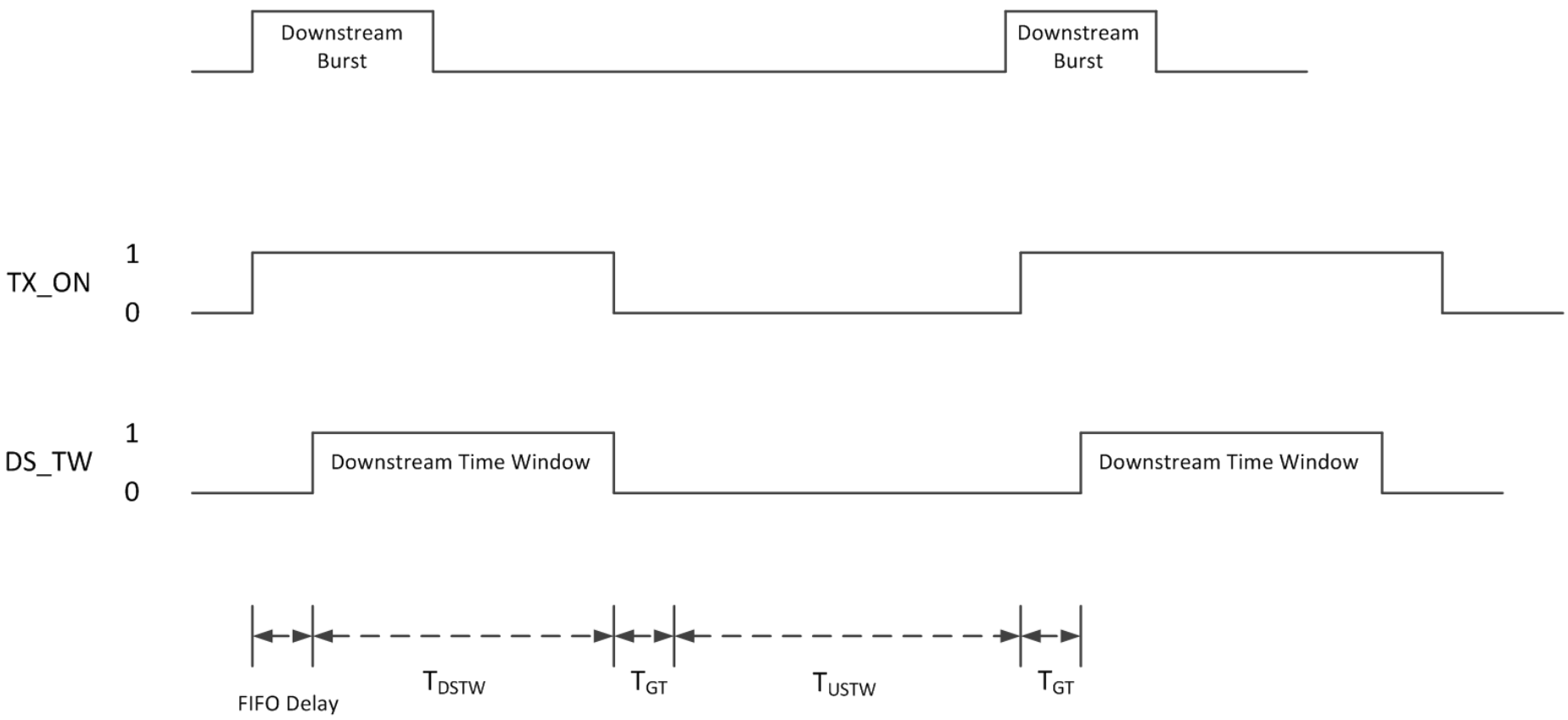
TDD Downstream Burst [3]

- The MAC will ensure that a burst is sent to begin the downstream time window
- If no data is available to be sent a GATE message with no grant is sent to ensure beginning the downstream time window
  - As done in 10G-EPON for synchronization (see Clause 77.3.6.1, first paragraph)

Timing Diagram – Parameters

Timing Parameter	Description
FIFO Delay	Necessary delay from the beginning of a burst arriving at the PCS until an OFDM symbol begins transmission on the medium. Possibly the same delay as in the upstream.
T_{DSTW}	Duration of downstream time window. Configurable parameter. An integer multiple of the OFDM symbol duration, including CP (Technical Decision 84)
T_{GT}	Duration of guard time. Configurable parameter. Integer multiple of 1.25 µs. (Technical Decision 83)
T_{USTW}	Duration of upstream time window. Configurable parameter. An integer multiple of the OFDM symbol duration, including CP (Technical Decision 84)

Timing Diagram – Parameters (cont.)

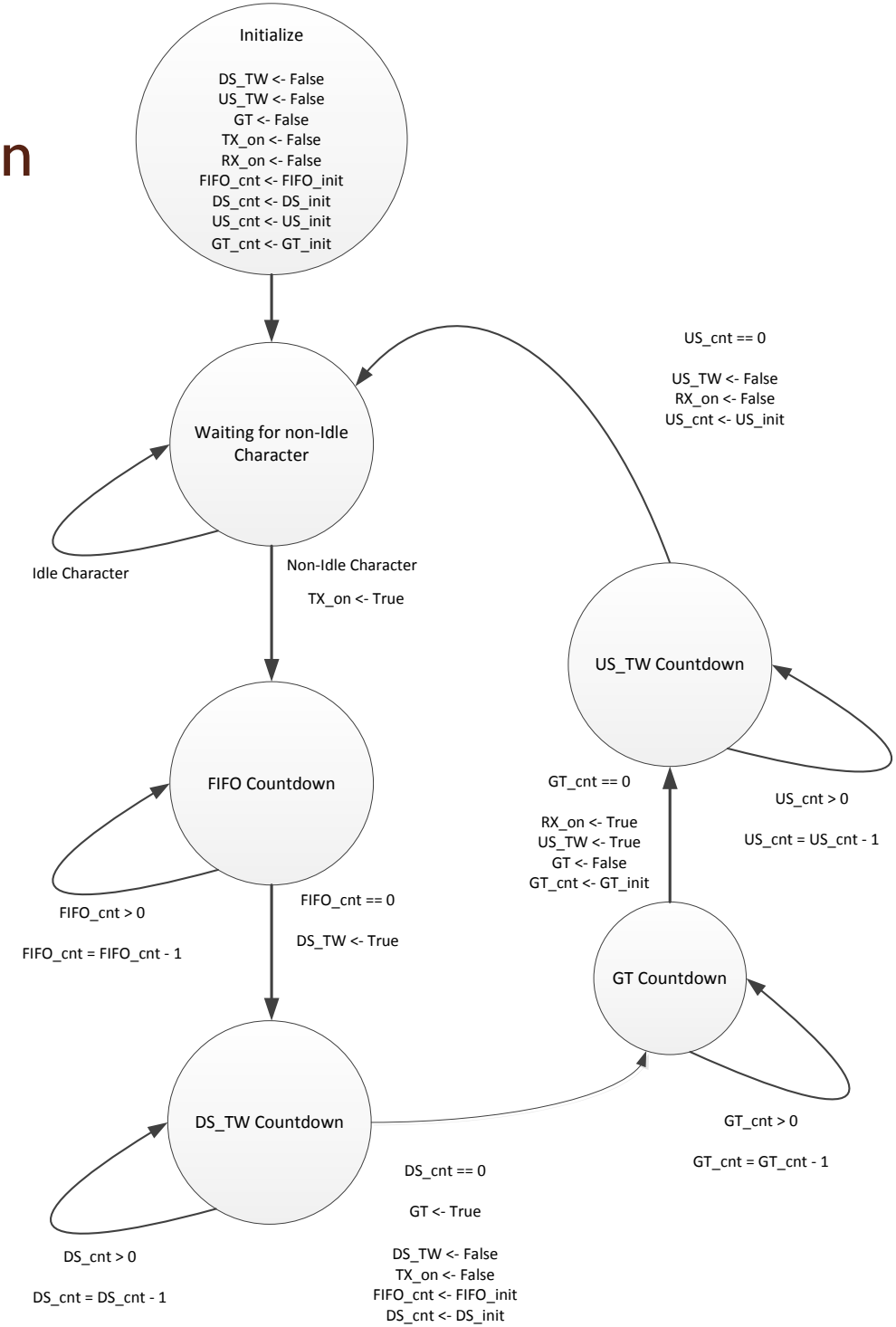


Timers

- The FIFO delay can be measured in XGMII characters (like in EPON)
  - This is similar to the upstream burst mode
- The downstream time window, the guard time interval and the upstream time window can measured using a countdown counter that is clocked with the PHY clock
  - These values are configured via MDIO

State Diagram: Illustration Purposes Only

- The following state diagram is designed to explain the operation
- The final state diagram will be based on updates of the EPON state diagrams [2] (Figures 76-16 and 76-17b in the 802.3 Standard)



Jitter

- The PCS receives characters according to the XGMII clock of 312.5 MHz
  - 156.25 MHz Double Data Rate (DDR)
- The PHY operates using a 204.8 MHz clock
  - Multiple of 10.24 MHz (Technical Decision 7)
- Implementations that use the XGMII interface could have some jitter in the TDD cycle repetition
  - Since the period of the XGMII clock is 3.2 ns, jitter due to the difference in XGMII and PHY clocks should be small
- There is also a jitter budget which in EPON is for the combination of the MAC and the PHY. This could result in some jitter in when the first non-Idle character is seen at the PHY interface [4]

Straw Poll

- Do you support this as a starting point for a baseline for the TDD downstream data detector?

References

1. Andrea Garavaglia and Patrick Stupar, "Local Grant Identification for EPOC TDD (baseline proposal amendment)," May 2013, garavaglia_3bn_04_0513

2. Andrea Garavaglia and Patrick Stupar, "EPoC TDD – Data Detector and Downstream PCS Considerations," May 2013, garavaglia_3bn_03_0513

3. Steve Shellhammer and Andrea Garavaglia, "EPoC TDD – A Proposal for DS Transmission and Related timing," August 2013

4. Comment during TDD Conference Call