EPoC Downstream Rate Adaption

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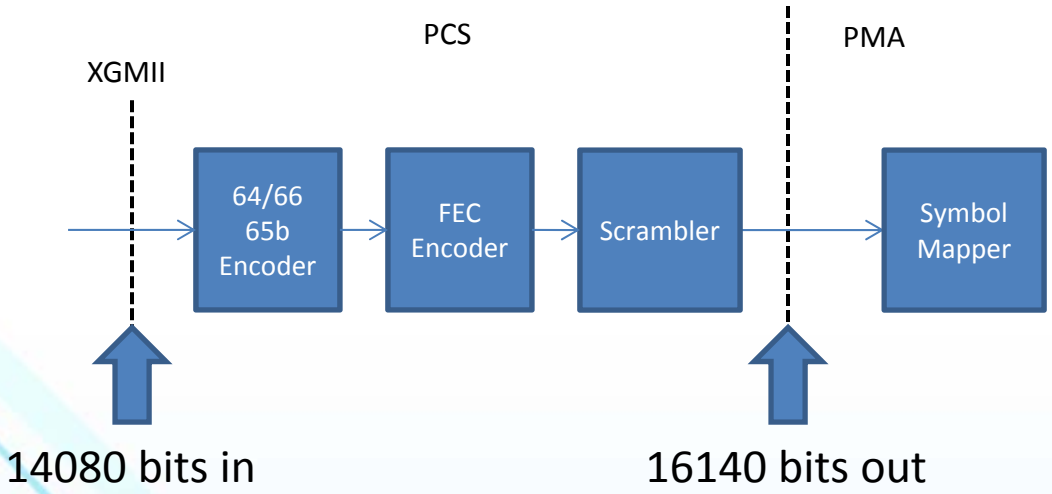
Overview

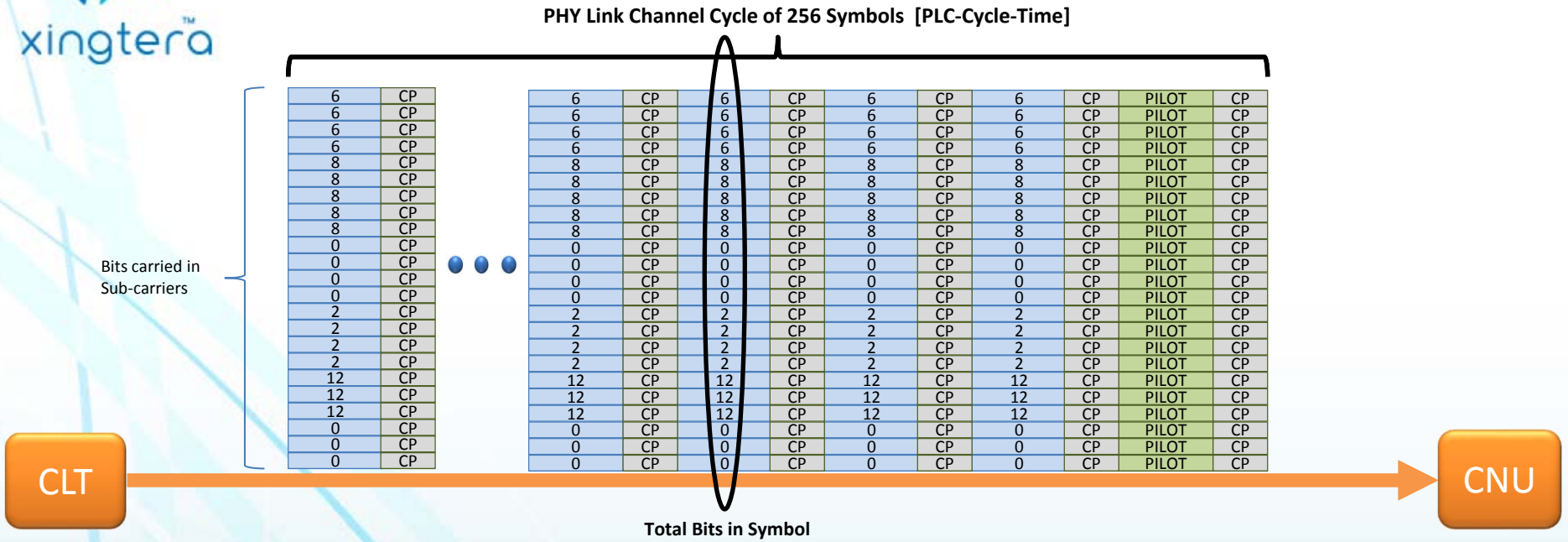
- This presentation describes the PCS & PMA to support a sub-rate downstream channel and downstream rate changes.
- A simple method to stream data from the PCS to PMA is considered.
- A modified IDLE deletion method is considered.
- Disclaimers
  - For simplicity, this presentation uses 256 symbols for the number of symbols in a PLC cycle (assuming 20us symbol duration). It is easy to replace 256 symbols with 128 symbols or a different symbol size.

EPoC PCS Overhead



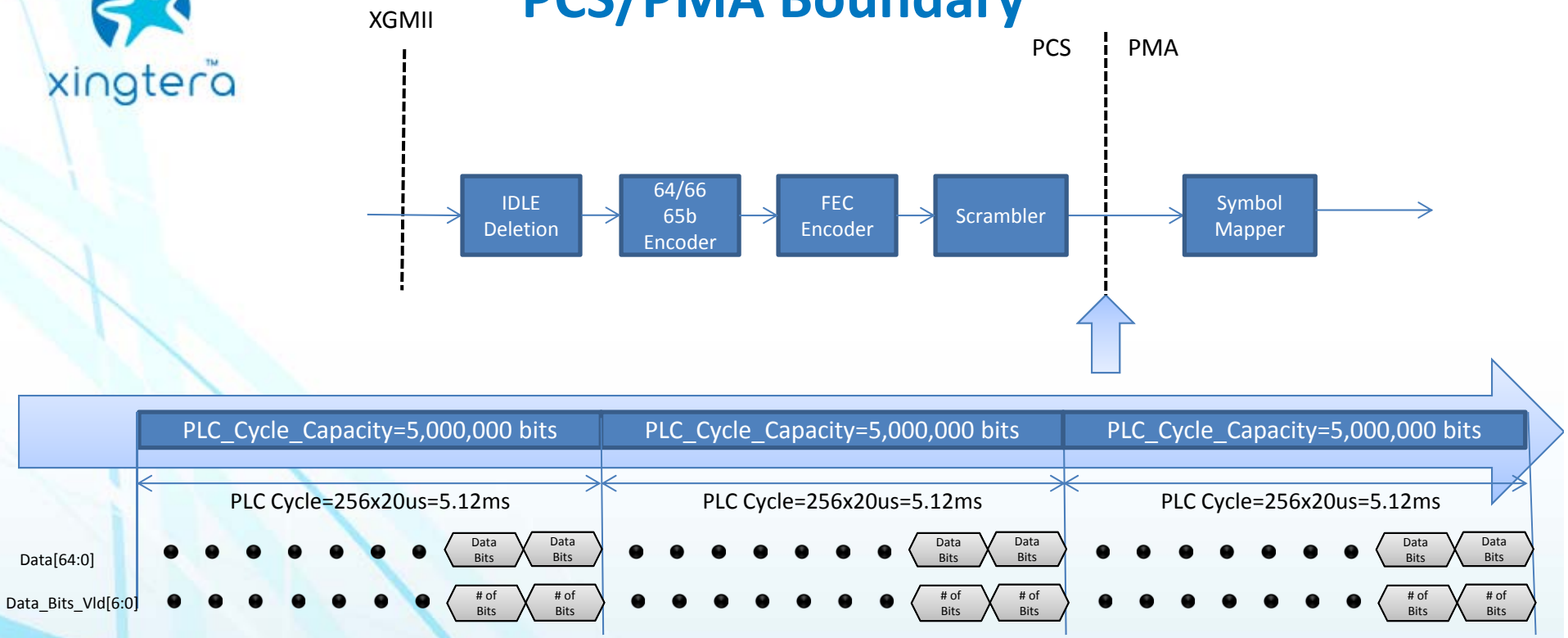
- Because of the fixed overhead 64/66 and single LDPC FEC code, the PCS has a known overhead from the input to the output.
  - Averaged over a single FEC block: 14080 bits into PCS produces 16140 bits out of PCS (87%)
- Data should be streaming at a constant rate from the PCS to the PMA.
- If the rate of PCS to PMA is known, the data rate at the XGMII can be determined for the IDLE deletion function.
- What is the streaming data rate at the PCS/PMA interface?

EPoC Downstream Rate at PCS/PMA Boundary



- Downstream MAC/PHY needs to have a known constant data rate.
  - Data Rate is averaged over PHY Link Cycle to absorb Pilots and cyclic prefix. (requires 1 symbol of delay)
  - Symbol Mapper will need to buffer 1 symbol worth of data to spread out over PLC cycle.
  - Pilots at the start of PLC cycle to avoid underrunning from streaming constant data.
    - Need to understand the implications of scattered pilots. Do we need to scatter the pilots? Do we need rules to avoid underrunning?
- Distribution of bits in sub-carriers or number of sub-carriers doesn't change Data Rate.
  - Only the total bits in symbol and the symbol/cyclic prefix size matter.
- PCS/PMA Data Rate is calculated…
  - PLC-Cycle-Capacity = Total-Bits-in-Symbol*(256-1)
  - PCS-PMA-Rate = PLC-Cycle-Capacity/PLC-Cycle-Time

PCS/PMA Boundary



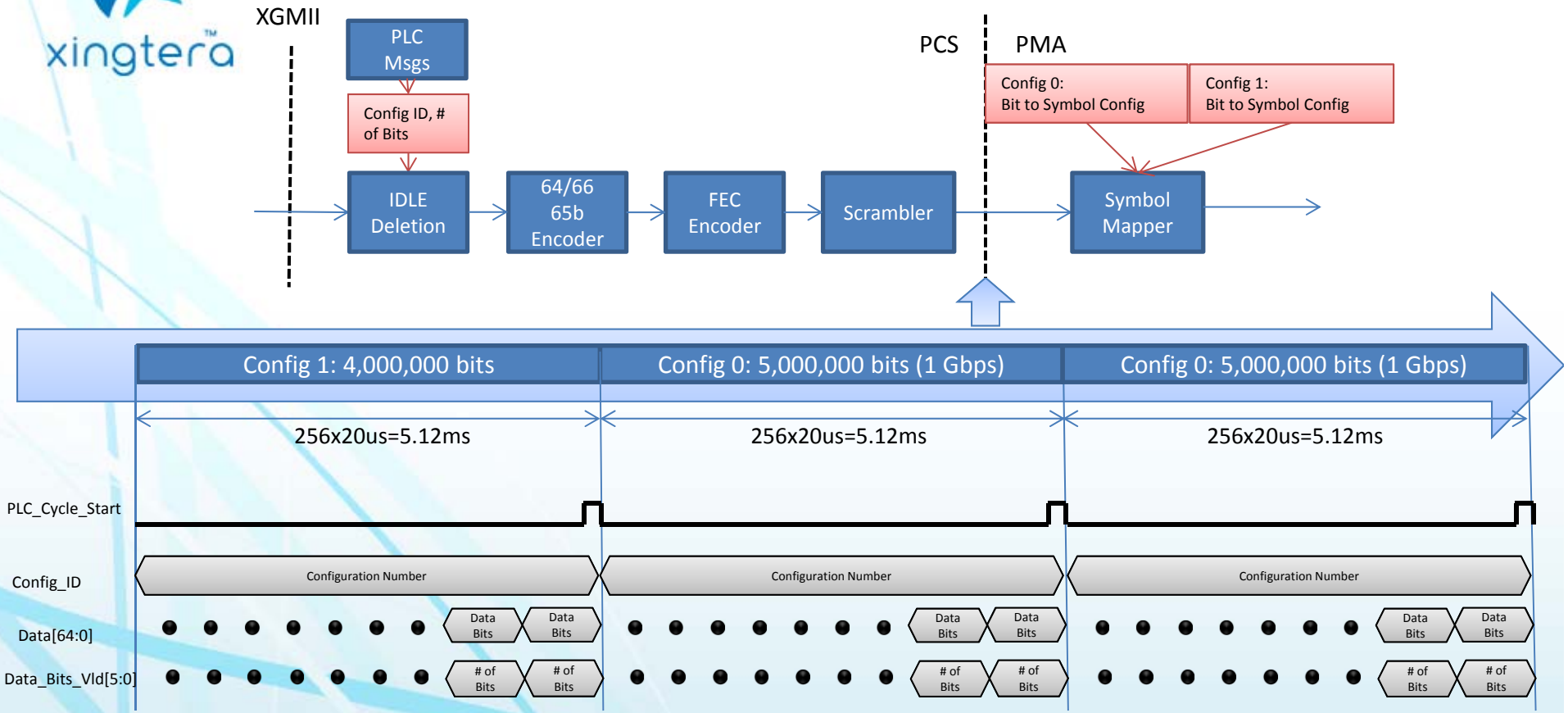
- PCS Streams data in 65 bit blocks to PMA.
  - Based on 204.8MHz clock, maximum data rate of 13.312 Gbps
- Data is spread evenly across entire PLC cycle.
  - PMA is responsible for buffering and smoothing data for Pilots

Configuration Switchover Review

- Goals
  - As CNUs register, the EPoC downstream maybe required to lower the bit loading to achieve a good BER.
  - During normal operation, interference may require the EPoC system to adapt the bit loading.
  - In both cases, it is important that EPoC provide a method to modify the bit loading table during normal operation and desirable that it be hitless (no packet loss) and non-service interrupting to the subscribers.
- Coordinating Switchover between MAC and PHY
  - MAC and PHY are not required to match transmit rates exactly.
  - The MAC TX rate must be equal to or less than PHY TX rate.
  - By selecting a proper order of operation, the TX can be safely changed
    - For decreasing rates: The MAC rate should be decreased before the PHY rate can be decreased.
    - For increasing rates: The PHY rate must be increased before the MAC rate is increased.
- Coordinating Switchover between CLT PHY and CNU PHY
  - The PLC Configuration ID allows for changing configuration at PLC Cycle boundaries.

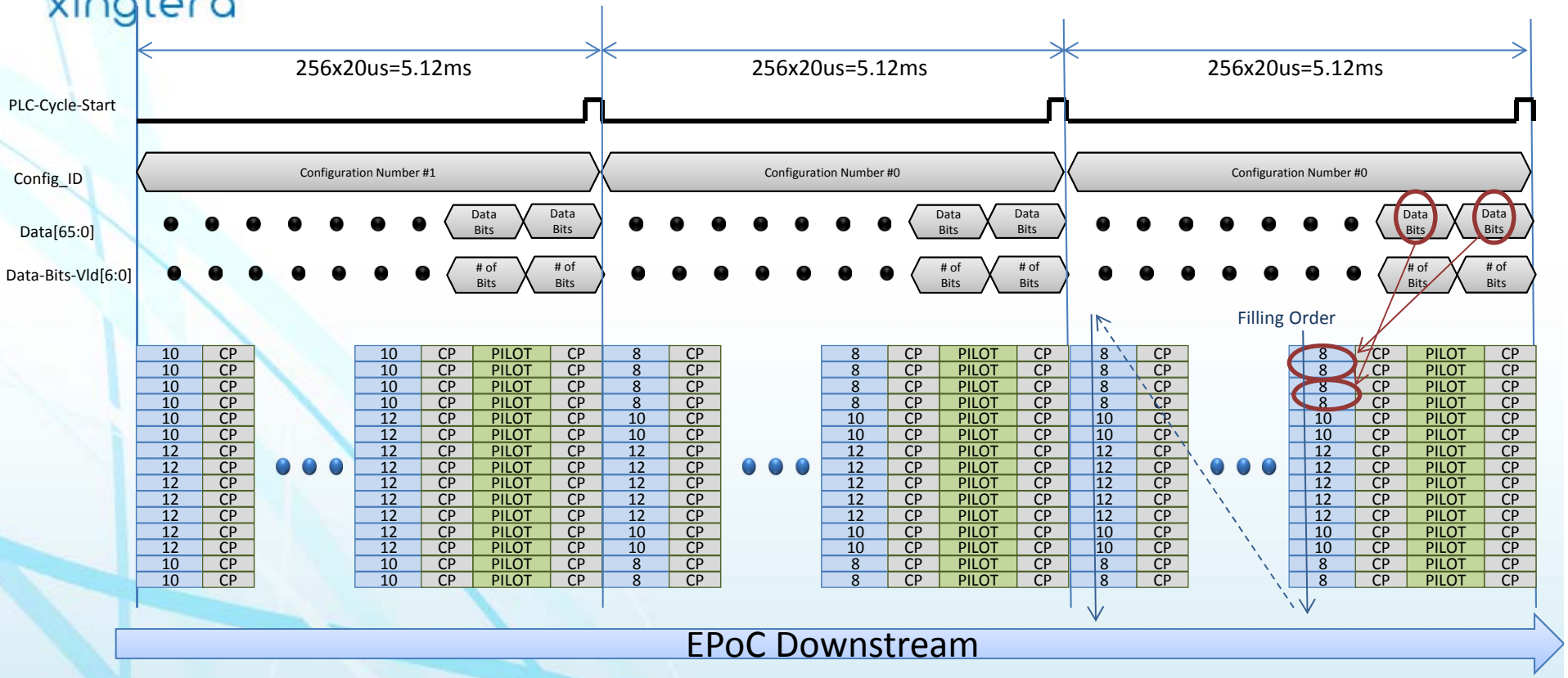
See boyd_3bn_02a_0313.pdf from the Orlando March 2013 meeting for additional details

PCS/PMA Boundary with Configuration Switch



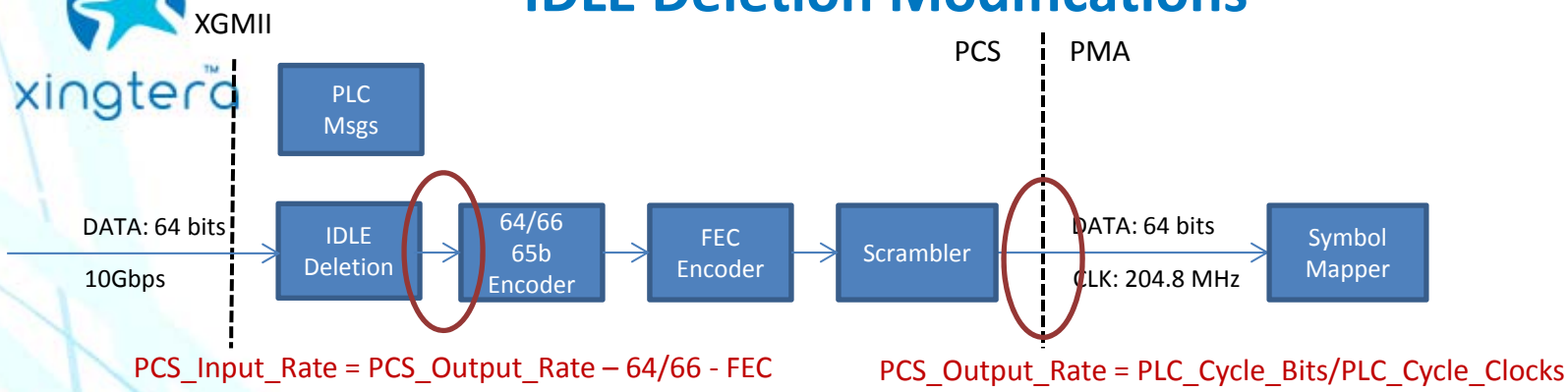
- PLC Cycle is a fixed duration and aligns with configuration boundaries.
- PLC Cycle Bit Capacity is based on configuration and could change over time.
- CLT PHY passes the configuration ID to the remote CNU PHY through the PLC Msgs.
- PLC Msgs block also passes the Configuration ID and bit capacity to the IDLE Deletion.
- PLC Cycle Start and Configuration ID are passed through the PCS to the PMA to clearly indicate the switchover between configurations on a PLC cycle boundary.
- Note: PLC_Cycle_Start and Config_ID maybe combined into a single type code for the interface.

Downstream PMA Symbol Mapper (1D-to-2D)



- A single Pilot Symbol is inserted on every sub-carrier at the start of the PLC cycle.
  - NOTE: Scattered Pilots could be considered as well but the pattern must guarantee than the output doesn't underflow.
- Streaming Data from the PCS is buffered and diced in a fixed order into the sub-carriers.
  - Frequency Interleaving would specify a different order for loading the data.
- Configuration changes (bit loading) will change the capacity of the entire PLC cycle and are aligned with new sub-carrier bit loading values for the PMA.

IDLE Deletion Modifications



- The IDLE Deletion function should be modified to accurately match the EPoC PHY.
  - State machine function for FEC and Data Rate Adaption can be combined.
  - The Data Rate Adaption should be referenced to the 204.8MHz PHY clock to match PMA exactly.
  - Support for configuration (bit loading) switch over should be added.
- IDLE Deletion Output Rate
  - PCS_Input_Rate = (64 bits/65 bits)*(FEC_Encoder_In_Bits /FEC_Encoder_Out_Bits)*PCS_Output_Rate
  - PCS_Output_Rate = PLC_Cycle_Bits/PLC_Cycle_Clocks [Based on 204.8MHz clock counts]
  - PCS-Input-Rate = (64*FEC_Encoder_In_Bits*PLC_Cycle_Bits) / (65*FEC_Encoder_In_Bits*PLC_Cycle_Clocks)
  - PCS-Input-Rate = Rate_Numerator / Rate_Denuminator
- New IDLE Deletion State Machine
  - Reference to 204.8MHz PMA sampling clock
  - Update Rate Changes on PLC cycle boundaries.
  - Add Counter to track fractions of bits to produce accurate output rate.

IDLE Deletion Modifications

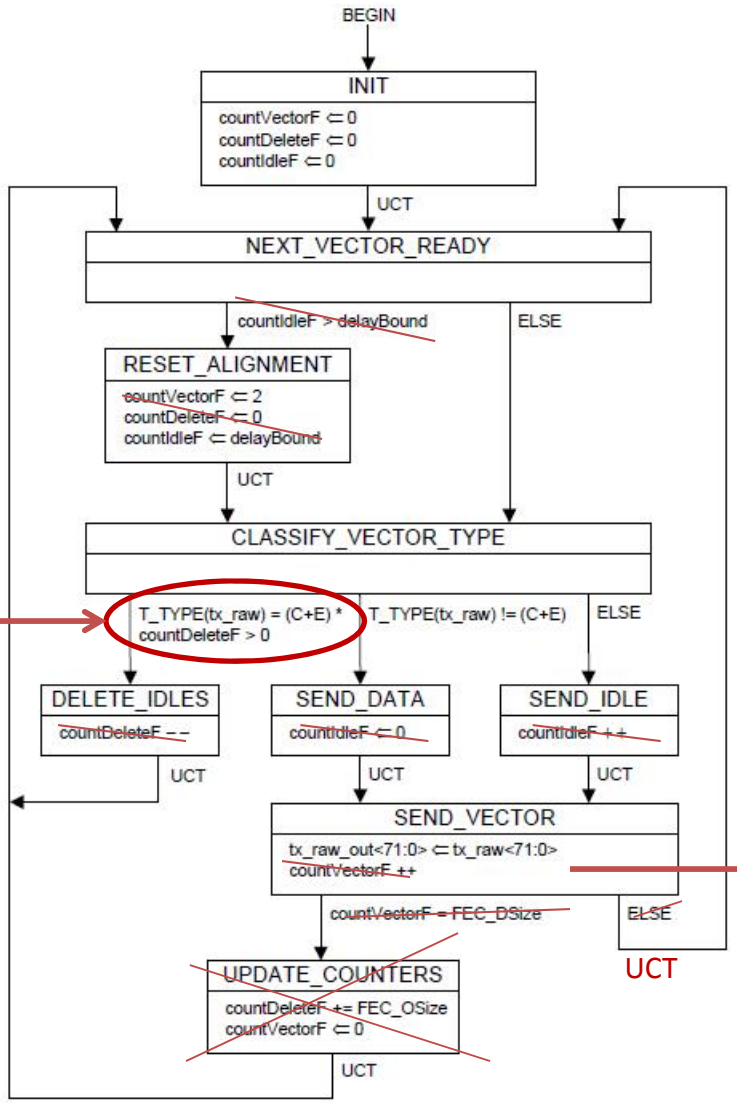


Figure 101–7—CNU Idle control character deletion process
(FEC overhead compensation sub-process)

Change "countDeleteF > 0" to "ExcessBitCounter > 64"

PLC Cycle Counter

Clock 204.8MHz

New numerator only at PLC cycle count boundary

ADD Rate_Numerator

Fraction Bit Counter

Clock 204.8MHz

SUB TxBitsOut*Rate_Denominator

TxBitsOut = Int(FractionBitCounter/Rate_Denominator)

SUB TxBitsOut

ADD 64 bits

Excess Bits Counter

XGMII

IDLE Deletion Modification Summary

- Rate Switchover
  - Only the Rate_Numerator will change with new bit loadings.
  - Rate_Numerator will only change on the PLC cycle boundary.
  - The number of PLC cycles with an output rate will be the same for PCS and PMA blocks.
- Determining the number of IDLEs to delete
  - The streaming output rate is tracked by a summation of fractional bits on every clock.
  - The number of bits over the streaming data rate that are passed through the IDLE Deletion block are tracked.
  - When a non-essential IDLE character appears on the IDLE, it is dropped if excess bits are greater than the size of the IDLE character.
- Timestamp Jitter
  - The IDLE insertion function in the MAC should guarantee a packet payload rate less than the PCS_Input_Rate.
  - The IDLE deletion function must be able to delete enough idles after a packet to make the “Excess Bits Counter” go under 64 bits.
  - The start of the packet will not experience more than 64 bits of jitter. (Should we reduce this amount?)
- IDLE Deletion Buffer Size
  - The FIFO in the IDLE Deletion block must be able to buffer a maximum size Ethernet Frame + Preamble + IPG. (2020 Bytes)
  - After buffering a single packet (worst cast rate difference), the IDLE characters will be deleted and buffer will empty.
- Receiver Side IDLE Insertion State Machine
  - It is simple to use the same approach to create a streaming output with IDLEs inserted on the CNU side.

Downstream Data Rate Summary

- PMA Symbol Mapper
  - Single Symbol of Pilots is simplest approach for insertion.
  - Symbol mapper should be defined to buffer 1 symbol of data to smooth data over PLC cycle.
- PCS/PMA Interface
  - 65 bit interface clocked at 204.8MHz (sampling clock locked)
  - Configuration ID and PLC Cycle Start should be included in the interface.
- IDLE Deletion
  - A single function based on the output streaming rate should be used. (combine FEC and rate functions)
  - The function should support rate switchover.
  - It should be locked to the 204.8MHz clock to accurately stream data to the PMA.
  - It is simple to use the same approach to create a streaming output with IDLEs inserted on the CNU side.