

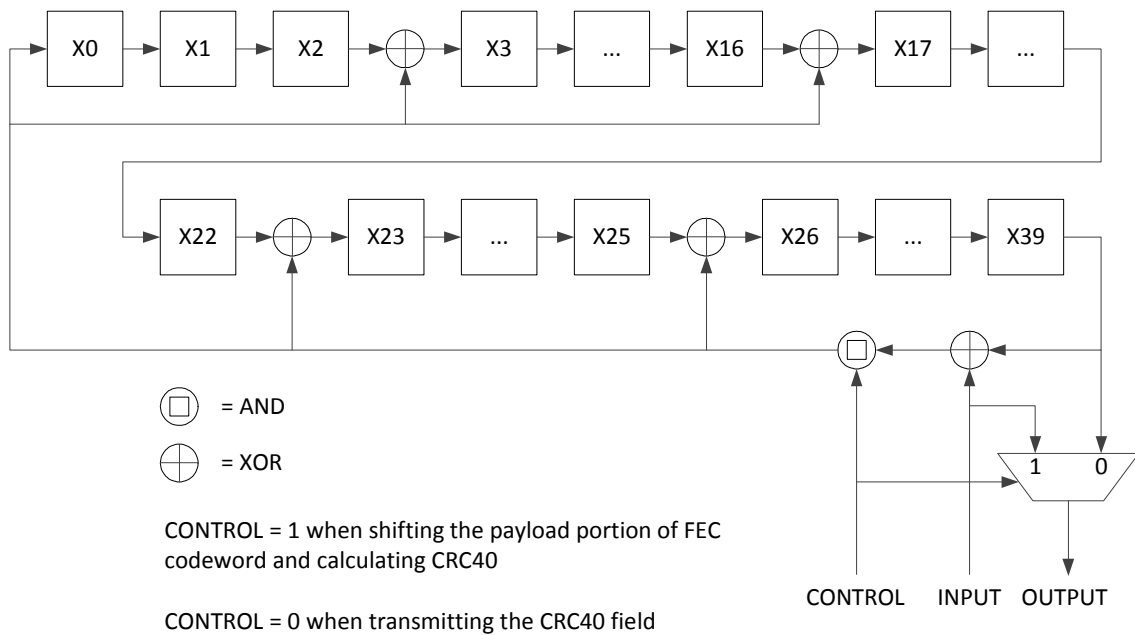
**101.3.2.3.6 CRC40**

The CRC40 field contains a 40-bit cyclic redundancy check value. This value is computed as a function of the contents of the B<sub>Q</sub> 65-bit blocks, forming the payload portion of the FEC codeword.

The encoding is defined by the CRC40 generating polynomial shown in Equation (101-1):

$$x^{40} + x^{26} + x^{23} + x^{17} + x^3 + 1 \tag{101-1}$$

This CRC40 calculation shall produce the same result as the serial implementation shown in Figure 101-1. At the beginning of each FEC codeword (before the calculation of CRC40 begins), the shift register shall be initialized to the value 0x00. The content of the shift register is transmitted without inversion.



**Figure 101-1—CRC40 generation**

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