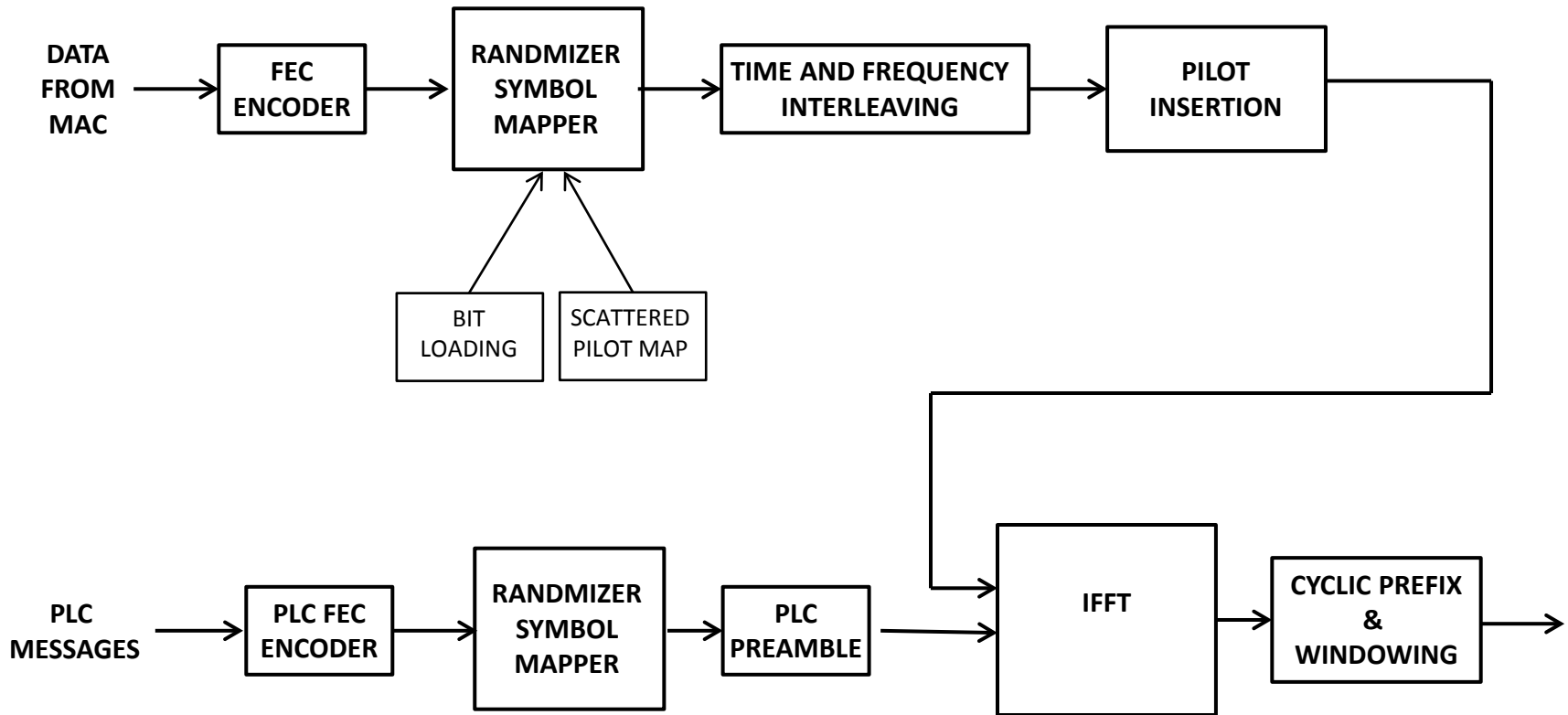


Update to Downstream PHY High Level Block Diagram – R01

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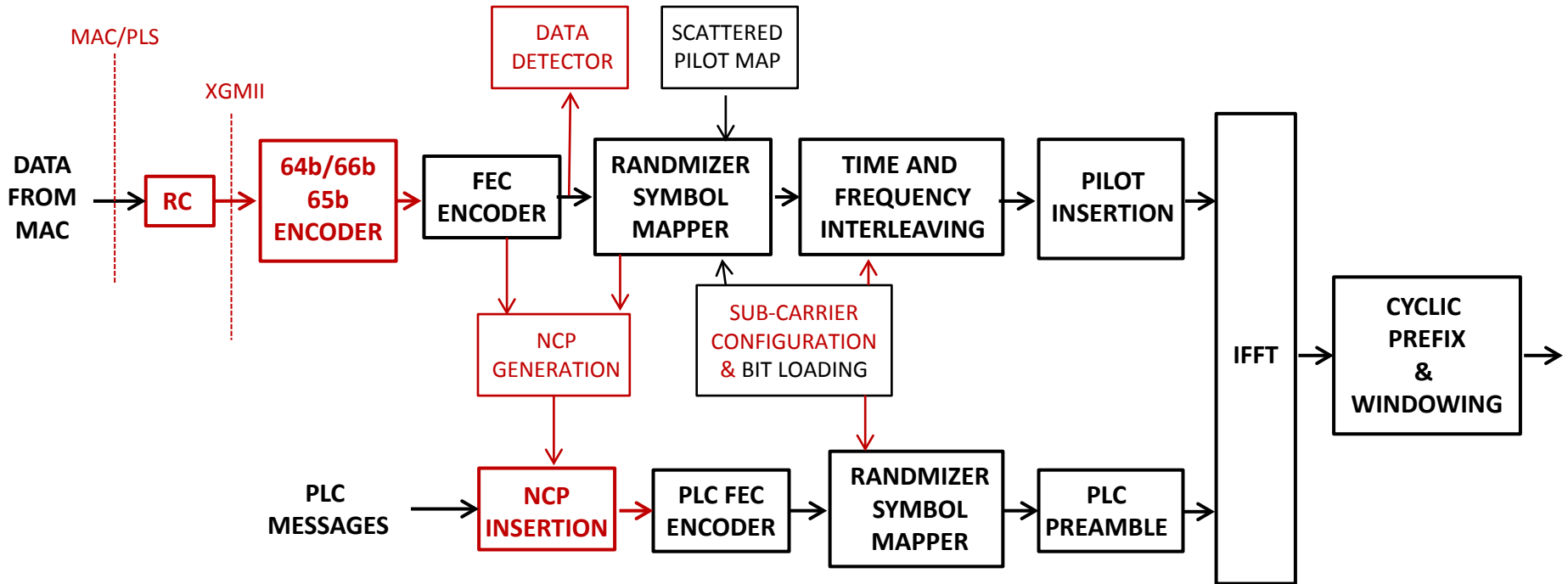
Previous:



EPoC Downstream Transmitter Block Diagram (starting point)

NOTE: All digital domain

Update R01:



EPoC Downstream **CLT** Transmitter Block Diagram

NOTE: All digital domain

NOTE: Sub-Carrier Configuration includes sub-carrier use and QAM mapping

NOTE: Not converted yet to IEEE 802 Vertical Form

Summary

- Update for CLT downstream PHY high-level block diagram
- CNU upstream PHY block diagram forthcoming
 - Dependent on upstream PLC architecture
- All digital domain
- NOTE: does not include channel bonding and compatibility at this time
 - T.B.D.

THANK YOU