Rate Adaptation

Changes Needed

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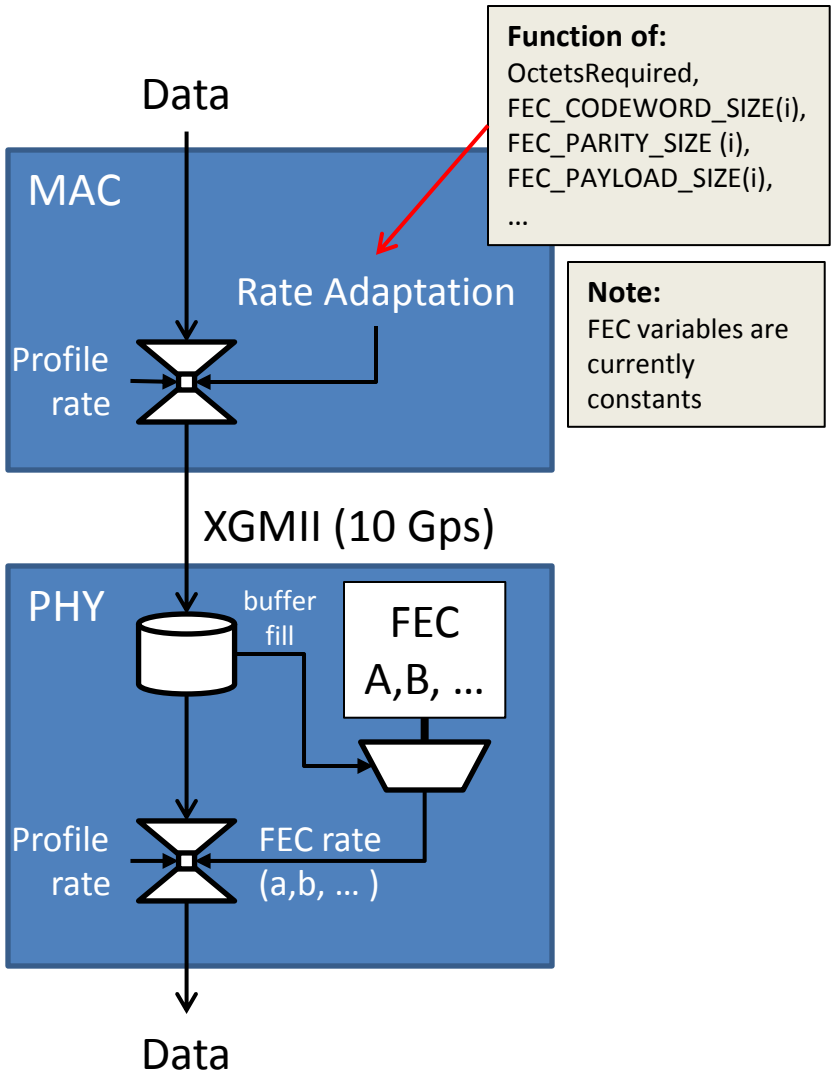
Current Rate Adaptation

- Assumes Constant Rate for PHY/media
  - But we have multiple FEC rates which will vary the effective rate on the media
  - Therefore this assumption is FALSE
- How can we address this?
  - Fixes needed in both MAC and PHY
  - Fixes needed for US (both FDD and TDD) and DS (TDD only)

TX Rate Adaptation

- MAC must not send data to the PHY at a rate greater than the average capacity
- BUT XGMII operates at a constant rate (~10 Gbps)
- For burst mode PHY the average capacity is not constant because the FEC rate will vary depending on burst size, and data to be sent.

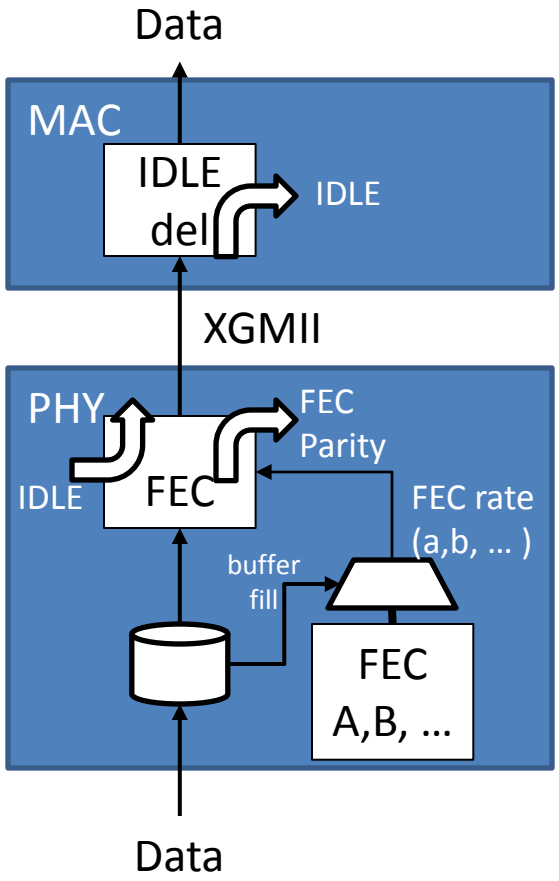


Other Rate Adaptation considerations

- MAC Tx Rate Adaptation:
  - Inserts IDLE to account for IPG
  - Inserts IDLE to account for FEC
    - Needs to predict FEC rate – which 1 of n rates
  - Inserts IDLE when no data is available or when data exceeds remaining burst size
- PCS Tx Rate Adaptation:
  - Removes IDLE to insert FEC
    - Needs to use same FEC rate predicted by MAC (OK to use higher rate FEC)
- Conclusion:
  - TX MAC and TX PCS need to use essentially the same algorithm to determine FEC/FEC Rate!

RX Rate Adaptation

- PCS removed FEC and replaces parity bits with IDLE
- Must determine which FEC the transmitter used
- Conclusion:
  - Rx PCS needs to use essentially the same algorithm to determine FEC as TX PCS and TX MAC!



State Diagrams possibly impacted

- CL 101
  - Figure 101–4—CLT Idle control character deletion process (data rate adaptation sub-process)
  - Figure 101–5—CLT Idle control character deletion process (FEC overhead compensation sub-process)
  - Figure 101–6—CNU Idle control character deletion process (data rate adaptation sub-process)
  - Figure 101–7—CNU Idle control character deletion process (FEC overhead compensation sub-process)
  - Possibly FEC SD's added in York; Figure 101–9—FEC encoder, input process state diagram, Figure 101–10—FEC encoder, output process state diagram (CLT), Figure 101–14—FEC decoder, input process state diagram (CNU), Figure 101–15—FEC decoder, output process state diagram (CNU)
  - Figure 101–16—Idle control character insertion process state diagram
  - Some fixes may be done in functions used in these SD's

State Diagrams possibly impacted

- CL 102
  - Figure 102–13—CLT Control Multiplexer state diagram
  - Figure 102–14—CNU Control Multiplexer state diagram
  - Figure 102–28—Gate Processing state diagram at CLT (?)
  - Figure 102–29—Gate Processing CLT Activation state diagram (TDD mode only)
  - Figure 102–30—Gate Processing CNU Programing state diagram
  - Figure 102–31—Gate Processing CNU Activation state diagram

  - Some fixes may be done in functions used in these SD’s

Conclusion

- Need a single algorithm for Rate Adaptation for MAC & PHY that uses different variables but is essentially the same and produces a deterministic results for IDLE insertion and deletion to allow for a variable line rate on the media.