Upstream Framing Options

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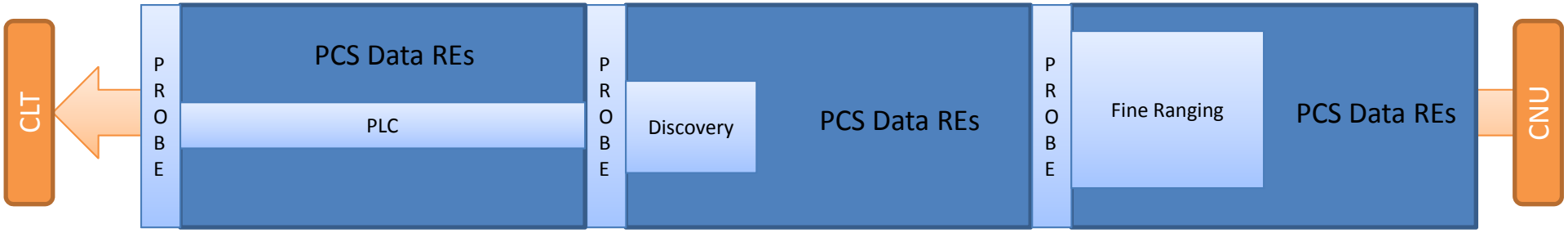
Overview

- This presentation is an attempt to simplify the EPoC upstream framing and remove some of the unnecessary inefficiencies as well.
- It is shouldn’t be viewed as an all or nothing. Most of the items are able to stand on their own.
- Topics to be addressed
  - PMA Framing: Single fixed structure.
  - Data Detector Starting Position
  - FEC/CRC40 Parity

PMA Framing

SINGLE STRUCTURE

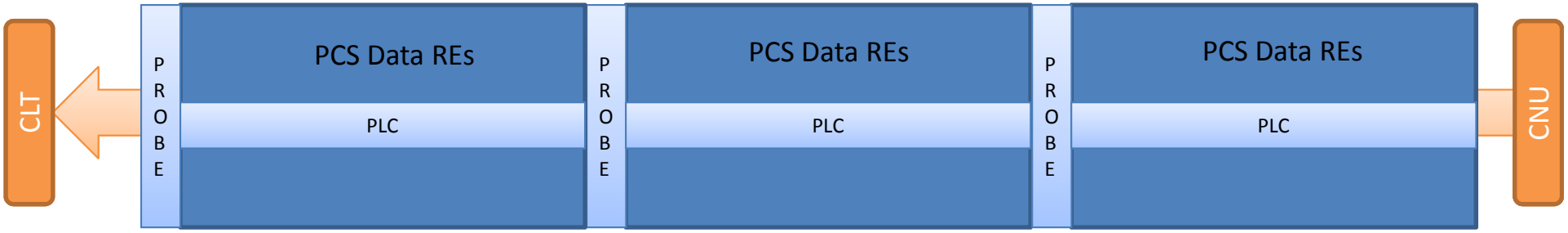
Granted Frame Structure



- The super frame creates space for the probe by delaying and buffering data.
- The capacity and definition for resource elements changes based on a granting from the PLC.
- The amount of buffering and delay required changes based on the granting of the frame structure.

This is too complex

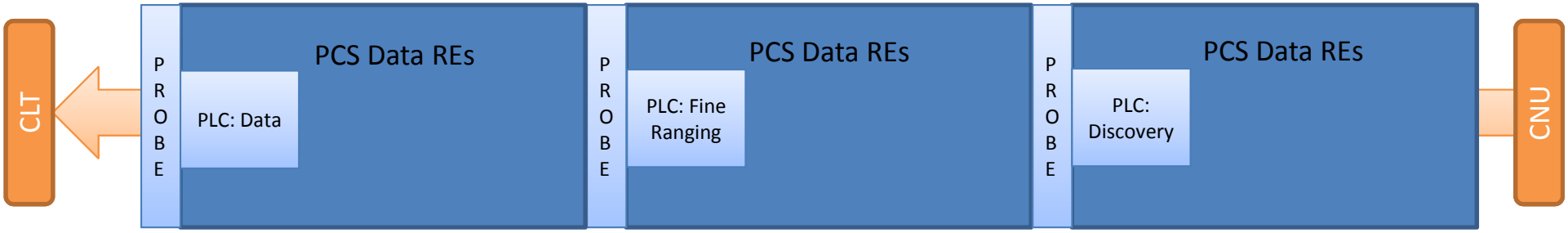
Simplified Structure



- PLC is dedicated sub-carriers.
  - Will be used for Initial Discovery and Ranging
- Probe is fixed duration and periodic.
- Capacity is always constant.
  - No need for dummy bits in different configurations.
  - No complicated decision on where to start.
- Delay is constant and lower
  - No additional delay in super frame outside of the Probe.
  - Probe delay is 2 symbols and not based on data rate.
  - Granting of different structures doesn't change delay based on bit loading of covered Res/
- Symbol mapper and Interleaver is simple
  - No need to worry about the granted structure.

This is the best solution if we can fit into a narrow PLC

Single Structure



- If fine ranging can't be done in the probe and discovery can't be done in a narrow PLC, we can still simplify.
- The PLC can become a fixed block of REs at the start of the superframe.
  - The PLC REs will use the same REs.
- Disadvantages from the Simplified Structure
  - The delay is increased and the amount of delay is based on the bit loading of the REs covered.
- Advantages over the granted frame structure
  - Capacity is always constant.
    - No need for dummy bits in different configurations.
  - Delay is constant for a configuration (doesn't change based on PLC grant)
- Additional Simplifications
  - We should consider using the same LDPC or error detecting on all REs in this block.

A single structure is another possible solution

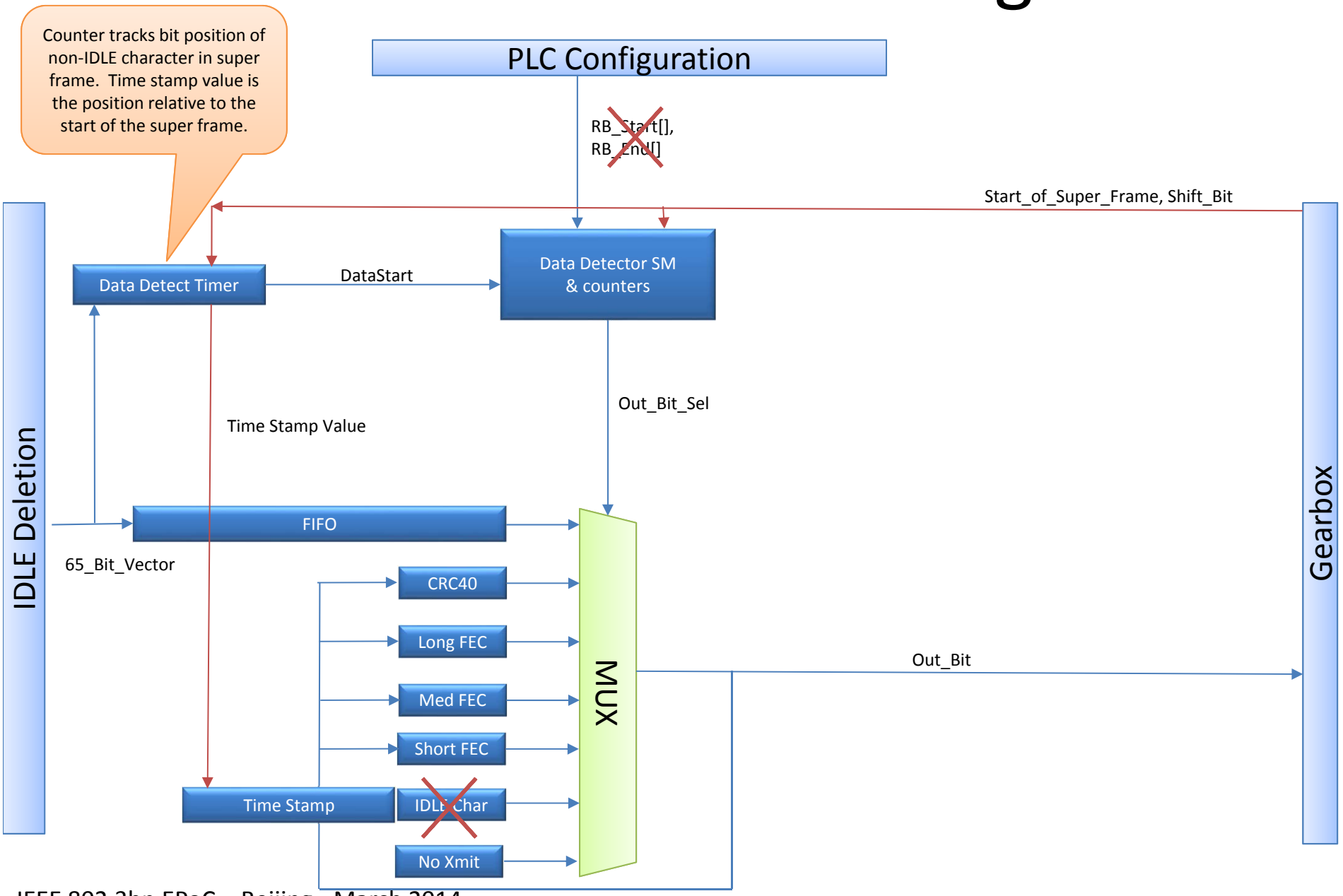
Data Detector

STARTING POSITION

Data Detector Review

- Data arriving at PCS triggers the data detector to start a burst.
- The PCS gearbox streams bits to the PMA at a constant data rate based on the configuration.
- The data burst will likely not align with the start of the Resource Block where a burst is allowed to start.
- Delaying the data a variable amount to align with the start of the burst will create too much jitter.
- The overhead for a burst because of alignment
  - Assume the highest bit loading for REs used by markers or pilots at start or end of burst.
  - Assume the worst alignment for alignment with RB.
  - Largest possible combined capacity for Start Marker+End Marker+2 RBs.
  - The overhead should be burst spacing at the CLT scheduler
- The Jitter can be removed by marking the position of the start of burst into the PCS and replaying the burst out of the receiver PCS at the same position.

Data Detector Block Diagram



PCS Data Detector

- Gearbox spreads the bits in a super frame evenly in time.
- Timer in Data Detector counts from 0 to bits_in_superframe.
- Timer is sampled when non-IDLE 65-bit codeword arrives from IDLE Deletion.
- Data Detector inserts 65 bit codeword containing the timer value at the start of the burst.
- PMA can shift packet a variable amount to insert start marker. (Maximum shift must be guardtime)
- Receiver delays data until time value in super frame is reached.

Data Detector

FEC/CRC-40

FEC & CRC-40

- These items were voted in as part of a larger package of material.
  - They should be resolved so the upstream data detector can be completed.
  - Multiple presentations have shown they decrease efficiency, add complexity, and have no benefit.
- K/2
  - The K/2 shortening does not improve the FEC efficiency but it add significant complexity.
  - It also adds delay to the transmitter and the receiver.
- Multiple CRC-40 at end of bursts
  - As shown in multiple presentations, there is no benefit to having multiple CRC-40s.
  - A single CRC-40 reduces complexity and improves efficiency.
- Parity at the end
  - Reduces the delay and the complexity of the transmitter.