Insert new clauses and corresponding annexes as follows:

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_05_0114.pfd slide 8 excluding the PHY Discovery open flag and PHY Discovery period bits.

45.2.aa Where should we put PHY-Link registers?

45.2.g.1 10GPASS-XR PHY Discovery control register (Register 1.117)

The PHY Discovery process is used to bring up new CNUs on the EPoC Coax network. The PHY Discovery control registers direct this process which is fully described in subclause 102.4. The assignment of bits in the 10GPASS-XR PHY Discovery control registers are shown in Table 45–g.

Table 45–g—10GPASS-XR DS Profile descriptor control registers bit definitions

Bit(s)	Name	Description	R/W[a]
1.117.15:13	PHY Discovery Duration	Duration of next open PHY Discovery window relative to the PHY Frame Counter	R/W
1.117.12:0	PHY Discovery start	Time of next open PHY Discovery window relative to PHY-Link frame counter.	R/W

[a]RO = Read only, R/W = Read/Write

45.2.g.1.1 PHY Discovery Duration

The PHY Discovery Duration bits 1.117.15:13 are used to set the duration, in PHY-Link frames, of the next PHY Discovery window.

45.2.g.1.2 PHY Discovery start

The PHY Discovery start bits 1.117.12:0 determine when the next PHY Discovery window is opened relative to the local PHY Link frame counter.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below correspond to remein_3bn_05_0114.pfd slide 8 and should be placed at:
45.2.1 PMA/PMD registers
45.2.1.106g last clause
Table 45–78g—last table

45.2.1.106h 10GPASS-XR PHY Frame Counter bit definitions (Register 1.1920)

The assignment of bits in the 10GPASS-XR PHY frame counter bit definition is shown in Table 45–78h

Table 45–78h—10GPASS-XR frame counter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1920.15:0	PHY Frame Counter	Counter that indicates the PHY-Link frame currently being processed by the PHY. This counter rolls over to zero and is incremented at the beginning of each PHY-Link frame	RO

[a]RO = Read only

45.2.1.106h.1 PHY Frame Counter (1.1920.15:0)

The PHY Frame Counter bits reflect the current PHY-Link frame count. This counter is incremented at the beginning of the PHY-Link frame and, on terminal count, rolls over to zero. For additional information on this counter see Clause 102.

EDITORS NOTE (NOT TO BE INCLUDED IN DRAFT): the sections below are necessary to bring the CNU to a link-up state and should be placed in Clause 45.2.1

45.2.1.60i 10GPASS-XR PHY Timing Offset (Register 1.1921)

The assignment of bits in the 10GPASS-XR PHY Timing Offset bit definition is shown in Table 45–78i

Table 45–78i—10GPASS-XR timing offset bit definitions

Bit(s)	Name	Description	R/W[a]
1.1921.15:0	PHY Timing Offset lower	Transmit timing offset adjustment. [15:0]	R/W, MW
1.1922.15:0	PHY Timing Offset upper	Transmit timing offset adjustment. [16:31]	R/W, MW

[a]MW = Multi-word

45.2.1.60i.1 PHY Timing Offset(1.1921.15:0 & 1.1922.15:0)

The PHY Timing Offset bits are used to align the CNU to the upstream OFDM timing. For more information on the use of this register see Clause 102.4.

45.2.1.60j 10GPASS-XR PHY Power Offset (Register 1.1923)

The assignment of bits in the 10GPASS-XR PHY Power Offset bit definition is shown in Table 45–78j

Table 45–78j—10GPASS-XR timing offset bit definitions

Bit(s)	Name	Description	R/W
1.1923.15:8	Reserved	Ignore on read	RO
1.1923.7:0	PHY Power Offset	TX Power offset adjustment (signed 8-bit, 1/4-dB units).	R/W

45.2.1.60j.1 PHY Power Offset (1.1923.7:0)

The PHY Power Offset, bits 7:0 of register 1.1923, are used to set the CNU upstream transmitter power. For more information on the use of this register see Clause 102.4.