

Work items for November 2013

IEEE P802.3bn EPoC PHY Task Force

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Downstream Items

- FEC (Marek)
 - Active / Passive, FDD / TDD
- Continuous Pilot Insertion (Avi, Christian, Jin)
- Randomizer and Symbol Mapper (Jin)
 - Bit Loading
 - Scattered Pilots
 - Sub-carrier configuration (e.g QAM level, pilot use, etc.)
- Exclusion rules (Steve, Leo)
- Time and Frequency Interleaving (Name Rich)
- IFFT (IDFT) (Leo)
- Cyclic Prefix and Windowing (mostly done, Leo)
 - OFDM Symbol definition (useable symbol + CP + postfix, picture, etc.)
- Burst Structure
- Burst Marker (Syed, Leo)
- Burst Control / Local Gates
- Data Detector (Marek)
- Channel “bonding” (Mark, Avi, ...)

Upstream Items

- FEC (Marek)
 - Active / Passive, FDD / TDD
 - Codeword Filling (FDD: Rich, TDD: Steve, Christian)
- Pilots
 - Pilot Structure (coupled with RB)
- Exclusion rules (Steve, Leo)
- 1D / 2D Mapping (Sanjay G.)
- Frequency Interleaving (Duane, Avi)
- Scrambling / Randomization
- Cyclic Prefix and Windowing (mostly done, Leo)
- Resource Block / Burst Structure (Marek, Sanjay G.)
- Burst Markers (Syed, Leo)
- Data Detector (Marek)
- Probing (Leo, Syed)
- Pre-equalization (Leo)

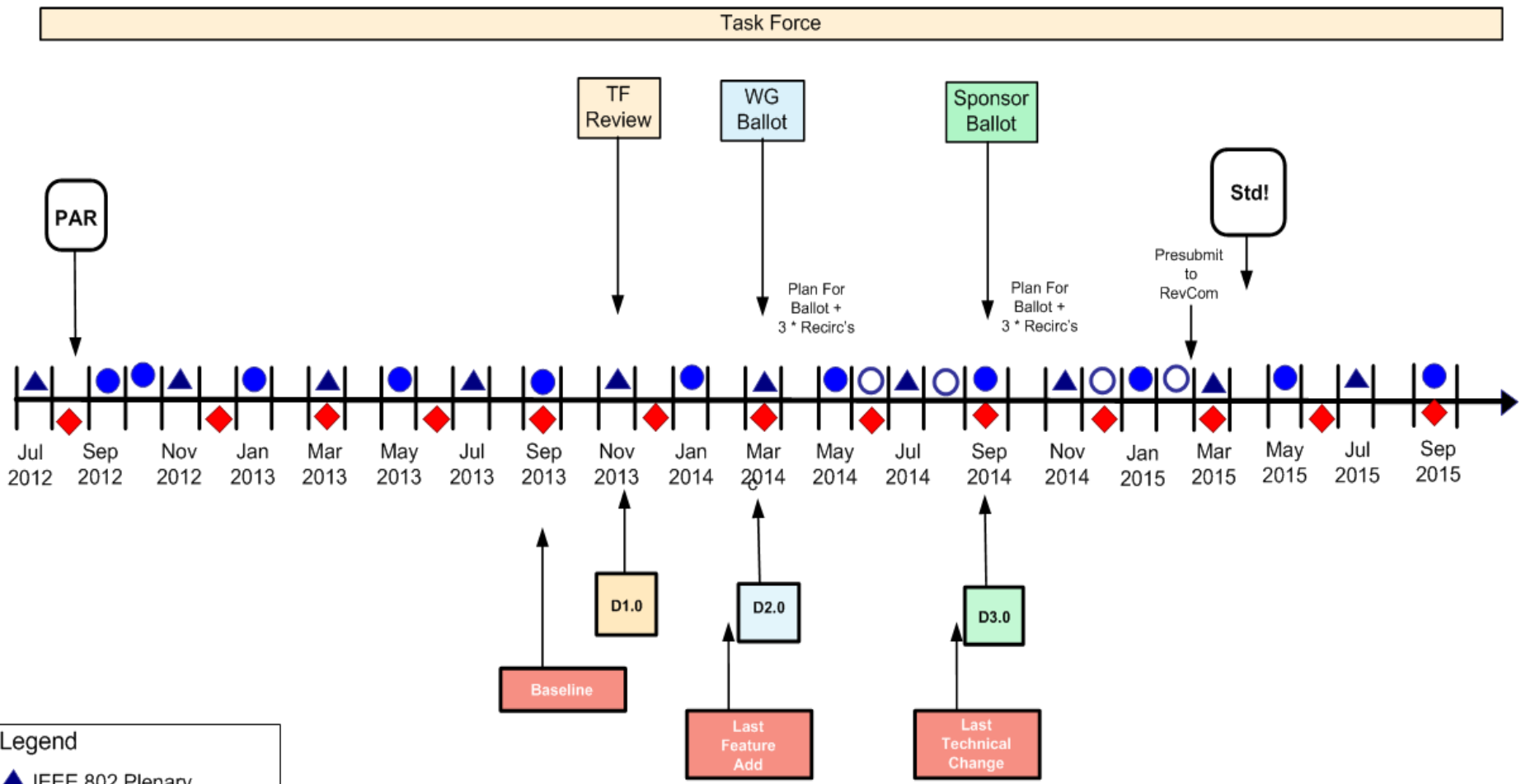
PHY Link

- PHY Link and procedures (Avi, Duane, Jin)
 - “Bring up” through auto-negotiation to Linked
 - “Ranging” and symbol synchronization (Bill, Leo, Avi, Hesham)
 - Includes periodic maintenance
- PHY Link acquisition
 - “Lock” and “lost sync” procedures

System Issues

- PHY path diagrams (Avi, Mark)
 - PCS, PMA
 - DS and US
- FEC CRC-40 baseline text (Rich)
- Sublayer interfaces (Marek)
 - Clocking / jitter
- MPCP Interoperation
 - Gate / Report (Sanjay G.)
 - MAC Discovery and registration verification (Sanjay G. maybe)
- Transmitter Power and Fidelity
- Performance
 - Error rates
 - Latency / Jitter
- RF Spectrum (Steve)
- Electrical Input / Output (Saif, Mark)

Task Force Timeline (updated 3/21/13)



Legend

- ▲ IEEE 802 Plenary
- IEEE 802 Interim
- ◆ IEEE-SA Standards Board

Thank You!