Table 97–3—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1	1.0.15	PMA_reset
Global transmit disable	Transmit disable register	1.9.0	Global_PMA_transmit_disable

Table 97–4—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Fault	Status register 1	1.1.7	PMA_fault
Transmit fault	Status register 2	1.8.11	PMA_transmit_fault
Receive fault	Status register 2	1.8.10	PMA_receive_fault

97.4.2.4 PMA Receive function

The PMA Receive function comprises a receiver for PAM3 signals on the twisted pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the twisted pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 3.6×10^{-7} after RS decoding, over a channel meeting the requirements of 97.5.4.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

97.4.2.5 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 97–18.

During PMA training (TRAINING and COUNTDOWN states in Figure 97–18), PHY Control information is exchanged between link partners with a 12 octet InfoField, which is XOR'ed with the first 96 bits of the 15th partial RS FEC frame (bits 2520 to 2615) of the RS FEC frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM3 transition.

The 12 octet InfoField shall include the fields in 97.4.2.5.2 through 97.4.2.5.8, also shown in the overview Figure 97–13, and the more detailed Figure 97–14 and Figure 97–16. Each message shall be transmitted at least 256 times (<1 msec) to ensure detection at link partner.

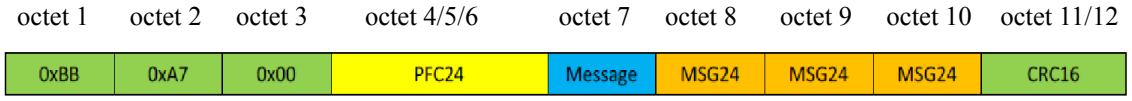

Figure 97–13—InfoField format

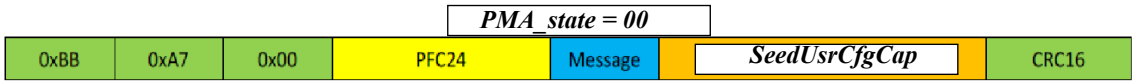

Figure 97–14—InfoField TRAINING format

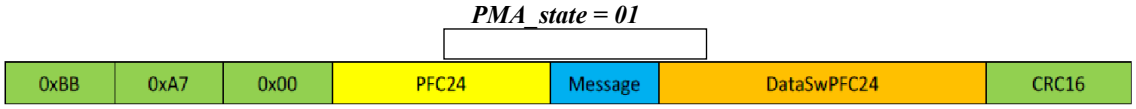

Figure 97–15—InfoField COUNTDOWN format

Figure 97–16—InfoField message exchange format

97.4.2.5.1 Infofield notation

For all the InfoField notation below, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. The InfoField is transmitted following the notation described in 97.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

97.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

97.4.2.5.3 Partial Frame Count (PFC24)

The start of Partial Frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial RS FEC frames sent LSB first. There are 15 partial frames per RS FEC frame and the Infofield is embedded within the 15th partial frame. The first partial frame is zero, thus the first partial frame count field after a reset is 14.

97.4.2.5.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 97–5 for the MASTER and Table 97–6 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 97–5 for the MASTER and the first row of Table 97–6 for the SLAVE. Moreover, for a given Message Field setting, the following Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status=OK the InfoField variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

Table 97–5—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 97–6—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

97.4.2.5.5 PHY Capability Bits, User Configurable Register, andData Mode Scrambler Seed

When PMA_state<7:6>=00, [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the two PHY capability bits (Cap), the user configurable register bits, and the 15-bit data mode scrambler seed (Seed). Each octet is sent LSB first.

The format of PHY capability bits is Oct9<7>=EEEen and Oct10<0>=OAMen, indicating EEE and OAM capability enable respectively. The PHY shall indicate the support of optional capabilities by setting the corresponding capability bits to 1. Otherwise it shall set the capability bit to 0 to indicate no support for the optional capability.

The data mode scrambler seed contain~~ings~~ bits S14 (sent first) to S0 (sent last) to indicate the initial state of data mode transmit scrambler of the local device upon reaching the data switch partial frame count. The state of the scrambler in Figure 97–7 shall be S14:S0 at the first bit of the first RS FEC frame when DataSwPFC24 = 0, see 97.4.2.5.6. The format of Seed is Oct8<7:0> = S<7:14>, Oct9<7> = 0, Oct9<6:0> = S<0:6>, Oct10<7:0> = 0 and shall not be all zeros. ~~Each octet is sent LSB first.~~

The remaining 7-bit Oct10<7:1> shall be user configurable register. See Subclause 97.4.2.5.10 for details.

97.4.2.5.6 Data Switch Partial Frame Count

When PMA_state<7:6>=01, [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial frame count when the transmitter switches from PAM2 to PAM3 which occurs at the start of a RS FEC block. The last value of PFC24 prior to the transition is DataSwPFC24 - 1.

97.4.2.5.7 Reserved Fields

When PMA_state<7:6> is greater than 01, [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

97.4.2.5.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 97–17. In Figure 97–17 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct5 through Oct10 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 97–17. After all the 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

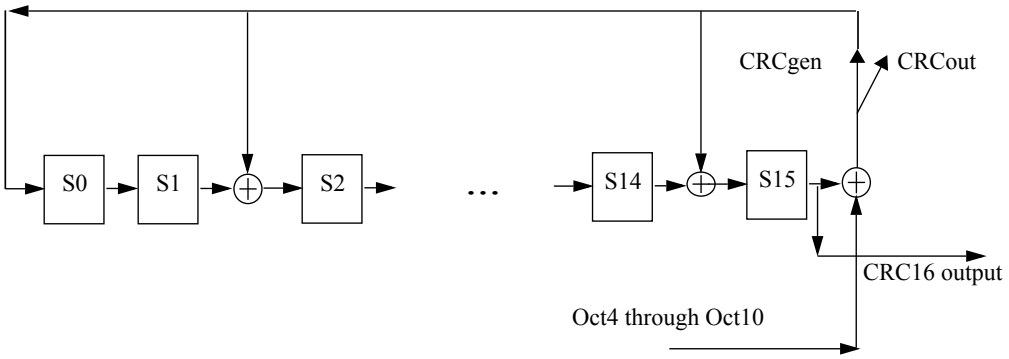

Figure 97–17—CRC16

Editorial Note (to be removed prior to publication): Figure 97-17 seems to be a replica of Figure 98-3. I am sure we could cross reference between Clauses, if CRC16 polynomials are exactly the same and operation can be generalized.

97.4.2.5.9 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 97–18.

During Auto-Negotiation, PHY Control is in the DISABLE_1000BASE-T1_TRANSMITTER state and the transmitters are disabled.

When the Auto-Negotiation process asserts link_control=ENABLE PHY Control enters the INIT_MAX-WAIT_TIMER state. Upon entering this state the maxwait_timer is started.

PHY Control then transition to the SILENT state. Upon entering this state the minwait_timer is started and the PHY transmits zeros (tx_mode=SEND_Z).

In MASTER mode PHY Control immediately transitions to the TRAINING state.

Upon entering the TRAINING state, the minwait_timer is started and the PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T, which includes the transmission of InfoFields. The PHY Control also sets PMA_state = 00 and sends the PHY capability bits, the user configurable register bits, and the Seed value used by the local device for data mode scrambler initialization, see 97.4.2.5.5.

The optional EEE capability shall be enabled only if both PHY set the capability bit EEEen=1. The optional OAM capability shall be enabled only if both PHY set the capability bit OAMen=1.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx=0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER must set en_slave_tx=1 to allow the SLAVE to transition to TRAINING.

In SLAVE mode PHY Control transitions to the TRAINING state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall align its transmit 81B-RS frame to within +0/-1 partial frames of the MASTER as seen at the SLAVE MDI. The SLAVE InfoField Partial Frame Count shall match the MASTER InfoField Partial Frame Count for the aligned frame.

Upon entering TRAINING state the SLAVE initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the SLAVE sets timing_lock_OK = 1.

Annex 98B

(normative)

IEEE 802.3 Selector Base Page definition

98B.1 Introduction

This annex provides the Technology Ability Field bit assignments, Priority Resolution table, and Message Page transmission conventions relative to the IEEE 802.3 Selector Field value within the Base Page encoding.

As new IEEE 802.3 LAN technologies are developed, a reserved bit in the Technology Ability field may be assigned to each technology by the standards body.

The new technology will then be inserted into the Priority Resolution hierarchy and made a part of the Auto-Negotiation standard. The relative hierarchy of the existing technologies will not change, thus providing backward compatibility with existing Auto-Negotiation implementations.

It is important to note that the reserved bits are required to be transmitted as logic zeros. This guarantees that devices implemented using the current priority table will be forward compatible with future devices using an updated priority table.

98B.2 Selector field value

The value of the IEEE 802.3 Selector Field is S[4:0] = 00001.

98B.3 Technology Ability Field bit assignments

The Technology bit field consists of bits D21 through D47 (A0–A26, respectively) in the IEEE 802.3 Selector Base Page. Table 98B–1 summarizes the bit assignments. Note that the order of the bits within the Technology Ability Field has no relationship to the relative priority of the technologies.

Table 98B–1—Technology Ability Field bit assignments

bit	Selector description
A0	RESERVED for 100BASE-T1 ability
A1	RESERVED
A2	1000BASE-T1 ability
~~A3~~	~~1000BASE-T1 EEE ability~~

98B.4 Priority Resolution

Since a local device and a link partner may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest.

— ~~1000BASE-T1 EEE~~
— 1000BASE-T1
— 100BASE-T1

98B.5 Message Page transmission convention

Each series of Unformatted Pages shall be preceded by a Message Page containing a message code that defines how the following Unformatted Pages will be used.

Next Page message codes should be allocated globally across Selector Field values so that meaningful communication is possible between technologies using different Selector Field values.