On Symbol Mapping For 1000BASE-T1

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Supporters

Agenda

- Considerations of Mapping
- Mapping Schemes
- FEC Requirements
- Clock Content
- Baseline Wander
- Discussions

Considerations of Mapping

- Bandwidth efficiency
  - Power increases with Baud Rate.
  - BW needs to be smaller than 500MHz to avoid potential RFI in the future.
- Clock Content
  - Clock can only be recovered with sufficient signal transitions. Lack of clock content leads to larger clock jitter.
  - Clock jitter affects error performance: echo cancellation and signal equalization.
- Baseline Wander
  - Larger baseline wander requires longer DFE feedback.
    - The difficulties of implementing DFE with large number of taps are often under estimated.
    - Cause more error propagation.
  - Increased signal dynamic range and increased power consumption.

Mapping Schemes

Mapping Schemes	Bandwidth Efficiency	Error Propagation Control	Run Length	Decision Distance	Complexity
7T11B	99%	No	12	0 dB	LUT of 2048 entries
2T3B	94.6%	No	Infinity	-0.5dB	LUT of 8 entries
7T10B	90.1%	6dB	4 for “+-1” 6 for “0”	-0.07dB	2 LUT of 8 entries

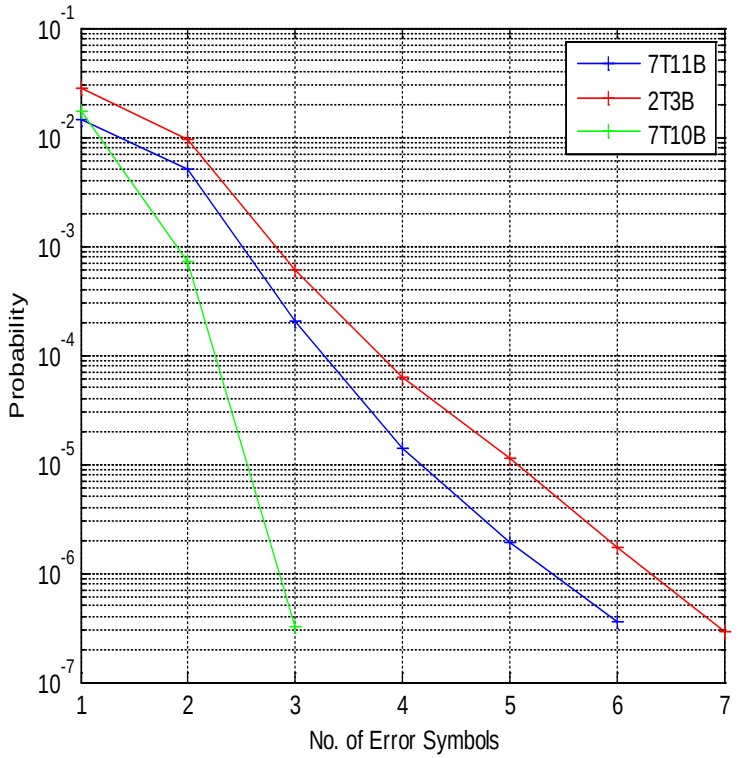
FEC Requirements

- RS codes.
- If connector interruption (>7ohm impedance) is not an issue, consider codeword length<300ns.
- A single error correction is sufficient for ISO 7637-3 transient noise [xiaofeng_3bp_02_0514].
- RFI dictates coding requirements.
  - Determine the required correction capability *t* as the maximal burst error length within a codeword at probability <Number_of_bits_per_codeword*1e-10.

Error Performance Under RFI

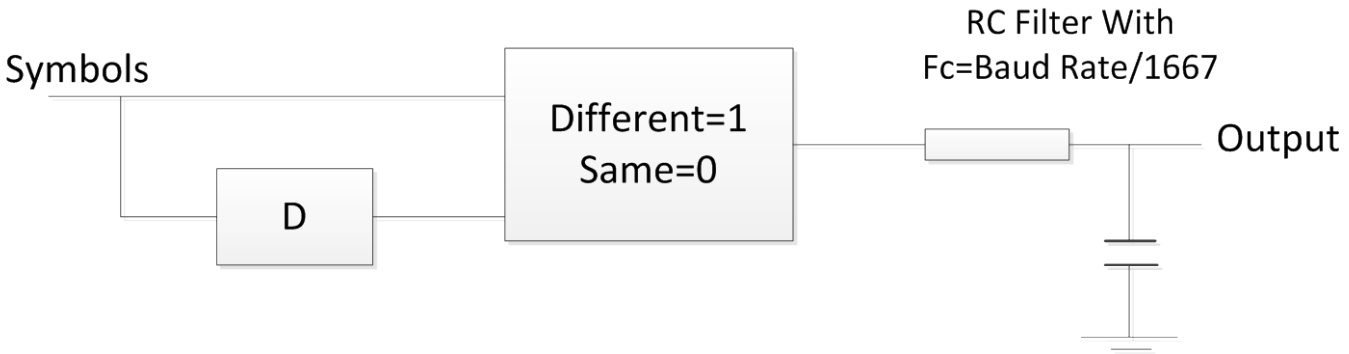
- DFE Tap B(n)=[0.6484 0.0978 -0.0452 -0.1192 -0.1232 -0.1309 -0.1196 -0.1166 -0.1050 -0.1000 -0.0898 -0.0845 -0.0758 -0.0708 -0.0634] for 2m channel at room temperature.
- RFI peak to peak amplitude =0.70 vs. eye height =1.
- RFI frequency at 0.47fb with fb as symbol rate.
- Codeword length 255.

Mapping Scheme	Required t	Coding Efficiency
7T11B	7	0.94
2T3B	8	0.933
7T10B	4	0.965

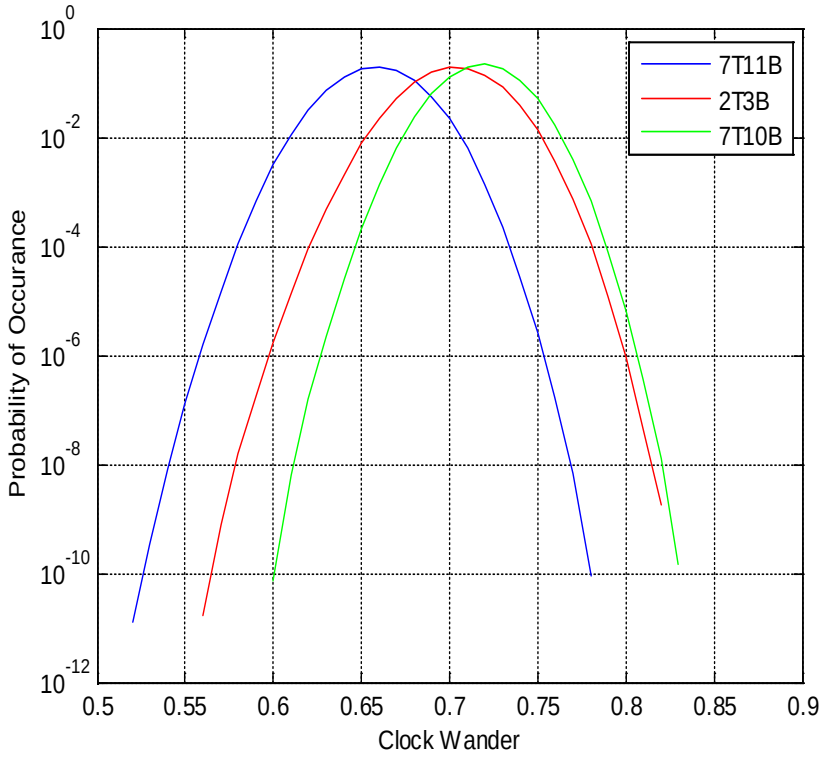


Clock Content

- Use OIF definition of “clock wander” as a metric of clock content, see http://www.oiforum.com/public/documents/OIF_WP_CEI_Short_Stress_Patterns.pdf
  - The Golden PLL with fc=Baud rate/1667 is appropriate for the purpose here (clock around 100ppm).
  - For PAM-3, make no distinction between signal levels in evaluating clock wander.

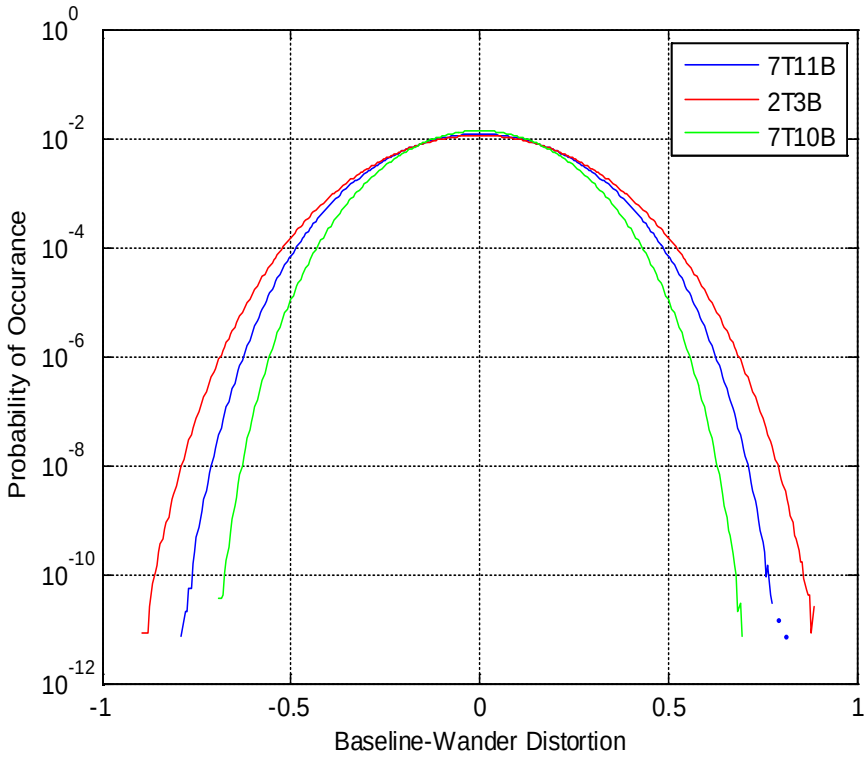


Clock Content II



- 7T10B provides the most clock content and 7T11B has the poorest clock content.
- At 1e-10, 7T10B has a 0.6 dB gain over 2T3B and 1.1 dB over 7T11B.

Baseline Wander



- Consider the instantaneous offset caused by an HPF with cutoff frequency at 10MHz.
  - Symbols take values {-1, 0, 1}.
- At 1e-10, 7T10B has 1dB less baseline wander distortion than 7T11B and 2.1dB less baseline wander distortion than 2T3B.
  - If allow truncation at 1e-12, the dynamic range of 7T10B is 0.5dB less than that of 7T11B and 1dB less than that of 2T3B.

Summary

Mapping Schemes	Bandwidth Efficiency With Coding	Clock Content @1e-10	Baseline Wander Distortion @1e-10
7T11B	93.2%	0.525	0.76
2T3B	88.3%	0.565	0.86
7T10B	87.0%	0.602	0.68

All three mappings can be accommodated within 750M Hz!

Discussions

- Symbol mapping affects bandwidth efficiency, clock, and baseline wander.
- 7T10B has the least bandwidth efficiency, 6.2% loss over 7T11B 1.3% over 2T3B, but provides the most signal transitions and less baseline wander distortion.
- Projected increase of power consumption of 7T10B due to bandwidth efficiency may well be made up by reduced implementation complexity due to desired signaling properties.
- At current stage, it is desirable to leave room for clock recovery implementation and jitter that have not been specified.