Answer To PoDL Questions

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1000 BASE-T1 – PoDL Liason Activities

- Dave Dwelley Presented PoDL liason Response to 1000BASE-T1 in May [dwelley_3bp_01a_0514.pdf].
- A list of questions were presented to 1000BASE-T1.

Response

Q1. There are two noise sources to be considered in PoDL – one in the PSE and one in the PD, located at either end of the cable. Does the 1000BASE--T1 group anticipate additonal effects due to this?

R1. The PoDL noise limit proposed in [wang_3bu_1_0514.pdf or xiaofeng_3bp_01_0514.pdf] will remain unchanged. There is a 6dB margin given in the calculation.

Q2. The effects of common mode noise and broadband noise generated by PoDL on data integrity should be considered and specified by 1000BASE--T1.

R2. Need more study on the effects of common mode noise on receiver performance and EMI.

The broadband noise at frequency greater than 10MHz measured before the coupling network at the supply side shall be less than -130dbm/Hz.

Response II

Q3. The PHY transmitter droop time and the HPF specification don't seem to agree. Additionally, the droop time spec doesn't seem to include insertion loss or return loss specs. Can we resolve this apparent discrepancy or modify or eliminate the droop time spec?

R3. The droop time will be determined by the HPF external to the chip associated with transformer or AC coupling cap, whichever will be used. The HPF that is used to filter PoDL noise is internal to the chip.

Transmit droop time for 1000BASE-T1 and receive HPF for filtering PoDL noise for 1TPCE are yet to be defined.

Q4. PoDL may affect the DC offset at the PHY receiver. PoDL would like to ignore this effect. Presumably the PHY transmitter can correct for this. Can we assume that DC correction will be handled in the 1000BASE---T1 PHY? – What is a reasonable limit on DC correction?

R4. Need clarifications of the cause of DC offset due to PoDL.

Response III

Q5. What is the tolerance of the PHY receiver to dVphy/dt as a result of PoDL noise?

R5. Set at 20dB below required RFI immunity. Given 200mVpp @10MHz, dv/dt=2*pi*1e7*10mV=0.63V/us.

Q6. Is 7dBmV stationary noise limit (from gardner_3bu_1_0514.pdf) a reasonable assumption?

R6. It's desirable to limit the stationary noise above 10MHz at -130dbm/Hz or 7dBmV. Noise below 10MHz shall meet proposed PoDL noise limit.