97.1.2 Relationship of 1000BASE-T1 to other standards

Relations between the 1000BASE-T1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 97-1. The PHY sublayers (shown shaded) in Figure 97-1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 1000BASE-T1 is defined in Clause 98. GMII is defined is Clause 35.

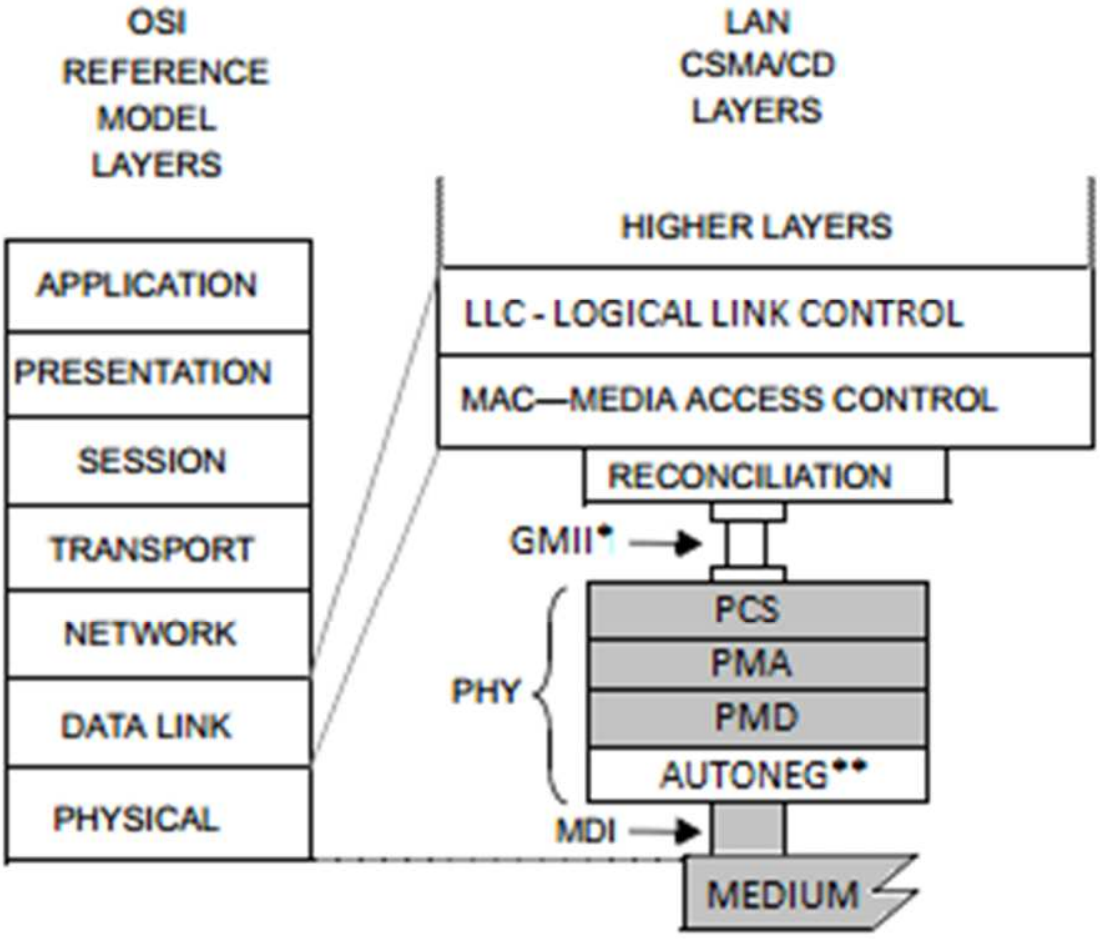


Figure 97-1 Relationship of 1000BASE-T1 PHY to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN Model

MDI = MEDIUM DEPENDENT INTERFACE
GMII = GIGABIT MEDIA INDEPENDENT INTERFACE
AUTONEG = AUTO-NEGOTIATION
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

* GMII is optional
** AUTONEG is optional

97.1.3 Operation of 1000BASE-T1

The 1000BASE-T1 PHY operates using full-duplex communications (using echo cancellation) over a single pair of balanced copper cabling with an effective rate of 1 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive and industrial environments . The PHY supports operation on two types of link segments:

a) An *automotive link segment* supporting up to four inline connectors using unshielded balanced copper cabling for at least 15 meters (referred to as *link segment type A).*
b) An *additional link segment* supporting up to four inline connectors using balanced copper cabling for at least 40 meters to support applications requiring additional physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus and heavy trucks). This link segment is referred to as *link segment type B.*

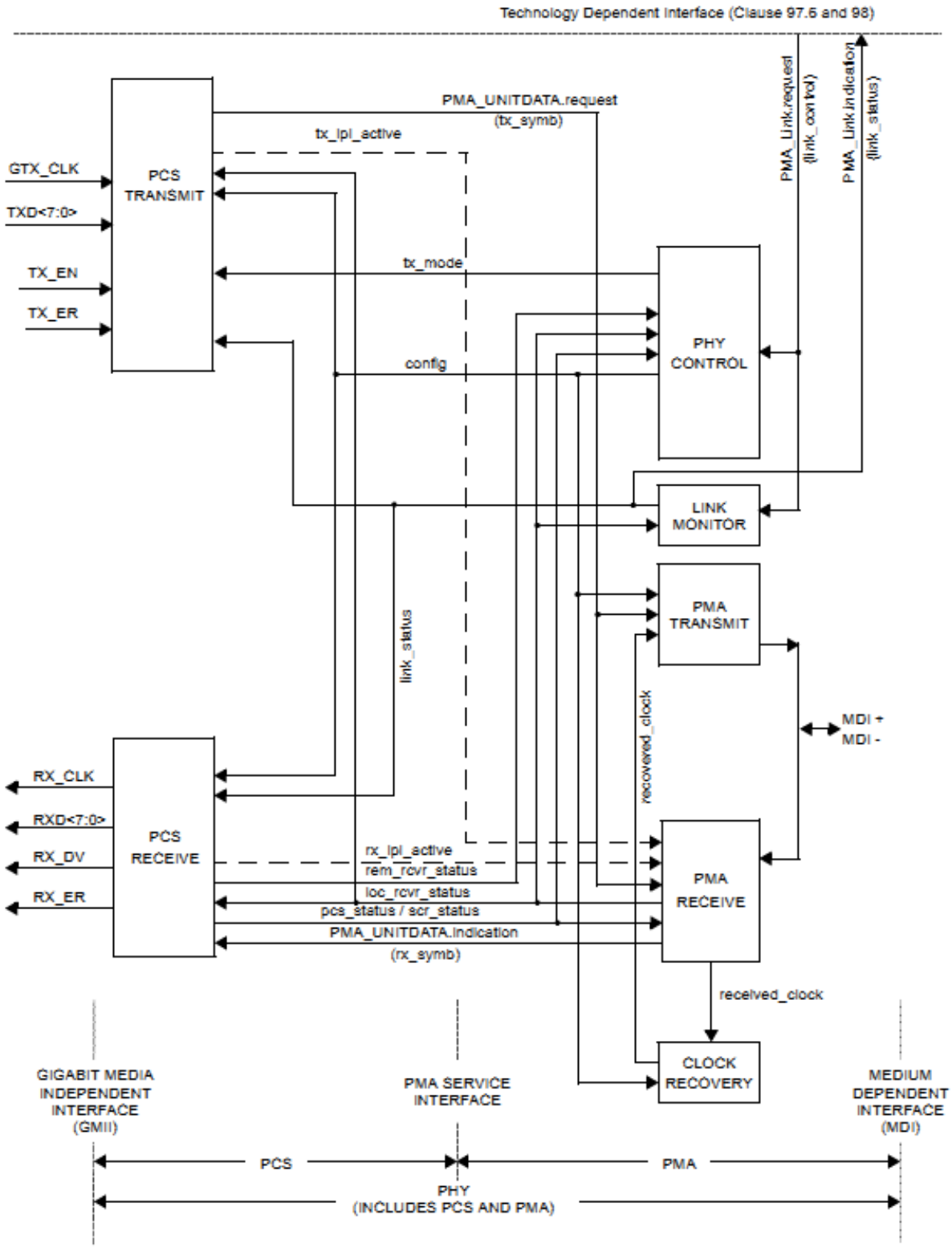
The 1000BASE-T1 PHY utilizes 3 level Pulse Amplitude Modulation (PAM3) transmitted at a 750 MHz rate. A 15-bit scrambler is used to improve the EMC performance. GMII TX_D, TX_EN, and TX_ER are encoded together in using 81B encoding where 10 cycles of GMII data and control are encoded together in 81 bits to reduce the overhead. To maintain a bit error ratio (BER) of less than or equal to 10^{-10}, the 1000BASE-T1 PHY adds a 396 bit Reed Solomon Forward Error Correction (RS FEC) code to each group of forty-five 81B blocks (containing 450 octets of GMII data). The PAM3 mapping, scrambler, RS FEC, and 81B encoder/decoder are all contained in the PCS (see 97.3).

Auto-Negotiation (Clause 98) may optionally be used by 1000BASE-T1 devices to detect the abilities (modes of
operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of half-duplex
differential Manchester encoding.

A 1000BASE-T1 PHY can be configured either as a MASTER PHY or as a SLAVE PHY. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 98,). If Auto-Negotiation is not used, MASTER-SLAVE relationship is established by management or hardware configuration of the PHY, and the MASTER and SLAVE are synchronized by a PHY Link Synchronization function in the PHY (see 97.6).

A 1000BASE-T1 PHY may optionally support Energy Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 78.3. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 1000BASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management and PHY Control functions. The PMA provides full duplex communications at 750 MBd over the single pair of balanced copper cabling. PMA functionality is described in section 97.4. The PMD is described in section 97.5. The MDI is specified in 97.8



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

Figure 97-2 Functional Block Diagram

97.1.3.1 Physical Coding Sublayer (PCS)

The 1000BASE-T1 PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to
a Physical Medium Attachment (PMA) sublayer, described in 97.4, which supports communication over a single pair of balanced copper cabling.

The PCS comprises the PCS Reset function, PCS Transmit, and PCS Receive. The Transmit and Receive functions start immediately after completion of the Reset function and run simultaneously and asynchronously with relation to each other.

In Data Mode, the PCS Transmit function data path starts with the GMII interface, where TXD, TX_EN, and TX_ER input data to the PCS every 8ns (as clocked by GTX_CLK). Data and control from ten GTX_CLK cycles are encoded into an 81 bit "81B block" that encodes every possible combination of data and control (control signals include error propagation, assert low power idle, and inter-frame signaling). Each set of forty-five 81B blocks along with 9 bits of OAM data (see 97.7) processed by a Reed Solomon FEC encoder (RS FEC). The RS encoder adds 396 bits of FEC data and the 4050 bits (forty-five 81B blocks = 3645 bits, 9 bits of OAM, and 396 bits of FEC data) are scrambled using a 15-bit side-stream scrambler. Each 3 bits of the scrambled data is converted to 2 ternary PAM3 symbols by the 3B2T mapper (the 4050 bits in the RS frame become 2700 PAM3 symbols) and passed to the PMA. PCS transmit functions are described in 97.3.2.2.

In Data Mode, the PCS Receive function data path operates in the opposite order as the transmit path. The incoming PAM3 symbols are synchronized to frame boundaries. Within each frame, each two PAM3 symbols are de-mapped to 3 bits by the 3B2T demapper (the 2700 PAM3 symbols are converted to 4050 bits). The data is then descrambled and passed to the RS FEC decoder for data validation and correction. Finally, each of the forty-five 81B blocks is decoded into GMII data or control. PCS data mode receive is described in 97.3.2.3.

In Training Mode (detailed in 97.4.2.5), the PCS transmits and receives data sequences to synchronize the RS FEC blocks, learn the Data Mode scrambler seed, and exchange EEE and OAM capabilities. Training mode uses PAM2 encoding.

97.1.3.2 Physical Medium Attachment (PMA) sublayer

The 1000BASE-T1 PMA transmits/receives symbol streams to/from the PCS onto the single balanced twisted pair and provides the clock recovery, link monitor and the 1000BASE-T1 PHY Control function. The PMA provides full duplex communications at 750 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the start-up functions required for successful 1000BASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. Failure of the receive channel causes data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

97.1.3.3 Physical Medium Dependent (PMD) sublayer

The1000BASE-T1 PMD (see 97.5) defines the transmit and receive electrical characteristics. The PMD also specifies the minimum link segment characteristics, EMC requirements, and test modes.

97.1.3.4 EEE capability

NOTE: No change to text from draft 1.3.

97.1.3.5 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled to synchronize between the MASTER PHY and SLAVE PHY before training starts. Link Synchronization provides a fast and reliable mechanism for the link partner to detect the presence of the other, validate link, and start the timers used by the link monitor. Link Synchronization operates in a half-duplex fashion. Based on timers, the MASTER PHY sends a synchronization sequence for 1us. If there is no response from the slave, the MASTER repeats by sending a synchronization sequence every 5us. If the slave detects the sequence, it responds by responding with a synchronization sequence for 1us (after the MASTER has stopped transmitting). If no other detection happens after the slave response for 4us then Link Synchronization is successfully complete, link monitor timers are started, and the PHY Control state machine starts Training. Link synchronization is defined in 97.6

97.1.4 Signaling

1000BASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single pair of balanced copper cabling. The signaling scheme achieves a number of objectives including:

a) Algorithmic mapping from TXD<7:0> to PAM3 symbols in the transmit path.
b) Algorithmic mapping from PAM3 symbols to TXD<7:0> in the receive path
c) Adding FEC coded data to transmit and validating data using FEC on receive
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
g) Optionally, ability to signal to the remote PHY that transmit in entering the LPI mode or exiting the LPI mode and returning to normal operation.

The PHY may operate in three basic modes, normal mode, training mode, or an optional LPI mode. In normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA.
In training mode, the PCS is directed to generate only a PAM2 pattern with periodic embedded data which enables the receiver at the other end to train and synchronize timing, scrambler seeds, and capabilities. LPI mode is enabled separately in each direction (see LPI signaling in 97.3.5). When transmitting in LPI mode, the PCS is directed to generate zero symbols and periodically send a REFRESH pattern to keep the two PHYs synchronized (see 97.3.2.2.16).

97.1.5 Interfaces

All 1000BASE-T1 PHY implementations are compatible at the MDI and at a physically exposed GMII, if made available. Physical implementation of the GMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

97.1.6 Conventions in this Clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions.

Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementer.