Consensus building ideas for 1000BASE-T1

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Supporters

- **Tom Brown - Vitesse**

Objective

- **Build consensus on various topics so task force can focus its studies so we can converge on a solution sooner**

Consensus So Far

- PAM3 modulation
  - Tazebay_3bp_01a_0314.pdf
- 25 MHz friendly baud rate
  - Lo_3bp_01_0314.pdf
- 8N/(8N+1) encoding and scrambling
  - Lo_3bp_02_0314.pdf
- Some form of block FEC
  - i.e. Reed Solomon, LDPC

Suggestion #1 – PAM2 Training

- **Better SNR**
- **Faster training**

- **We can leverage training ideas from Clause 55 (10GBASE-T) or Clause 72 (10GBASE-KR). Both are using PAM2.**

Suggestion #2 – Simplify Startup

- **Preference is to avoid use of PBO or THP**
  - **100ms to link up. Transferring coefficients and readapting slows things down.**
- **If shaping is required used a single fixed setting**
  - **Worst case scenario limit to choice of a few predetermined fixed settings**

Suggestion #3 – Self Contained FEC Block

- Integer number of 8N/(8N+1) blocks fit into one FEC block
- Integer number binary to PAM 3 conversions per FEC block
  - (i.e. 11 binary bits to 7 ternary symbol mapping is one conversion)
  - (i.e. 3 binary bits to 2 ternary symbol mapping is one conversion)
- Above would simplify things as the internal alignment of one FEC block do not differ from another
- Startup sequence can be based on units of FEC block time
  - When startup is done FEC block boundary is known
- EEE timing can also be based on FEC block time
  - Start and stop traffic cleanly on FEC boundary

Suggestion #4 – Best if baud rate can be 700MHz

	MHz	Overhead
Theoretical PAM3	631	0.0%
Theoretical PAM3 + 10%	694	10.0%
28 x 25MHz	700	10.9%
29 x 25MHz	725	14.9%
30 x 25MHz	750	18.9%

- **700MHz closest to 10% overhead and 25MHz friendly**
- **Lower baud rate ➔ lower power and lower EMI**
- **8N/(8N+1) encoding would need N>8 to be more bandwidth efficient**
- **Binary to Ternary encoding need to be efficient**
- **Give as much of the overhead to FEC parity bits**
- **Don't waste any bandwidth for FEC block alignment markers – align during training instead**

Suggestion #4 – Best if baud rate can be 700MHz (continued)

- **Don't neglect power when considering FEC performance, latency, baud rates, PAM3 mapping**
- **Power is analog dominated**
  - **Survey of recent process node 1000BASE-T and 10GBASE-T PHYs:**
  - **60% to 90% analog, 40% to 10% digital**
  - **Assume average for 1000BASE-T1: 75% analog, 25% digital**
- **Power optimization tradeoff**
  - **Simplify analog (i.e. run as slow as possible)**
  - **More complex digital**

Suggestion #5 – Tie FEC proposals to line baud rate

- Number of FEC parity bits cannot be unbounded
- FEC with higher % parity bits usually look better
  - Better performance
  - Better burst protection
- Higher % parity bits ➔ higher line baud rate ➔ more power

- Suggest that all presentations on FEC also explictly list out the assumed line baud rate so task force can make tradeoffs

Suggestion #6 – FEC burst correction performance to around 100 ns

- Related to FEC parity bits cannot be unbounded (#5)
- Worst transient noise seen at the receiver is less than 50ns
  - Chini_Tazebay_3bp_01a_0114.pdf
- Assumption of internal transient error propagation in DSP is 200 ns in some discussions
  - Is this too pessimistic?
  - Is this too limiting on the FEC solution space?
- Suggest that we reduce this to something around 100 ns
  - Otherwise latency may get too long or
  - Line bandwidth increase unnecessarily

Motion

Move that 1000BASE-T1 PHY training use PAM2.

M: William Lo S:

Y: N: A:

MOTION (Technical >=75%)

THANK YOU