802.3bp 1000BASE-T1
PHY Ad Hoc F2F Meeting

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Objectives

1. **Need to converge on critical baseline PHY proposals before the next plenary in July, 2014.**

2. **Goal is to create consensus on possible topics (which are listed in this document). Anybody who wants to contribute is welcome**

3. **Develop a multi-vendor proposal based on #2 by 07/14**

Transmitter Specification

Topics	Options/ Assumptions	Consensus	Action Item
PSD Upper Mask			
PSD Lower Mask			
Transmit Pre-filtering	Define it or leave it to the vendor?		
Frequency Tolerance	+/- 100ppm		
Electrical Tests & corresponding modes	(Jitter, droop, pulse template, etc.)		

FEC ←→Line Coding & Mapping

Topics	Options/ Assumptions	Consensus	Action Item
Maximum burst protection	100 ns, 200 ns, 400 ns?	Tentative	
Latency	4 us and 8 us	Tentative	
Line Coding & Mapping → Baud rate	3 different proposals?		
FEC Proposal	RS	Agreed	

PHY Control

Topics	Options/ Assumptions	Consensus	Action Item
Loop timing	Master/Slave	Agreed	
Training Mode	PAM2, PAM3? Start-up PAM2 power?		
Startup training	Blind or Training Sequence (1000BASE-T or 10GBASE-T model)?		
Convergence time			
Convergence robustness in noise			

Receiver Specification

Topics	Options/ Assumptions	Consensus	Action Item
Frequency Tolerance	+/- 100ppm?		
Jitter Tolerance			
Interference Tests	EMC, simulated PoDL, Crosstalk		
Test Channel models for the above tests			
IC level EMC testing	DPI, 150-Ohm emissions?		
Component Level Testing	Differential CW test setup & procedure?		

EEE Mode*

Topics	Options/ Assumptions	Consensus	Action Item
Sleep, Deep Sleep and Fast Wake Modes	Re-training time?		
Asynchronous mode			
Robustness in noise			
LPI	Is it needed? Shall we consider a different mapping for LPI mode? Simple PAM3?		

* What does EEE mean for automotive?
* Would be easier once PAM3 mapping and start-up procedure is defined

Management Registers

Topics	Options/ Assumptions	Consensus	Action Item
Diagnostic Registers	What to report?		
Configuration Registers	Loopbacks, test modes, speed select, Master/Slave?, FEC mode		
Status Registers	Link status, loc_rcvr_status, rem_rcvr_status, scrambler lock, block lock, signal quality indicator [1-5], etc?		

Proposals are needed by 07/14

- **Specify N for the 8N/(8N+1) Encoder**
- **Specify FEC parameters**
  - **Data, Parity bits, symbol size**
  - **Theoretical minimum latency**
  - **Burst correction performance**
  - **Coding gain under NBI @ frequency TBD**
- **Specify PAM3 mapping scheme**
- **Specify Baud rate**
- **Specify how 8N/(8N+1) blocks and PAM3 mapping fit into FEC block**