Proposed Changes to Clause 45 MDIO Registers for 1000BASE-T1

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Introduction

- 802.3bp D1.4 defines new MDIO registers:
  - 1.2304 to 1.2308 for PMA/PMD
  - 3.2304 to 3.2317 for PCS
  - 7.512 to 7.525 for Clause 98
- Conflicts with existing registers, examples:
  - PMA/PMD reset 1.0.15 vs. 1.2304.15 vs. Table 97-5
  - Low-power mode 1.0.11 vs. 1.2304.11
  - PCS reset 3.0.15 vs. 3.2304.15
  - PCS loopback 3.0.14 vs. 3.2304.14
- Using only isolated register blocks may cause complexity in management interface in multi-capability PHY
- Follow 802.3bw approach
  - Reuse basic control registers 1.0, 1.7, 1.11, 1.18, 3.0, etc.
  - Remove redundant control bits in 802.3bp register blocks

REGISTER 1.7

Includes all BASE-T1

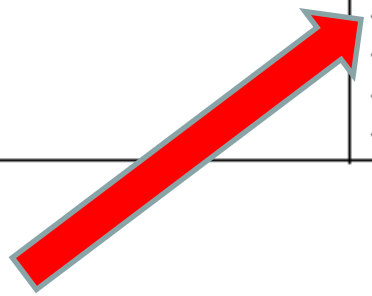
45.2.1.7 PMA/PMD control 2 register (Register 1.7)

Replace indicated line in the 1.7.5:0 row of Table 45-4 with five new lines, as follows (unchanged lines not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 ~~1 1 x x x x = reserved for future use~~ 1 1 1 1 1 x = reserved for future use 1 1 1 1 0 1 = 100BASE-T1 PMA/PMD 1 1 1 1 0 0 = reserved for future use 1 1 1 0 x x = reserved for future use 1 1 0 x x x = reserved for future use	R/W

[a]R/W = Read/Write



Redefine 111101 = BASE-T1 PMA/PMD

REGISTER 1.11 AND 1.18

Reuse Register 1.11 from 802.3bw

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change the reserved row in Table 45-13, and insert a new row immediately below the changed row as follows (unchanged rows not shown):

Table 45–14—PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.15:~~11~~ 12	Reserved	Value always 0	RO
1.11.11	BASE-T1 extended abilities	1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1 extended abilities	RO

[a]RO = Read only

Insert 45.2.1.10.a before 45.2.1.10.1 as follows:

45.2.1.10.a BASE-T1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1 extended abilities.

Add 1000BASE-T1 to Register 1.18

Table 45-16a PMA/PMD extended ability register bit definitions

Bits (s)	Name	Description	R/W
1.18.15:2	Reserved	Set to 0s	RO
1.18.1	1000BASE-T1 ability	1=PMA/PMD is able to perform 1000BASE-T1 0=PMA/PMD is not able to perform 1000BASE-T1	RO
1.18.0	100BASE-T1 ability	1=PMA/PMD is able to perform 100BASE-T1 0=PMA/PMD is not able to perform 100BASE-T1	RO

REGISTER 1.2304

Original Table 45-98a

Bits (s)	Name	Description	R/W	Comments
1.2304.15	Reset	1=PMA/PMD reset 0=Normal operation	R/W, SC	Use 1.0.15
1.2304.14:12	Reserved	Set to 0s	R/W	Following 1.2100
1.2304.11	Low power	1=Low-power mode 0=Normal operation	R/W	Use 1.0.11
1.2304.10:5	Reserved	Set to 0s	R/W	
1.2304.4	Master/Slave	1=Master 0=Slave	R/W	Following 1.2100
1.2304.3:0	PHY Type	Base-T1 PHY speed when Auto-negotiation is disabled 0000=Reserved 0001=reserved 0010=1000BASE-T1 Else=Reserved	R/W	Consolidate with 1.2100

Revised Table 45-98a

Table 45-98a 1000BASE-T1 PMA Control Register

Bits (s)	Name	Description	R/W
1.2304.15	Force Mode Enable	1=Enable force mode 97.6 0=Enable autoneg CL98	R/W
1.2304.14	Master/Slave	1=Configure PHY as Master 0=Configure PHY as Slave	R/W
1.2304.13:4	Reserved	Set to 0s	R/W
1.2304.3:0	PHY Type	Base-T1 PHY speed when Auto-negotiation is disabled 1xxx=Reserved 01xx=Reserved 001x=Reserved 0001=1000BASE-T1 0000=100BASE-T1	

Proposed Texts for register 1.2304

- Delete original 45.2.1.130a.1 to 45.2.1.130a.4

- 45.2.1.130a.1 1000BASE-T1 Force mode enable (1.2304.15)

Bit 1.2304.15 returns a one to indicate the PHY is in Force mode. In that case, Auto-Negotiation shall be disabled and the PHY Link Synchronization specified in 97.6 shall be enabled. Further, bit 1.2304.14 is used to determine if the PHY operates as MASTER or SLAVE. When this bit returns a zero then it indicates the PHY is not in Force mode and Auto-Negotiation is enabled.

- 45.2.1.130a.2 1000BASE-T1 Master/Slave (1.2304.14)

When Force mode is enabled, this bit is used to configure the PHY to be master or slave. When set as a one the PHY is configured to be a master. When set as a zero the PHY is configured to be a slave. The setting of this bit shall be ignored when Auto-Negotiation is enabled.

- Move original 45.2.1.130a.4 as new 45.2.1.130a.3

REGISTER 3.2304

Proposed texts for register 3.2304

- Use 3.0.15 for PCS reset
- Use 3.0.14 for PCS loopback
- In Table 45-163a, set all bits (15:0) in register 3.2304 as reserved.
- Change 45.2.2.50a to:

45.2.2.50a 1000BASE-T1 PCS Control Register (Register 3.2304)

All bits in register 3.2304 shall be reserved and set to value 0.

- Delete 45.2.2.50a.1 and 45.2.2.50a.2.