Proposal for an OAM channel v.0.1

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Motivation

- Currently, 1000BASE-T1 has an additional throughput of 2.5Mbit/s data exchange capability during normal operation.
- This additional throughput can be used for additional control and status information exchange between the nodes and it is often called OAM (operations, administration and management) process.
- In order to utilize this additional capability interoperably, this is a proposal on how to use the data field so that all the PHY vendors can implement the same function.

Mapping	8n	8n+1	RS m	RS N	RS K	FEC rate	OAM bits	RS N-K	FEC Block ns	Correction ns	FEC latency ns	OAM Mbps
3B2T	80	81	9	450	406	0.902	9	44	3600	176.00	3952.00	2.50

Data of interest

Diagnostics

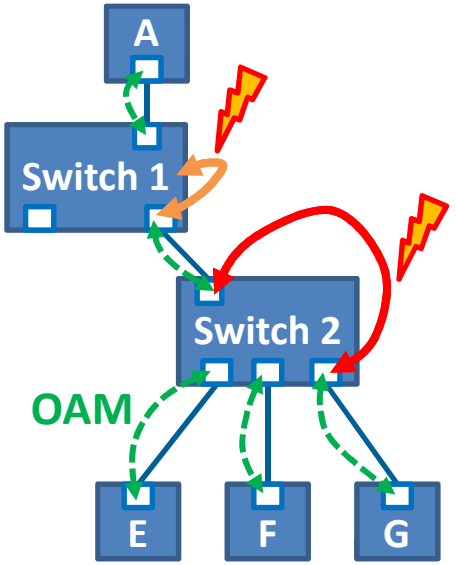
- Signal To Noise Ratio (SNR)
- MIB register information
  - Frame loss ratio
  - Additional MIBs on request via a “getMIB” instruction set
- Remote failure indication
  - Loopback tests to identify if end nodes are “alive”
  - Cable diagnosis

Network control data

- Network management
- Control of subsequent switches (Start-up and Shutdown, support of wake-up)

Restrictions

Functional



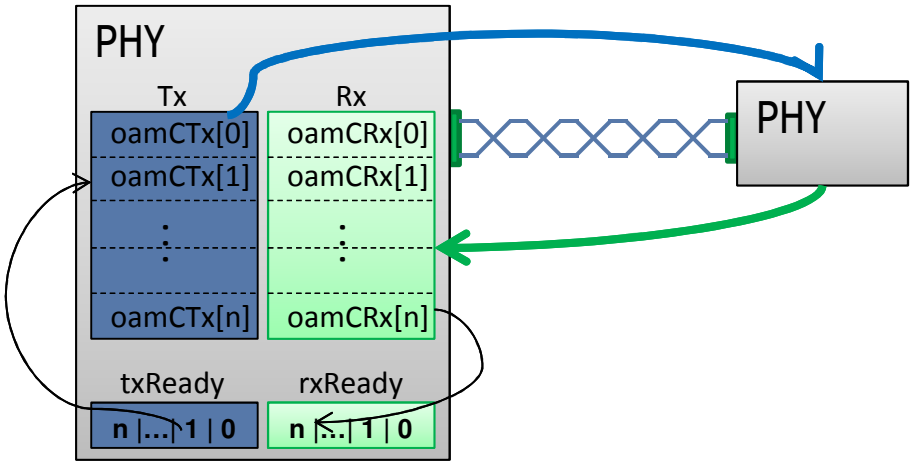
- OAM channel shall only use data that is accessible by the PHY. **No (new) interface to MAC / switch**, e.g., to read out lost frames or MIB counters.
- Addressing scheme / propagation of data transmitted via the OAM channel should be defined by OEM. **No implicit routing** of OAM data by switch IP.

Timing

- Detailed definitions of OEM use can potentially cause delays of the overall timing of the 1000BASE-T1 project.

Proposal

- Provide generic OAM channel address space;
- With **n** (virtual) software accessible registers – each **b** bytes wide (**b** may be higher then actual PHY register width);
- Where each register is transmitted/mirrored atomically every **c** ms;
- Some registers & bits may be reserved (e.g., for SNR or NM).



Open issues

- Amount of available memory (**n*b**) and max. register width (e.g., **b** = 8 byte)
- Register access (e.g., via tx ready register if **b** > MDIO register width)
- Cycle time (e.g., 1 ms or 5 ms)
- Amount of
  - predefined/reserved registers (e.g., for SNR, NM),
  - registers for individual use
- Impact on EEE idle mode?
- Expectation that the same OAM channel is not possible for existing protocols (e.g., 100BASE-T1/TX)

Back up