PCS Transmit and Receive Bit Ordering for 1000BASE-T1

San Antonio, TX, USA

November 4, 2014

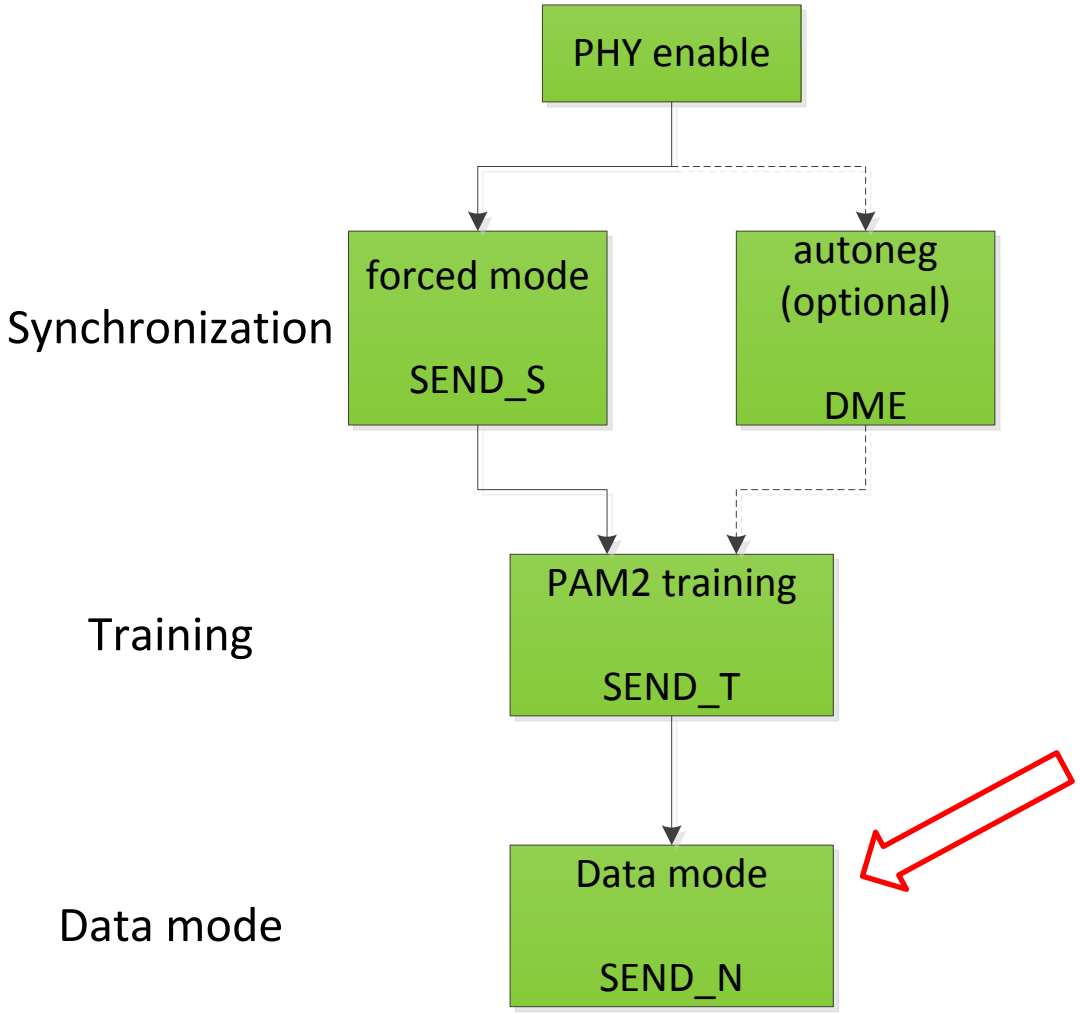
Mike Tu

tum@broadcom.com

Contributors

- Steven Chen
- Jim Graba
- Ahmad Chini
- Peiqing Wang
- BZ Shen
- Mehmet Tazebay

Overall Startup Sequence



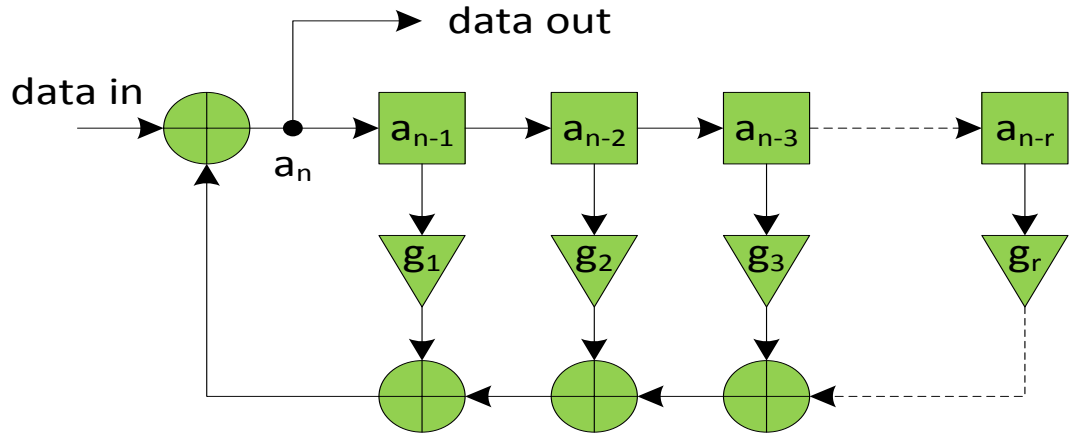
TX Mode	Definition
SEND_Z	Send all zeros
DME	Differential Manchester encoding for autoneg
SEND_S	Send special periodic PAM2 sequences with good correlation properties
SEND_T	Send PAM2 training sequence
SEND_N	Send normal data

Outline

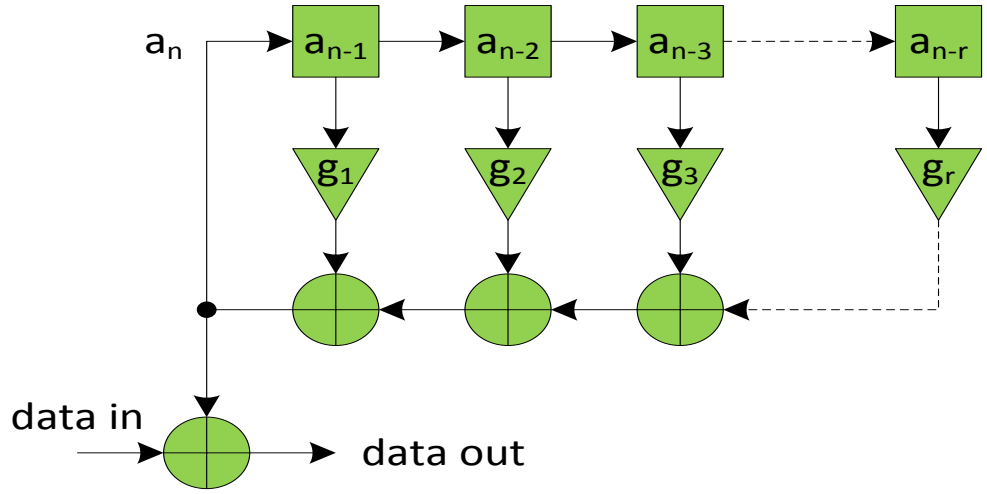
- FEC and PCS baseline passed in September Interim Meeting
  - RS (450,406,m=9)
  - PCS 80/81 encoding
  - 9-bit OAM
  - Bit ordering
  - 3B2T mapping
- Additional proposal
  - Choice of data mode scrambler
  - PCS transmit and receive bit ordering diagrams

Common Types of Scramblers

- Multiplicative scrambler
  - Also called self-synchronizing scrambler
  - Descrambler initial state not needed at receiver
  - Bit errors result in descrambler re-synchronization. FEC protection is required.

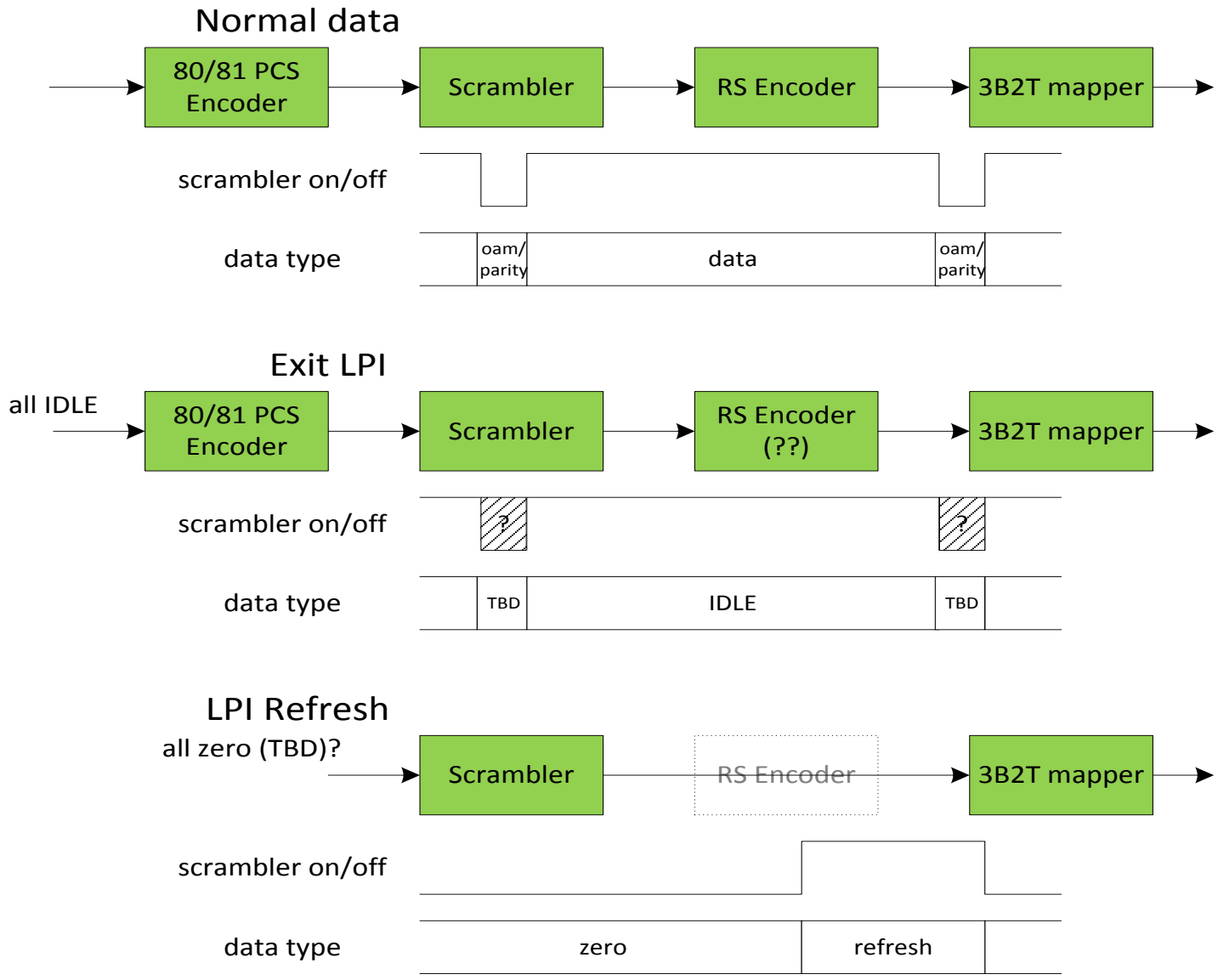


- Additive scrambler
  - Also called synchronous scrambler
  - Initial state must be specified and run continuously once started (no sync words)
  - Descrambler not affected by bit errors if clock timing remains locked
  - Proposal: exchange initial scrambler states during training



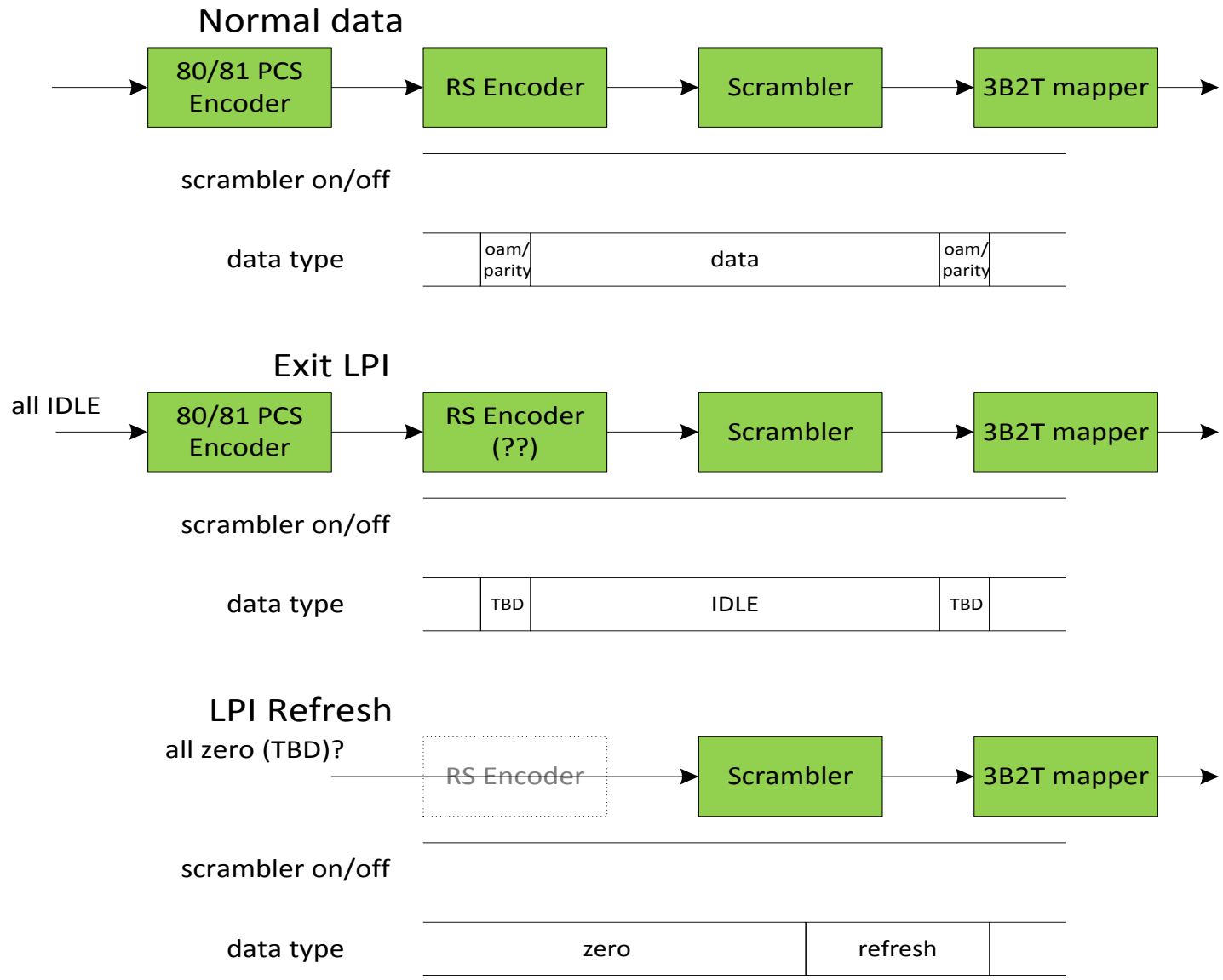
Scrambler Option #1

- Self-synchronizing scrambler before FEC encoder
- OAM symbol is not scrambled and consists of fixed pattern.
- In normal data the scrambler is ON during RS data symbols.
- When exiting LPI
  - No FEC protection during IDLE detection.
  - Bit errors might cause descrambler re-synchronization.
- In LPI REFRESH
  - Scrambler is ON at the end of frame.
  - Regenerating reference sequence is not easy under noisy condition.



Scrambler Option #2

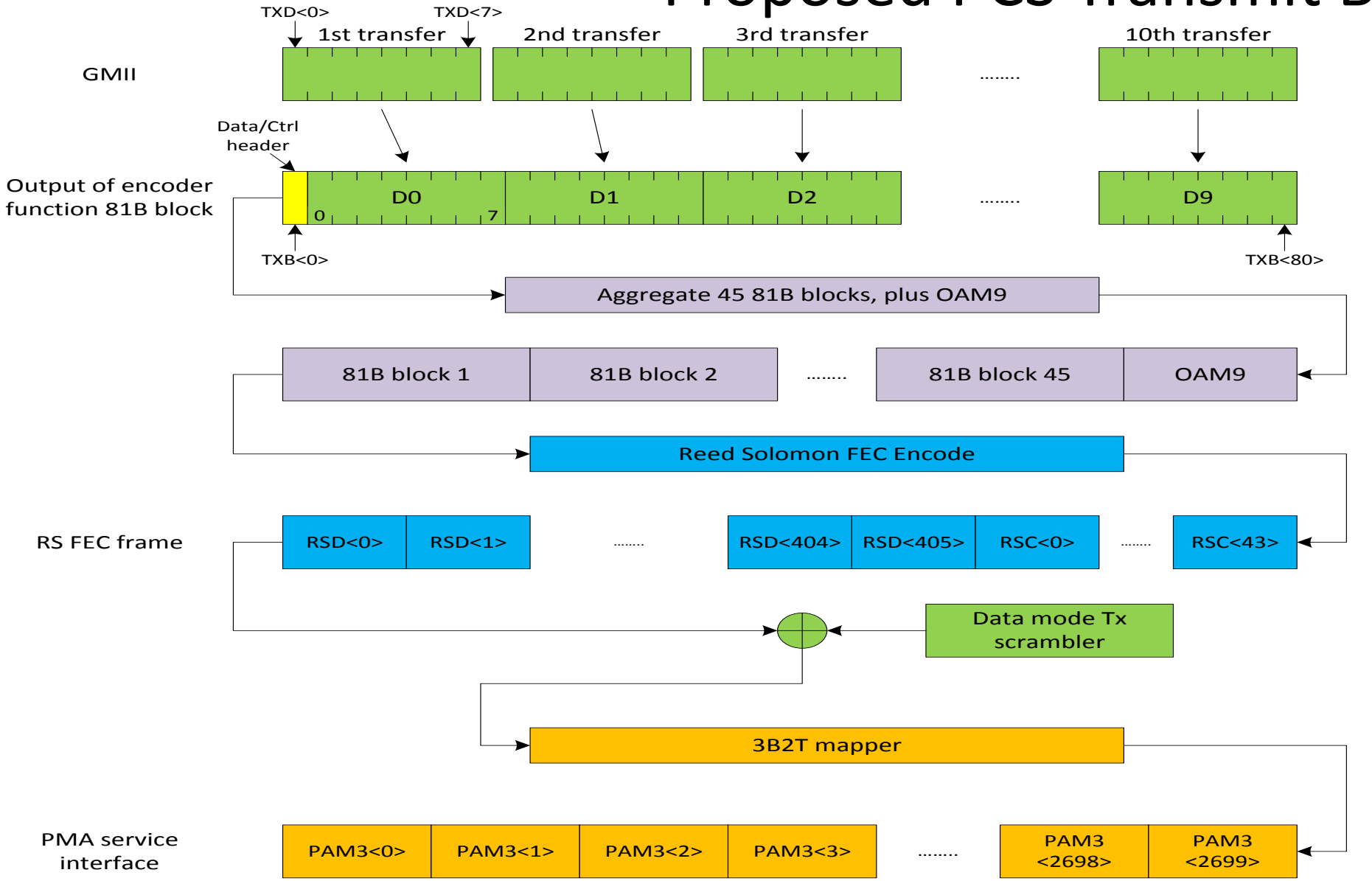
- Additive scrambler after FEC encoder
  - Initial scrambler states exchanged during training.
  - Scrambler is always enabled throughout normal data, exiting LPI, and LPI refresh.
- OAM symbol is scrambled.
- In LPI REFRESH
  - Reference sequence can be easily regenerated for improved performance.



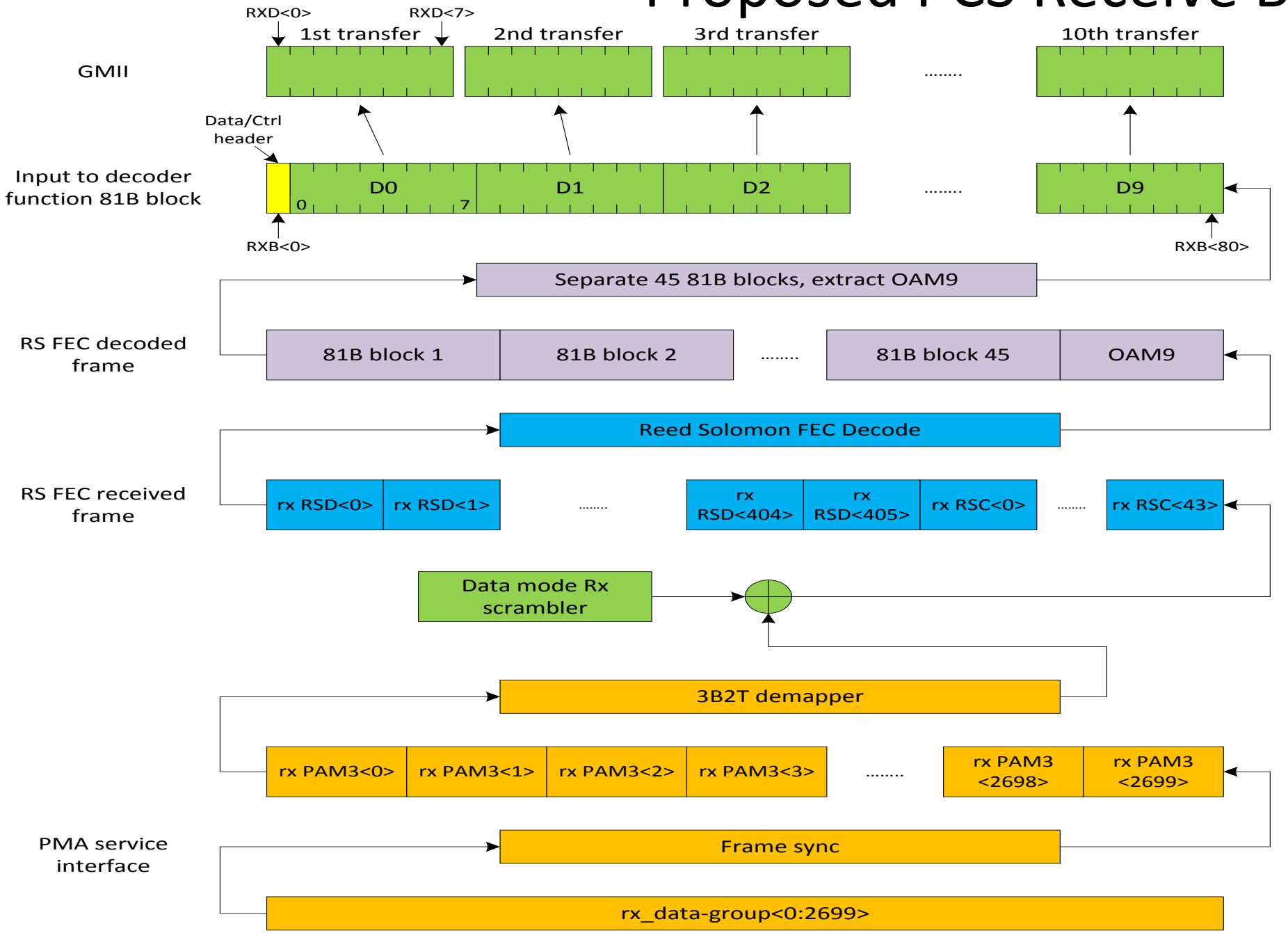
Proposal for Data Mode Scrambler

- Place scrambler after RS FEC encoder
- Use additive (synchronous) scrambler in data mode
- Exchange scrambler initial state and start time during training
- Once started, the scrambler shall run continuously throughout normal data and LPI

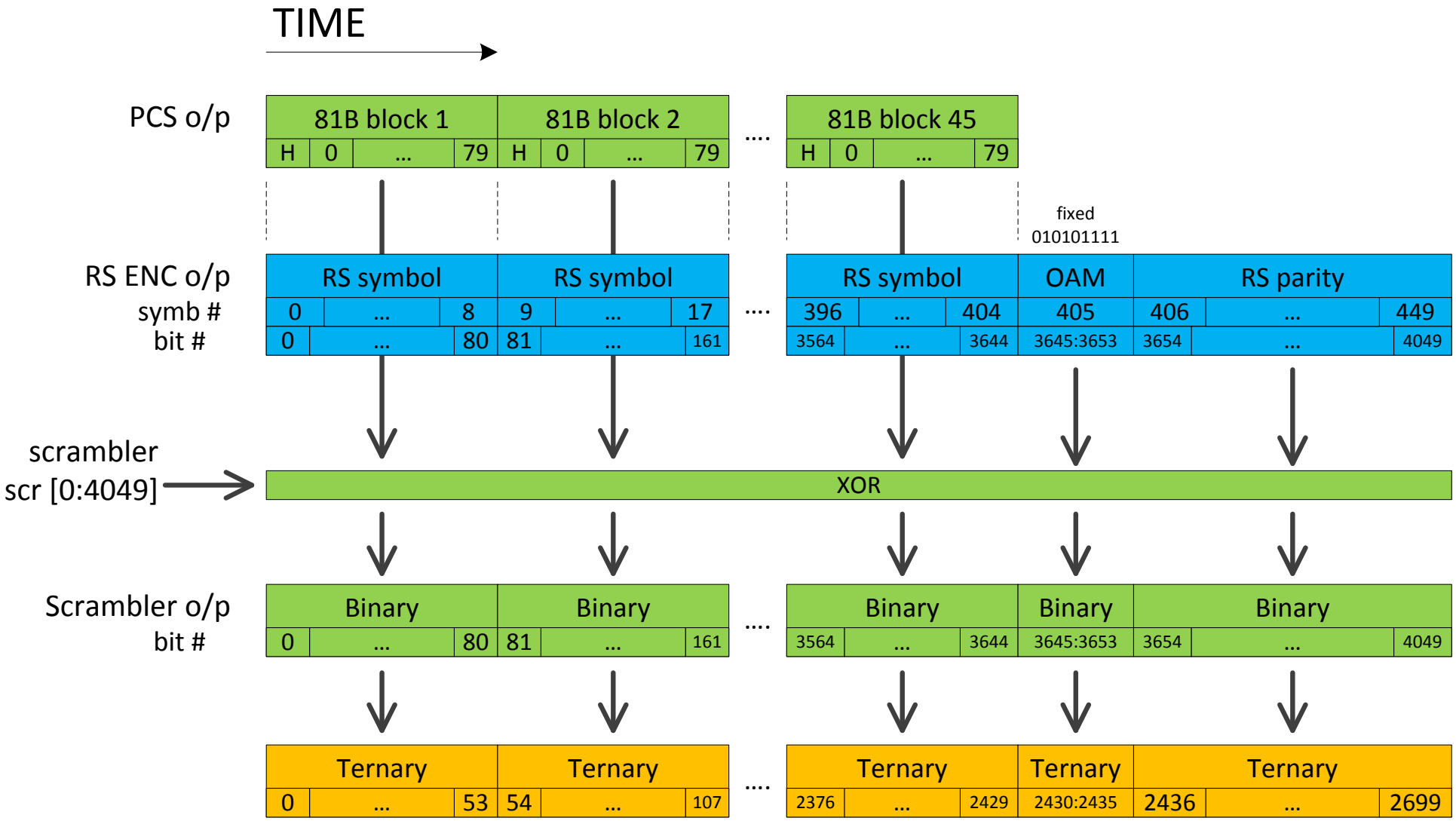
Proposed PCS Transmit Bit Ordering



Proposed PCS Receive Bit Ordering



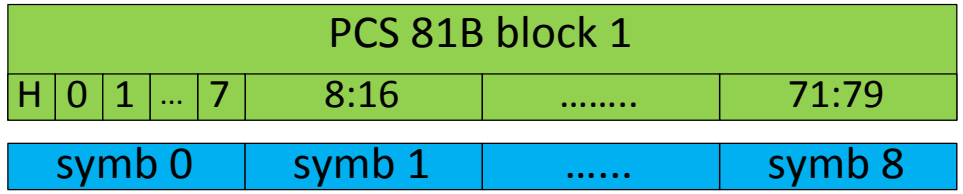
PCS Detailed Transmit Bit Ordering



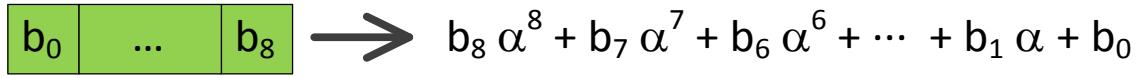
PCS Detailed Transmit Bit Ordering (cont.)

- For information ONLY.
- Previously adopted

PCS to FEC bit mapping



RS symbol over GF(2^9)



3B2T mapper

b2 b1 b0	T1, T0
000	-1, -1
001	0, -1
010	-1, 0
011	-1, +1
100	+1, 0
101	+1, -1
110	+1, +1
111	0, +1

- b0 is first bit
- T0 is transmitted first