Change value in "Support" cell for PICS MM126 as shown below. Insert PICS items MM128a through MM128s, as shown below.

45.5.3.3 PMA/PMD management functions

Item	Feature	Subclause	Value/Comment	Status	Support
MM126	Writes to the BASE-T1 PMA/PMD extended ability register have no effect	45.2.1.14b		PMA:M	Yes [ ] N/A~~o~~ [ ]
MM128a	A reset sets all 1000BASE-T1 PMA/PMD registers to their default states	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128b	1000BASE-T1 PMA/PMD returns a one in bit 1.2304.15 when a reset is in progress	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128c	1000BASE-T1 PMA/PMD returns a zero in bit 1.2304.15 when a reset is complete	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128d	The control and management interface is restored to operation within 0.5 s from the setting of bit 1.2304.15	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128e	During a reset, the 1000BASE-T1 PMD/PMA responds to reads from register bits 1.2304.15 and 1.8.15:14.	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128f	During a reset, the 1000BASE-T1 PMD/PMA register bits are ignored.	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128g	Setting either 1.2304.15 or 1.0.15 resets the 1000BASE-T1 PMA/PMD.	45.2.1.130a.1		PMA:M	Yes [ ] N/A [ ]
MM128h	When bit 1.2304.14 is set to a one, the PMA disables output on the transmit path.	45.2.1.130a.2		PMA:M	Yes [ ] N/A [ ]
MM128i	When bit 1.2304.14 is set to a zero, the PMA enables output on the transmit path.	45.2.1.130a.2		PMA:M	Yes [ ] N/A [ ]
MM128j	While in the low power mode, the device, as a minimum, responds to management transactions necessary to exit the low power mode.	45.2.1.130a.3		PMA:M	Yes [ ] N/A [ ]
MM128k	Setting either 1.2304.11 or 1.0.11 puts the 1000BASE-T1 PMA/PMD in low power mode.	45.2.1.130a.3		PMA:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
MM128l	The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path returns a value of zero for bit 1.2305.1.	45.2.1.130b.6		PMA:M	Yes [ ] N/A [ ]
MM128m	Bit 1.2305. is implemented with latching low behavior.	45.2.1.130b.6		PMA:M	Yes [ ] N/A [ ]
MM128n	Bit 1.2306.1 is set to 0 if the 1000BASE-T1 PHY does not support OAM.	45.2.1.130c.2		PMA:M	Yes [ ] N/A [ ]
MM128o	Bit 1.2306.0 is set to 0 if the 1000BASE-T1 PHY does not support EEE.	45.2.1.130c.3		PMA:M	Yes [ ] N/A [ ]
MM128p	OAM capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising OAM capability.	45.2.1.130d.2		PMA:M	Yes [ ] N/A [ ]
MM128q	EEE capability is enabled only when both the 1000BASE-T1 PHY and link partner are advertising EEE capability	45.2.1.130d.3		PMA:M	Yes [ ] N/A [ ]
MM128r	Bit 1.2100.14 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.131.2		PMA:M	Yes [ ] N/A [ ]
MM128s	Bits 1.2100.3:0 is ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.	45.2.1.131.3		PMA:M	Yes [ ] N/A [ ]

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Insert PICS items RM106a through RM106ae, as shown below.

45.5.3.7 PCS management functions

Item	Feature	Subclause	Value/Comment	Status	Support
RM106a	This action sets all 1000BASE-T1 PCS registers to their default states.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106b	Bit 3.2304.15 is self-clearing, and the 1000BASE-T1 PCS returns a value of one in bit 3.2304.15 when a reset is in progress.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106c	Otherwise, bit 3.2304.15 returns a value of zero	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106d	The control and management interface is restored to operation within 0.5 s from the setting of bit 3.2304.15.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106e	During a reset, the 1000BASE-T1 PCS responds to reads from register bits 3.2304.15 and 3.8.15:14.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106f	All other register bits are ignored during a reset.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106g	Setting either bit 3.2304.15 or 3.0.15 resets the 1000BASE-T1 PCS.	45.2.3.50a.1		PCS:M	Yes [ ] N/A [ ]
RM106h	The 1000BASE-T1 PCS is placed in a loopback mode of operation when bit 3.2304.14 is set to a one.	45.2.3.50a.2		PCS:M	Yes [ ] N/A [ ]
RM106i	When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS accepts data on the transmit path and return it on the receive path.	45.2.3.50a.2		PCS:M	Yes [ ] N/A [ ]
RM106j	Setting either bit 3.2304.14 or 3.0.14 enables loopback.	45.2.3.50a.2		PCS:M	Yes [ ] N/A [ ]
RM106k	All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register has no effect.	45.2.3.50b		PCS:M	Yes [ ] N/A [ ]
RM106l	Bit 3.2305.11 is implemented with latching high behavior.	45.2.3.50b.1		PCS:M	Yes [ ] N/A [ ]
RM106m	Bit 3.2305.10 is implemented with latching high behavior.	45.2.3.50b.2		PCS:M	Yes [ ] N/A [ ]
RM106n	Bit 3.2306.10 is implemented with latching high behavior.	45.2.3.50b.6		PCS:M	Yes [ ] N/A [ ]
RM106o	All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register has no effect.	45.2.3.50c		PCS:M	Yes [ ] N/A [ ]
RM106p	Bit 3.2306.7 is implemented with latching high behavior.	45.2.3.50c.4		PCS:M	Yes [ ] N/A [ ]
RM106q	Bit 3.2306.6 is implemented with latching high behavior.	45.2.3.50c.5		PCS:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
RM106r	Bits 3.2306.5:0 are reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset.	45.2.3.50c.6		PCS:M	Yes [ ] N/A [ ]
RM106s	Bits 3.2306.5:0 are held at all ones in the case of overflow.	45.2.3.50c.6		PCS:M	Yes [ ] N/A [ ]
RM106t	Bit 3.2308.15 is set to 1 when the OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted.	45.2.3.50d.1		PCS:M	Yes [ ] N/A [ ]
RM106u	Register 3.2308 is cleared by the state machine to indicate whether the next OAM message can be written into the registers.	45.2.3.50d.1		PCS:M	Yes [ ] N/A [ ]
RM106v	The state machine assigns a value alternating between 0 and 1 to associate with the 8 octet OAM message transmit by the 1000BASE-T1 PHY.	45.2.3.50d.2		PCS:M	Yes [ ] N/A [ ]
RM106w	Bit 3.2308.14 is read and recorded prior to setting 3.2308.15 to 1.	45.2.3.50d.2		PCS:O	Yes [ ] No [ ]
RM106x	Bit 3.2308.15 self clears when registers are loaded by the state machine.	45.2.3.50d		PCS:M	Yes [ ] N/A [ ]
RM106y	Bit 3.2308.14 self clears on read.	45.2.3.50d		PCS:M	Yes [ ] N/A [ ]
RM106z	Bit 3.2308.13 indicates whether the most recently transmitted OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner.	45.2.3.50d.3		PCS:M	Yes [ ] N/A [ ]
RM106aa	Bit 3.2308.13 clears on read.	45.2.3.50d.3		PCS:M	Yes [ ] N/A [ ]
RM106ab	Bit 3.2313.15 is set to 1 when the OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8.	45.2.3.50f.1		PCS:M	Yes [ ] N/A [ ]
RM106ac	Register 3.2313 is cleared when register 3.2317 is read.	45.2.3.50f.1		PCS:M	Yes [ ] N/A [ ]
RM106ad	Bit 3.2313.15 self clears when register 3.2317 is read.	45.2.3.50f		PCS:M	Yes [ ] N/A [ ]
RM106ae	Register 3.2313.15 is cleared when register 3.2317 is read.	45.2.3.50g		PCS:M	Yes [ ] N/A [ ]

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Insert PICS items AM60a through AM60y, as shown below.

45.5.3.9 Auto-Negotiation management functions

Item	Feature	Subclause	Value/Comment	Status	Support
AM60a	Setting bit 7.512.15 to a one sets all BASE-T1 AN registers to their default states.	45.2.7.14a.1		AN:M	Yes [ ] N/A [ ]
AM60b	Bit 7.512.15 is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise.	45.2.7.14a.1		AN:M	Yes [ ] N/A [ ]
AM60c	The reset process is completed within 0.5 s from the setting of bit 7.512.15.	45.2.7.14a.1		AN:M	Yes [ ] N/A [ ]
AM60d	During an AN reset, AN responds to reads from register bit 7.512.15.	45.2.7.14a.1		AN:M	Yes [ ] N/A [ ]
AM60e	All other register bits are ignored.	45.2.7.14a.1		AN:M	Yes [ ] N/A [ ]
AM60f	The Auto-Negotiation function is enabled by setting bit 7.512.12 to a one.	45.2.7.14a.2		AN:M	Yes [ ] N/A [ ]
AM60g	If bit 7.512.12 is set to one, then PHY type bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 has no effect on the link configuration, and the Auto-Negotiation process determines the link configuration.	45.2.7.14a.2		AN:M	Yes [ ] N/A [ ]
AM60h	If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 is zero.	45.2.7.14a.2		AN:M	Yes [ ] N/A [ ]
AM60i	If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD returns a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 are ignored.	45.2.7.14a.3		AN:M	Yes [ ] N/A [ ]
AM60j	Otherwise, the Auto-Negotiation process is restarted by setting bit 7.512.9 to one.	45.2.7.14a.3		AN:M	Yes [ ] N/A [ ]
AM60k	Bit 7.512.9 is self clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated.	45.2.7.14a.3		AN:M	Yes [ ] N/A [ ]
AM60l	If Auto-Negotiation was completed prior to this bit being set, the process is reinitialized.	45.2.7.14a.3		AN:M	Yes [ ] N/A [ ]
AM60m	The Auto-Negotiation process is affected by clearing this bit to zero.	45.2.7.14a.3		AN:M	Yes [ ] N/A [ ]

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Item	Feature	Subclause	Value/Comment	Status	Support
AM60n	All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register has no effect.	45.2.7.14b		AN:M	Yes [ ] N/A [ ]
AM60o	The Page received bit (7.513.6) is set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525.	45.2.7.14b.1		AN:M	Yes [ ] N/A [ ]
AM60p	The Page received bit is reset to zero on a read of the BASE-T1 AN status register (Register 7.513).	45.2.7.14b.1		AN:M	Yes [ ] N/A [ ]
AM60q	The BASE-T1 PMA/PMD returns a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12.	45.2.7.14b.2		AN:M	Yes [ ] N/A [ ]
AM60r	The BASE-T1 PMA/PMD also returns a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.	45.2.7.14b.2		AN:M	Yes [ ] N/A [ ]
AM60s	The remote fault bit is implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and remain set until it is cleared.	45.2.7.14b.3		AN:M	Yes [ ] N/A [ ]
AM60t	Bit 7.513.4 is cleared each time register 7.513 is read via the management interface, and is also cleared by a AN reset.	45.2.7.14b.3		AN:M	Yes [ ] N/A [ ]
AM60u	The link status bit is implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface.	45.2.7.14b.5		AN:M	Yes [ ] N/A [ ]
AM60v	Bit 7.513.2 is cleared upon AN reset.	45.2.7.14b.5		AN:M	Yes [ ] N/A [ ]
AM60w	A write to the BASE-T1 AN LP Base Page ability register has no effect.	45.2.7.14d		AN:M	Yes [ ] N/A [ ]
AM60x	On power-up or AN reset, registers 7.520, 7.521, and 7.522 contain the default value, which represents a Message Page with the message code set to Null Message.	45.2.7.14e		AN:M	Yes [ ] N/A [ ]
AM60y	A write to the BASE-T1 AN LP Next Page ability register has no effect.	45.2.7.14f		AN:M	Yes [ ] N/A [ ]

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