40GBASE-T Uncoded Bit Protection Proposal

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Objective

- **Propose an encoding to protect the uncoded bits without disturbing existing LDPC, 128DSQ, and 3200Mbaud/s**

Current Baseline – Based on 10GBASE-T

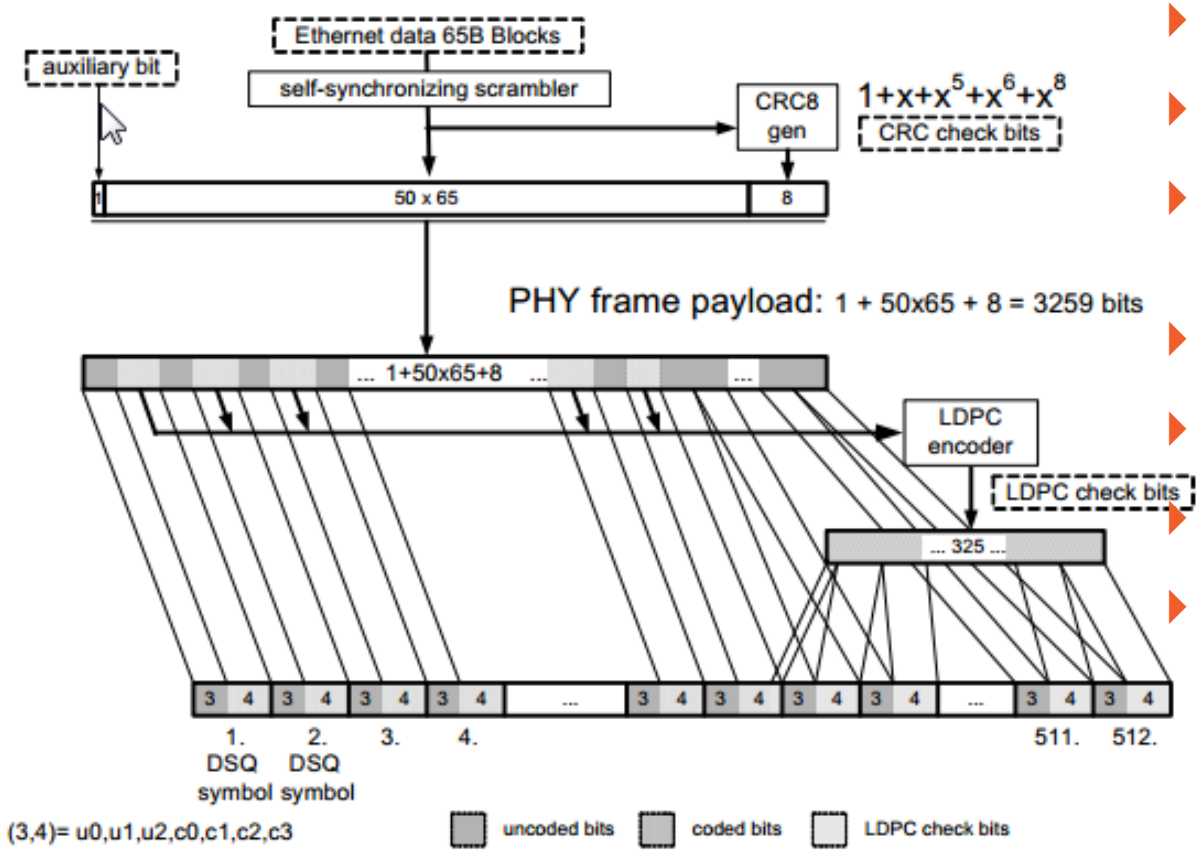


Figure 55–8—PCS detailed transmit bit ordering

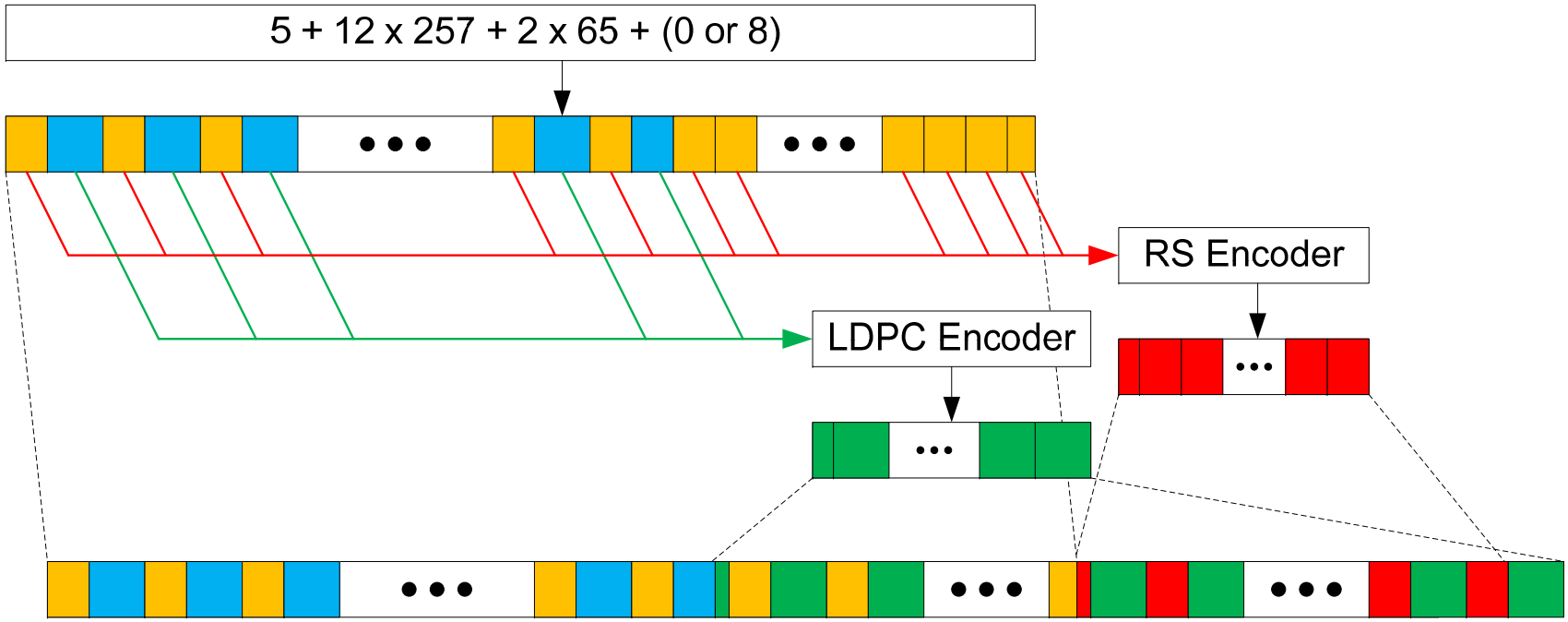
- 64/65 coding
- Scramble
- Pad + 50 x 65 bit + CRC = 3259 bits
- 1536 bits – uncoded
- 1723 bits – coded
- 325 bits – LDPC parity
- 3584 bits - Total

Protect uncoded bits with Reed Solomon

- **Change 50 x 64/65-bit blocks (3250 bits) with**
- **12 x 256/257-bit blocks + 2 x 64/65-bit blocks (3214 bits)**
- **Net 36 bits available for RS parity in addition to 1 pad bit and CRC8 bits**

	10GBASE-T	40GBASE-T Option 1 RS(192, 187) No CRC8	40GBASE-T Option 2 RS(192, 188) with CRC8
50 x 65 bits (64/65 coding)	3250	0	0
12 x 257 bits (256/257 Transcoding) + 2 x 65 bits (64/65 Transcoding)	0	3214	3214
8 (CRC)	8	0	8
Pad	1	5	5
Uncoded bits	1536	1496	1504
Reed Solomon parity bits	0	40	32
Coded bits	1723	1723	1723
LDPC parity bits	325	325	325
Total Bits	3584	3584	3584

LDPC and Reed Solomon Assembly



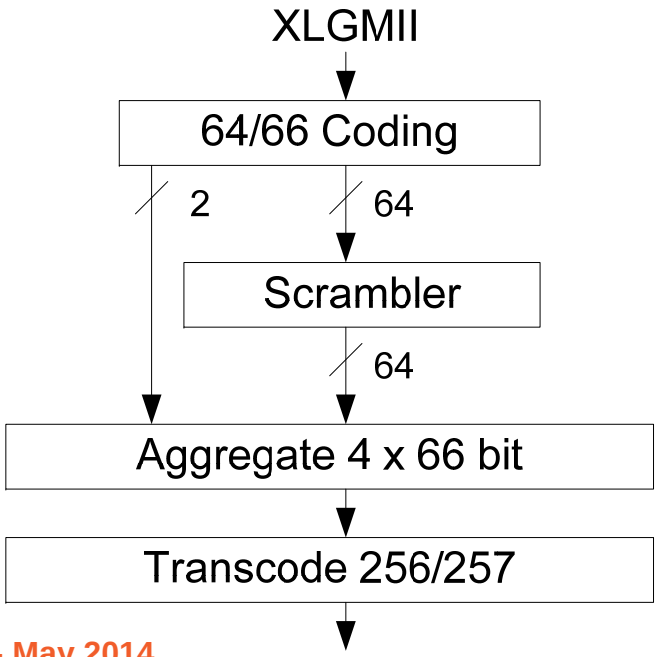
- 325 bits LDPC parity
- 40 or 32 bits Reed Solomon parity
- No change to 128 DSQ

Reed Solomon

- Reed Solomon parity bits placed in uncoded bit slots
- Option #1 RS(192, 187, 2^8)
  - No CRC8
  - Corrects 2 8-bit symbols
- Option #2 RS(192, 188, 2^8)
  - Has CRC8
  - Corrects 2 8-bit symbols

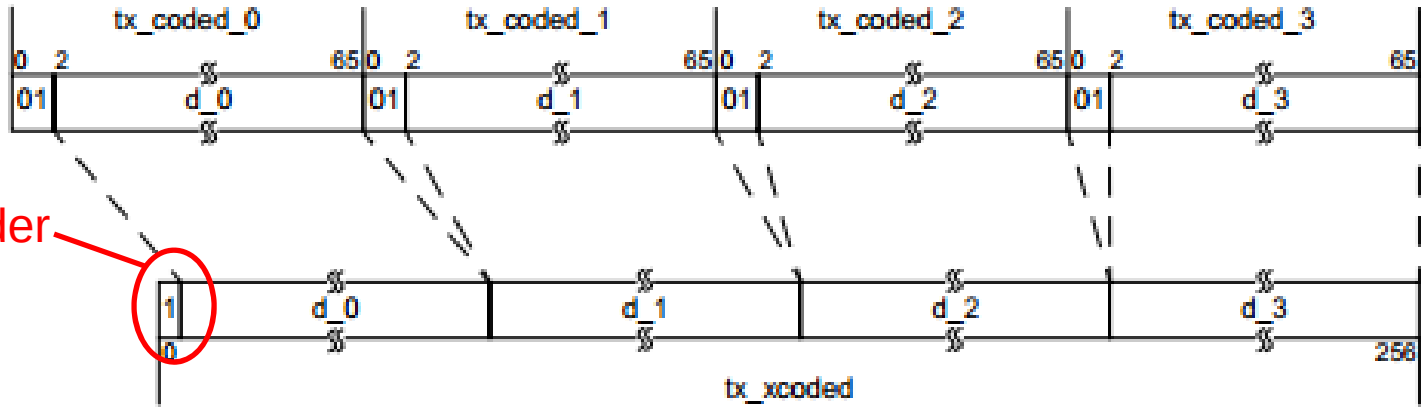
256/257 Transcoder From 802.3bj Clause 91.5.2.5

- Four 64/66 blocks mapped to 256/257 block after scrambling
- 2 bit header is not scrambled
- First bit of 257-bit block not scrambled (header bit)
- 2nd to 5th bit not scrambled for control blocks (control bits)



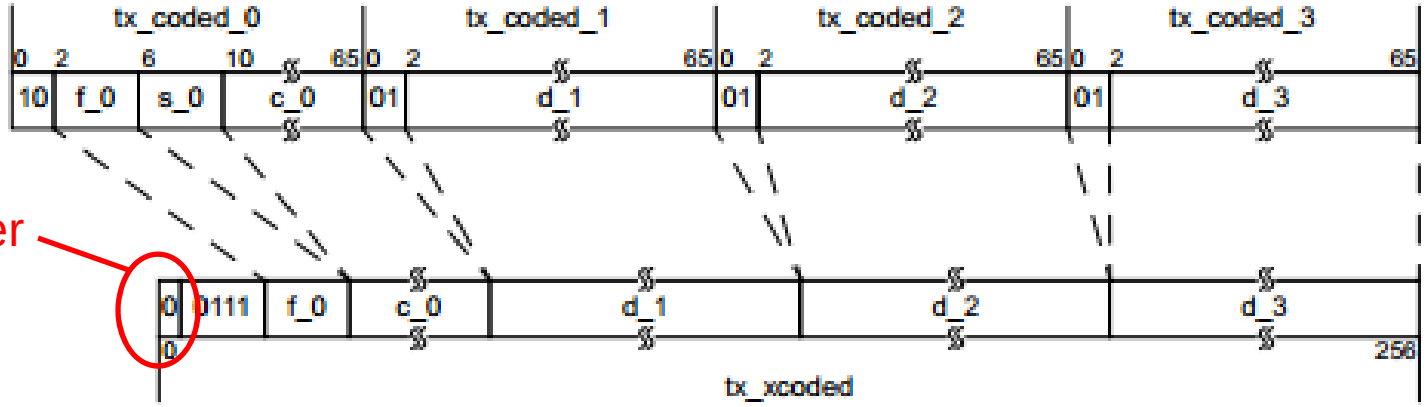
Examples

Data header



Example 1: All data blocks

Control header

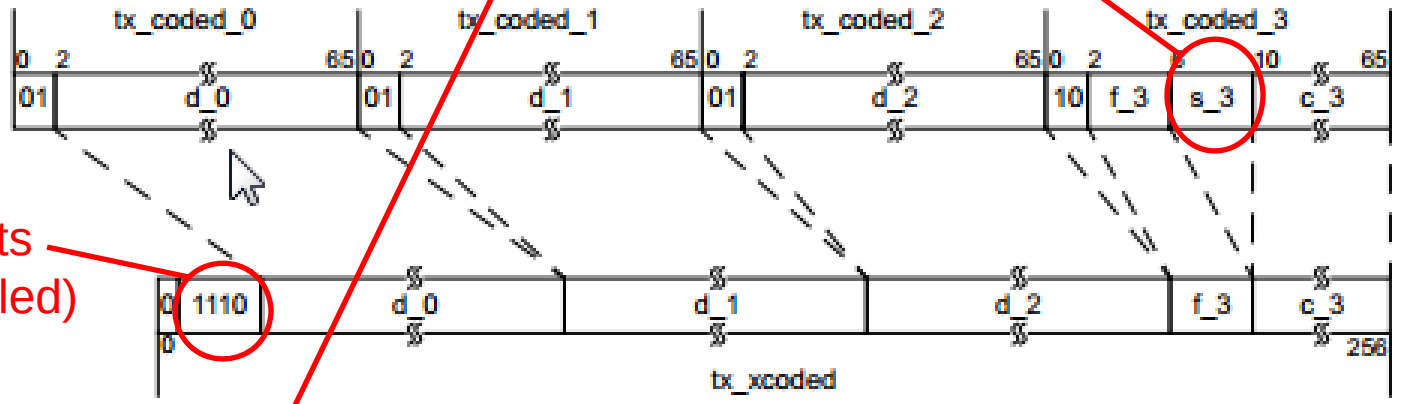


Example 2: Control block followed by three data blocks

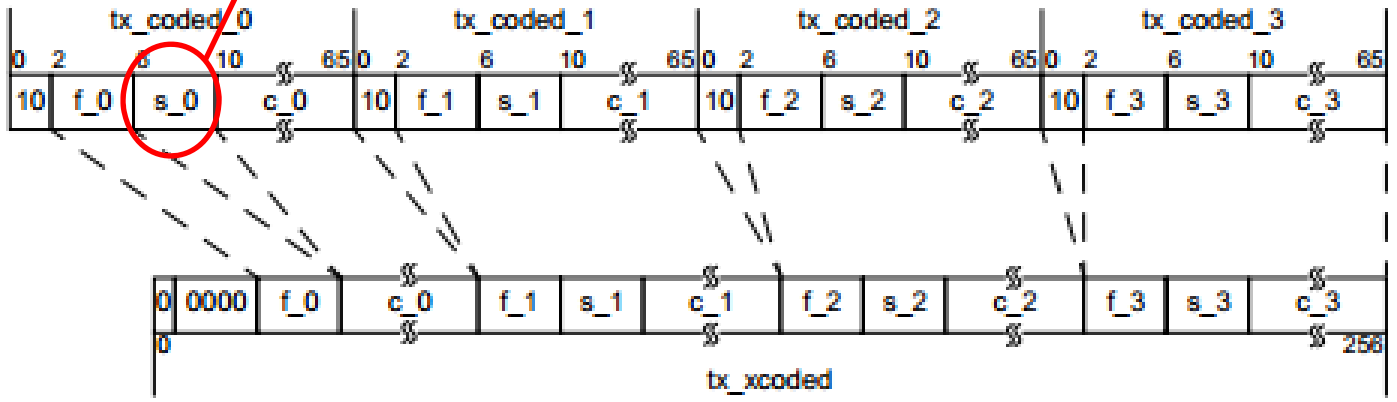
Examples

4 bits of type field removed from first control block to fit control bits

Control bits
(not scrambled)



Example 3: Three data blocks followed by a control block



Example 4: All control blocks

Ok To Remove Lower 4 Bits From 64/65 Bit Block

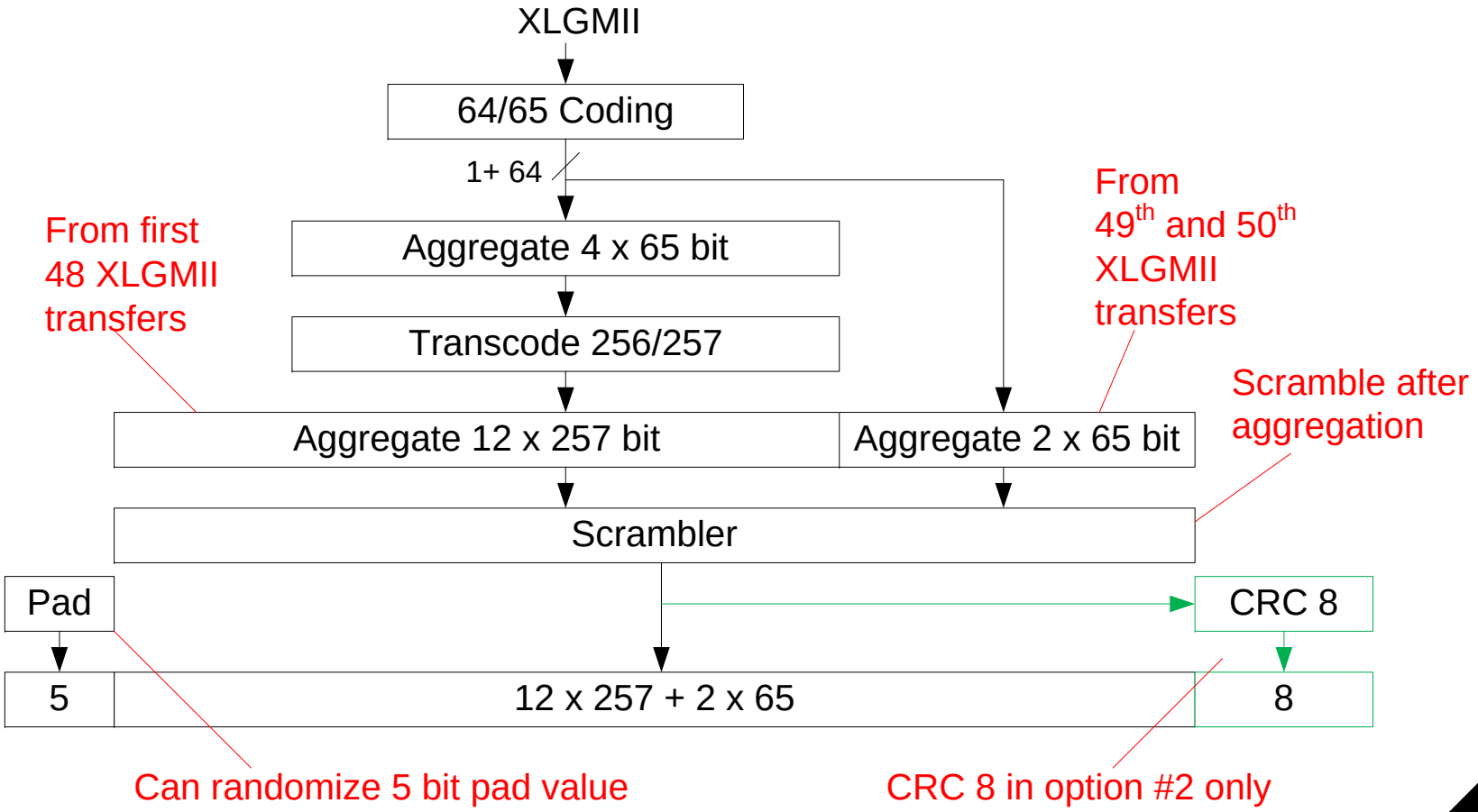
- **Upper 4 bits are unique – Can reconstruct lower 4 bits at receiver**

Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 55–9—64B/65B block formats

40GBASE-T Modify Scrambler Placement

- **Would be good to scramble header bit and control bits**
- **10GBASE-T scrambled the header bit in 64/65 bit block**



THANK YOU