IEEE 802.3bq
BASE-T Architecture Layers

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Background

- BASE-T and Fiber Architecture Layers are different by definition as defined by Clause 30.5 MAU
  - The sublayer that connects directly to the media is called MAU for 10 Mb/s operation and its equivalent is the combined PMA and PMD sublayers at higher operating speeds
  - MAU clause defines management for use at many speeds, it needs to be able to refer to MAUs and the PMA and PMD sublayers as a group
- PCS/PMA architecture layer model applies to 100BASE-T, 1GBASE-T and 10GBASE-T
- WE NEED to keep the architecture layers model for next generation BASE-T PHYs – 802.3bq (25G/40G)and 802.3bz (2.5G/5G),

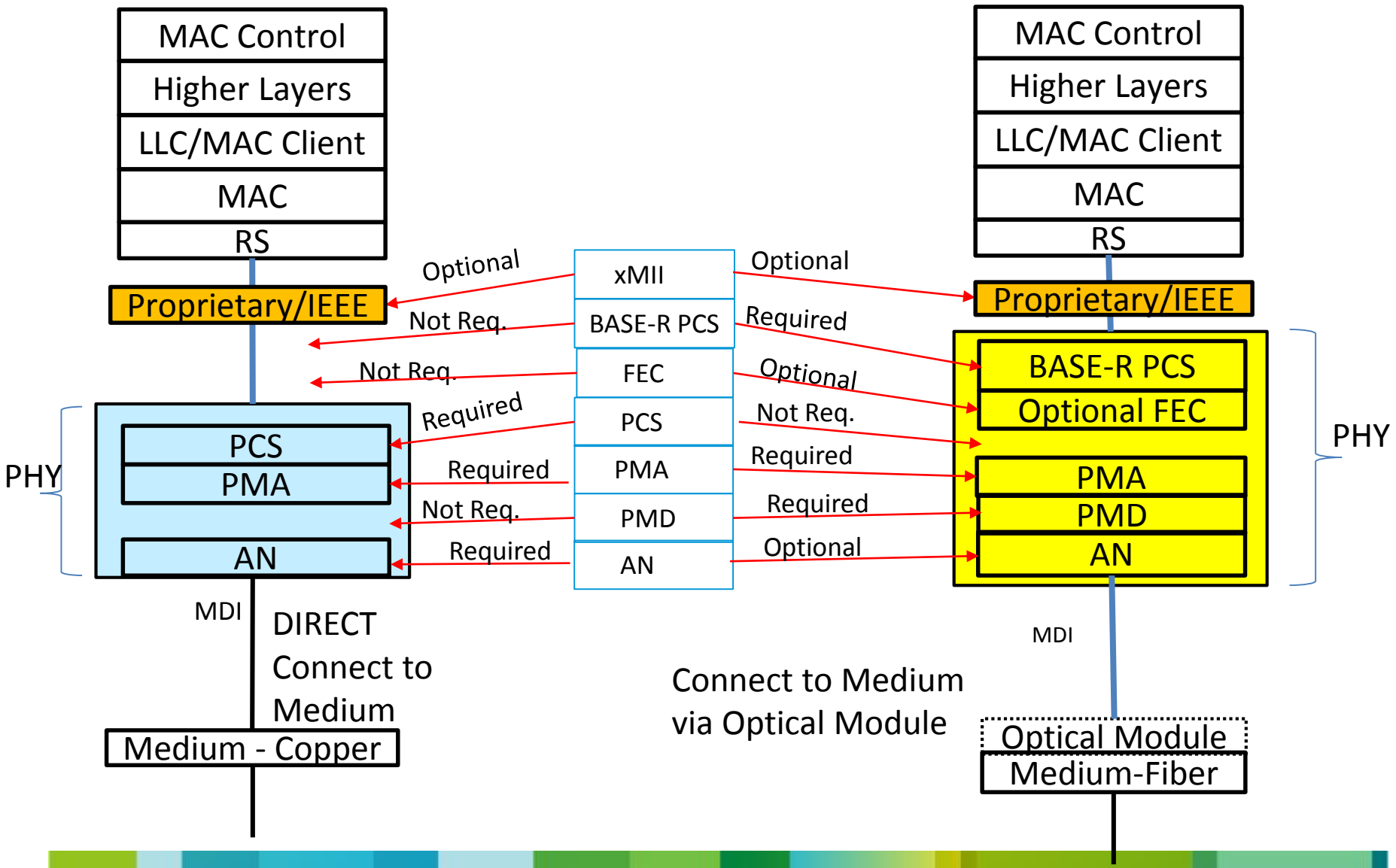
Supporters

- George Zimmerman – CME Consultant
- David Chalupsky

Why is BASE-T different from BASE-X?

- Backwards compatibility: Support 10M/100/1G and 10G speed on same Copper Medium
- Multi-Speed: Support multiple speed using same PHY, e.g., 100M/1G/10GBASE-T
- Multi-Port: Architecture model in 802.3 is based on single ports, high-volume implementations are often multiport
- Auto-Negotiation: Support speed 10M/100/1G/10G via auto-neg message exchange
- Speed-Adaptive: Fast convergence time expected using same medium. No physical intervention required

BASE-T and Fiber Architecture Layer Comparison



Why not provide a module architecture too?

- History shows module interfaces for BASE-T are not used in mass deployment
- Industry first favors proprietary integrated C2C or within-chip solutions
- Module implementations, if they arise, use proprietary MMD models
- Examples follow…

MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications

- 10G
  - XGMII (Clause 46) - Logical
    - 32-bit DDR TXD, 4-bit TXC and TX_CLK
    - 32-bit DDR RXD, 4-bit RXC and RX_CLK
  - XGXS (Clause 47) – XAUI Electrical Spec (PMA)
    - 4 SERDES TX and 4 SERDES RX (PCS 8B/10B) @ 3.125Gbps
  - 10GBASE-R Clause 49 (IEEE 64B/66B PCS only)
    - No IEEE Electrical Spec (no PMA)

XGMII and XGXS – NOT USED by commercially avaiable PHY devices

Technology Status

- 3.125Gbps SERDES available at time of IEEE definition (2000yr), but not 10.325Gbps SERDES

10.3125G SERDES (2002) available

Third party Solution

- Single port of 10G over Single Tx/Rx Serdes defined by OIF (XFI)
- Eight port of 10M/100M/1G over Single Tx/Rx SERDES (10Gbps)

MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications: 40G/100G

- **XLGMII/CGMII (Clause 82 PCS only)**
  - 40GBASE-R (4 lane 64b/66bPCS – 10.3125Gbps)
  - 100GBASE-R (10 lane 64b/66b PCS – 10.3125 Gbps)

10.3125G SERDES

Technology Status

- **XLAUI/CAUI-10 – Annex 83A/B (normative) – Electrical Spec (PMA)**
  - 4 x 10.3125Gbps used for 40Gbps
  - 10x10.3125Gbps for 100Gbps

25.78125Gbps SERDES

- **CAUI-4 – Annex 83D (normative) – Electrical Spec (PMA)**
  - 4 x 25.78125Gbps

Next Speed?

- **Third party solution will appear after IEEE specification – e.g. 50Gbps SERDES**
- **Multiple ports options: Example 2 x 25G over single SERDES**

Summary

- NGBASE-T Architecture Model with direct-reference to xxxMII MUST be preserved in order to support:
  - Backward compatibility
  - Multiple – rates and ports
  - Auto-negotiation
  - Fast Auto-negotiation
  - XGXS layer not used

Thank you.

MAC/PHY Interface – IEEE 802.3 and Technology Evolution

IEEE Specifications

- MII for 10 Mbps (clause 22) and 100 Mbps (Clause 35)
  - 4-bit TXD, TX_ER, TX_EN ,TX_ CLK
  - 4-bit RXD, RX_ER, COL, RX_ CLK
- GMII for 1 Gbps
  - 8-bit TXD, TX_ER, TX_EN ,TX_ CLK
  - 8-bit RXD, RX_ER, COL, RX_ CLK

Proprietary Solution

- Parallel Physical interface defined by IEEE – SERDES Tech not available

1G SERDES Available

Third party Solution

- Single port of 10M/100M/1G over Single Tx/Rx SERDES (1.25Gbps)
- Four ports of 10M/100M/1G over Single Tx/Rx SERDES (5Gbps)

Parallel Interface – Not used by commercial available PHYs