Cl **122** *SC* **122.7.2** *P* **177** *L* **11** # 1

Stassar, Peter Huawei Technologies

Comment Type **ER** *Comment Status* **A**

Table 122-7: Row on "Damage threshold, each lane (min)", contains "(min)", which shouldn't be there in the same way as the same row in Table 123-8. It is already a threshold and this should not be tested because it is a destructive test

SuggestedRemedy

Remove "(min)" from Table 122-7 for "Damage Threshold, each lane (min)".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
[Editor's note: Subclause set to 122.7.2, Page set to 177, Line set to 11]

In Table 122-7, change "Damage threshold, each lane (min)" to "Damage threshold, each lane"

Cl **122** *SC* **122.1.1** *P* **169** *L* **47** # 2

Stassar, Peter Huawei Technologies

Comment Type **ER** *Comment Status* **A**

Clause 122.1.1 currently contains the sentence ".when processed according to Clause 120 and Clause 119", which seems editorially a "funny" order, while it is intentional to process according to Clause 120 first before processing it according to Clause 119.

SuggestedRemedy

Add "next" between "Clause 120 and" and "Clause 119" to read ".when processed according to Clause 120 and next Clause 119"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add "then" between "Clause 120 and" and "Clause 119" to read "when processed according to Clause 120 and then Clause 119"

Cl **123** *SC* **123.1.1** *P* **191** *L* **30** # 3

Stassar, Peter Huawei Technologies

Comment Type **ER** *Comment Status* **A**

Clause 123.1.1 currently contains the sentence ".when processed according to Clause 120 and Clause 119", which seems editorially a "funny" order, while it is intentional to process according to Clause 120 first before processing it according to Clause 119.

SuggestedRemedy

Add "next" between "Clause 120 and" and "Clause 119" to read ".when processed according to Clause 120 and next Clause 119"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add "then" between "Clause 120 and" and "Clause 119" to read "when processed according to Clause 120 and then Clause 119"

Cl **121** *SC* **121.10** *P* **155** *L* **22** # 4

King, Jonathan Finisar

Comment Type **ER** *Comment Status* **A**

Fiber optic cabling model section needs text to equate the fibre optic cabling model (channel) to 'link segment', as is done in other optics clauses.

SuggestedRemedy

Add the sentence "The fiber optic cabling model (channel) defined here is the same as a simplex fiber optic link segment."
immediately before the sentence "The term channel is used here for consistency with generic cabling standards."

(commenter notes that this is the same text as used in equivalent sections in clauses 52,68, 87, 88 etc...

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.6.2.4** *P* **109** *L* **48** # 5

Sun, Phil Credo

Comment Type **T** *Comment Status* **A**

cw_bad_count counts the number of consecutive uncorrected FEC codewords. But it does not specify 3 uncorrectable frames are from one FEC decoder or 2 decoders in toal. Counting uncorrected blocks from one FEC provides lower false unlock rates.

SuggestedRemedy

counts the number of consecutive uncorrected FEC frames from one of the FEC decoders.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See the reponse to comment #68

Cl **119** *SC* **119.2.1** *P* **90** *L* **20** # 6

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A** *Bucket*

Data is not distributed to Code Words, but to FECs

SuggestedRemedy

Replace sentence starting with 'The data stream is distributed to two FEC.' with
The data stream is distributed to two logical FECs, weach of which encodes the data to Code Words.

Add 'The' to the beginning of the next sentence: 'The two FEC codewords are then...'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
The data stream is distributed to two FEC codewords and then FEC encoded to control errors.
To:
The data stream is distributed to two 5140-bit blocks and then FEC encoded to control errors.

Change the second sentence to:
'The two FEC codewords are then.'

Cl **119** *SC* **119.2.1** *P* **90** *L* **33** # 7

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

Declare what we do know about PCS lane identification

SuggestedRemedy

change TBD on line 33 to :
unique, per PCS lane markers (values are TBD)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
It attains alignment marker lock based on the common AM0 pattern that is periodically transmitted on every PCS lane. After alignment markers are found on all PCS lanes, the individual PCS lanes are identified using TBD and then re-ordered and deskewed.
To:
It attains alignment marker lock based on the common marker (CM) portion that is periodically transmitted on every PCS lane. After alignment markers are found on all PCS lanes, the individual PCS lanes are identified using the unique marker portion (UM) and then re-ordered and deskewed.

Also see response to comment #10.

Cl **119** *SC* **119.2.1** *P* **90** *L* **39** # 8

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

The description does not have enough detail as to what the receive process entails

SuggestedRemedy

On line 34, after 'Next the PCS' , add the following text:
", redistributes the FEC code word symbols to form a single stream, "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Next the PCS removes alignment markers,
to:
Next the PCS re-interleaves the correced FEC codewords on a 10-bit basis to form a single stream. The PCS then removes alignment markers,

See also comment #139

Cl **119** *SC* **119.2.4.1** *P* **93** *L* **34** # 9

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

Add reference to CL82 IDLE deletion rules

SuggestedRemedy

On line 37, add the following sentence: 'Refer to CL82 section 82.2.3.6 for IDLE insertion and deletion rules"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #21

Cl **119** *SC* **119.2.4.4** *P* **97** *L* **7** # 10

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

The Encoding description in Table 119-1 does not match the format of the entries

SuggestedRemedy

Change the Encoding description to be:
{ M0, M1, M2, FIXED3, M4, M5, M6, FIXED7, Unique FEC Lane Identifier}

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the heading of the table which is currently incorrect to:
{CM0, CM1, .CM7, UM0, UM1.UM6}
Also see response to comment #146.

Also on page 96, line 28:
Change:
There is a portion that is common across all alignment markers, and then a unique portion per PCS lane.
To:
There is a portion that is common across all alignment markers (designated as CM0 to CM7), and then a unique portion per PCS lane (designated as UM0 to UM6).

Cl **119** *SC* **119.2.4.5** *P* **99** *L* **30** # 11

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

Description is unclear and does not really match the functions

SuggestedRemedy

Replace sentences on lines 30 and 31 with the following:
To improve error correction ability, symbols from the two FEC codewords are symbol interleaved, to form the final PCS lanes. Data is distributed to the two FECs by breaking the stream up into 10 bit message symbols, and then distributing those message symbols in a round robin fashion to the two FECs.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
Data is distributed to those two FEC codewords by performing a 10 b round robin distribution of the tx_scrambled<256:0> data as follows
To:
Data is distributed to two 5140-bit message blocks by performing a 10-bit round robin distribution of the tx_scrambled_am<256:0> data.

Cl **119** *SC* **119.2.4.6** *P* **99** *L* **50** # 12

Baden, Eric Broadcom

Comment Type **TR** *Comment Status* **A**

Description is unclear as to how the FECs are organized

SuggestedRemedy

replace sentence on line 50 starting with 'The PCS interleaves." with the following:
The 400G RS(544,514) is formed from two, logical, 200G RS(544,514) FECs operating in parallel. The PCS interleaves 10 bit message symbols from the scrambler on a round robin basis, to these two, logical, FECs. Therefore, it takes 40 - 257 bit blocks from the transcoder to provide two codewords of message symbols, one to each, logical FEC. Each code is based on the generating polynomial given by Equation (119-1).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See the response to comment #124

Cl **119** *SC* **119.2.5.1** *P* **103** *L* **43** # 13

Baden, Eric — Broadcom

Comment Type **TR** *Comment Status* **A** *Bucket*

The receive function is a PCS function and not an FEC function.

SuggestedRemedy

Change 'RS-FEC' to 'PCS' on line 43.

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.5.7** *P* **105** *L* **53** # 14

Baden, Eric — Broadcom

Comment Type **TR** *Comment Status* **A** *Bucket*

Add reference to CL82 IDLE deletion rules

SuggestedRemedy

On line 53, add the following sentence: 'Refer to CL82 section 82.2.3.6 for IDLE insertion and deletion rules"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
of idle control characters
to:
of idle control characters (see 82.2.3.6 and 82.2.3.9 for insertion and deletion rules)

Cl **119** *SC* **119.2.6.2.1** *P* **106** *L* **38** # 15

Baden, Eric — Broadcom

Comment Type **TR** *Comment Status* **A** *Bucket*

The output of the Encoder is forwarded to the transcoder

SuggestedRemedy

Change 'PMA' to 'transcoder' on line 38

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.6.2.1** *P* **106** *L* **43** # 16

Baden, Eric — Broadcom

Comment Type **TR** *Comment Status* **A** *Bucket*

The output of the Encoder is forwarded to the transcoder

SuggestedRemedy

Change 'PMA' to 'transcoder' on line 43

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.1.5** *P* **89** *L* **14** # 17

Trowbridge, Steve — Alcatel-Lucent

Comment Type **TR** *Comment Status* **A**

OTN Mapping Reference Point Not identified

SuggestedRemedy

Indicate OTN Mapping Reference point in Figure 119-2 as the input of the "256B/257B Transcode" block in the Tx direction and the output of the "Reverse Transcode" block in the Rx direction

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add text to the end of 119.2.4.1
Note-The stream of 66-bit blocks generated by this process is used as the reference signal for mapping to OTN. See ITU-T G.709 [B50].

Add text to the end of 119.2.5.6
Note-The stream of 66-bit blocks generated by this process is used as the reference signal for de-mapping from OTN. See ITU-T G.709 [B50].

Cl **119** *SC* **119.1.5** *P* **89** *L* **12** # 18

Trowbridge, Steve — Alcatel-Lucent

Comment Type **TR** *Comment Status* **A**

Clock Rate Adaptation (idle/LI/ordered set insertion/deletion) location not indicated

SuggestedRemedy

Include clock rate adaptation in the 64B/66B Encode/Decode blocks

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See the response to comment #35

Cl **119** *SC* **119.2.3.5** *P* **93** *L* **1** # 19

Trowbridge, Steve Alcatel-Lucent

Comment Type **TR** *Comment Status* **A**

Missing EEE functionality and clock rate adaptation from the description - it is much more than the "Idle" control characters that are inherited from 82.2.3.6

SuggestedRemedy

Change section heading to "Idle (/I/), Low Power Idle (/LI/), and clock rate adaptation", change text to "Behavior of Idle and Low Power Idle control characters are described in 82.2.3.6"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Idle control characters are identical to those in 82.2.3.6
To:
Idle and LPI control characters are identical to those in 82.2.3.6

Cl **119** *SC* **119.2.3.8** *P* **93** *L* **15** # 20

Trowbridge, Steve Alcatel-Lucent

Comment Type **T** *Comment Status* **D**

It is not clear that it is not only the format of ordered sets, but the behavior of ordered sets that are the same as described in 82.2.3.9, in particular that ordered sets can be deleted for clock rate adaptation.

SuggestedRemedy

Change text to "The behavior of ordered sets is described in 82.2.3.9."

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

It is correct as stated.
"Ordered sets are specified identically as in 82.2.3.9." Implies all aspects are identical including clock compensation.

Cl **119** *SC* **119.2.4.1** *P* **93** *L* **30** # 21

Trowbridge, Steve Alcatel-Lucent

Comment Type **TR** *Comment Status* **A**

Since the AMs occupy <200ppm of space, idles are not necessarily deleted to make room for them: if the layers above are -100ppm and the layers below are +100ppm, you may insert idles - this is reflected in the last sentence of the first paragraph of 119.2.4.2, but the second paragraph only refers to deleting idles.

SuggestedRemedy

After the last sentence of the first paragraph of 119.2.4.2, add "See 119.2.3.5 and 119.2.3.8". Delete the 2nd paragraph of 119.2.4.2 since it is wrong.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
The transmit process generates 66-bit blocks based upon the TXD<63:0> and TXC<7:0> signals received from the CDMII. One CDMII data transfer is encoded into one 66-bit block. The transmit process must delete idle control characters or sequence ordered sets to accommodate the transmission of alignment markers. If the PCS transmit process spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle control characters. There are sufficient idle control characters to delete in order to make room for alignment markers, in addition to handling clock compensation. Idle control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the alignment markers. See 119.2.4.4 for more details.

To:
The transmit process generates 66-bit blocks based upon the TXD<63:0> and TXC<7:0> signals received from the CDMII. One CDMII data transfer is encoded into one 66-bit block. If the PCS transmit process spans multiple clock domains, it may also perform clock rate compensation via the deletion of idle control characters or sequence ordered sets or the insertion of idle (or LPI) control characters. Idle (or LPI) control characters or sequence ordered sets are removed, if necessary, to accommodate the insertion of the alignment markers. See 119.2.3.5 and 119.2.3.8 for the deletion and insertion rules, and 119.2.4.4 for more details on alignment markers.

See also comment #9

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **35** # 22

Wang, Tongtong Huawei

Comment Type **ER** *Comment Status* **A**

Sync header of all 66-bit blocks out of 256B/257B to 64B/66B transcoder are corrupted, while "rx_coded_0<1:0> ..." only indicates the first 66-bit block in 257b.

SuggestedRemedy

"it shall ensure that, for every 257-bit block within the two
associated codewords, the synchronization header for all 66-bit blocks at the output of the 256B/257B to 64B/66B transcoder, rx_coded_j<1:0> for j=0 to 3, are set to 11."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
the synchronization header for all 66-bit blocks at the output of the 256B/257B to 64B/66B transcoder, rx_coded_0<1:0>, is set to 11
to:
the synchronization header for all 66-bit blocks at the output of the 256B/257B to 64B/66B transcoder, rx_coded_j<1:0> for j=0 to 3, are set to 11.

Cl **120E** *SC* **120E.3.1.6.1** *P* **251** *L* **31** # 23

Smith, Ben Inphi Corporation

Comment Type **T** *Comment Status* **A**

The reference receiver currently includes a CTLE defined in 83E.3.2.1.1. Due to the increased sensitivity of PAM4 to residual ISI, an improved CTLE (that includes a low-frequency equalizer (LFEQ)) is beneficial.

SuggestedRemedy

Slide 4 of smith_01_122115_elect proposes a LFEQ+CTLE with 0.5dB peaking step sizes. Results in same presentation show a typical improvement in margin of 0.5 to 1.0 dB. Current reference to CTLE defined in 83E.3.2.1.1 should be replaced by the table on slide 4 of smith_01_122115_elect. Please note that an analogous change is required for Subclause 120E.3.2.1.1, Page 252, Line 37.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Bring Reference CTLE definition into 120E as new sub-clause based on 83E.3.2.1.1 and slides 3 and 4 of
http://www.ieee802.org/3/bs/public/adhoc/elect/21Dec_15/smith_01_122115_elect.pdf
with editorial license

Cl **120E** *SC* **120E.3.4.1** *P* **257** *L* **19** # 24

Smith, Ben Inphi Corporation

Comment Type **T** *Comment Status* **A**

The "high loss" module stressed input test sets the frequency-dependent attenuation to 13.8dB (10.25dB plus host transmitter package losses). It appears as though the current intent is that the pattern generator does not implement any form of pre-emphasis. However, based on presented simulation results (e.g., smith_3bs_01a_0915, smith_01_122115_elect), operation over high loss C2M links is expected to require pre-emphasis in the transmitter (to reduce the impact of pre-cursor ISI) in order to close the link. Therefore, the module stressed input test appears to be inconsistent with the likely operation of the link, and it isn't even clear that (in the absence of a TXFIR) the 50mV eye opening can be attained for the currently described test. As shown in smith_3bs_01a_0915.pdf, a fixed TXFIR with 10% precursor pre-emphasis (i.e., [-0.1,0.9]) provides reasonable performance over a wide range of channels.

SuggestedRemedy

The existing description of the stressed signal generation reads: "The stressed signal is generated by adding sinusoidal jitter, random jitter,
and bounded uncorrelated jitter to a clean pattern, followed by frequency-dependent attenuation". It is suggested to add the following text:
For high loss channels, pre-emphasis capability is likely to be required in the pattern generator to meet the TP4a EH6 and EW6 specifications.

Response *Response Status* **C**

ACCEPT.

Cl **121** *SC* **121.11.3.2** *P* **163** *L* **41** # 25

Kolesar, Paul CommScope

Comment Type **T** *Comment Status* **A**

The two TBDs in the last sentence of the paragraph can be removed becasue the IEC standards are published. It is possible to add further performance embellishments on the second standard that stipulate the minimum insertion loss and return loss of the MDI-to-cabling interface. Those will be proposed in the remedy to specify:
1) insertion loss Class Cm (the lowest performance class) that specifies a mean <= 0.50 dB and a maximum <= 1.0 dB for 97% of mated combinations;
2) return loss Class 2m that specifies a minimum of 20 dB, consistent with the requirement on the Tx, Rx, and cable plant.

SuggestedRemedy

Change the sentence as indicated:
The MDI shall meet the interface performance specifications of IEC 61753-1 TBD and IEC 61753-022-2 TBD for performance Class Cm/2m.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
[Editor's note: Comment Type set to T]

Change the 5th sentence in 121.11.3.2 from:
"The MDI shall meet the interface performance specifications of IEC 61753-1 TBD and IEC 61753-022-2 TBD."

to

"The MDI shall meet the interface performance specifications of IEC 61753-1 and IEC 61753-022-2 for performance Class Cm/2m."

Set text colour to black for 121.11.3.2.

Cl **121** *SC* **121.11.3.2** *P* **163** *L* **36** # 26

Kolesar, Paul CommScope

Comment Type **T** *Comment Status* **A**

ANSI/TIA-604-18 Fiber Optic Connector Intermateability Standard (FOCIS 18) was published in November 2015. An IEC equivalent will likely not be published until 2017. The first five TBDs in this clause can be determined using references to the ANSI/TIA standard. The last two TBDs will be addressed in a separate comment. Please refer to contribution kolesar_3bs_01_1215_mmf.pdf for further rationale.

SuggestedRemedy

Change the first two sentences of the clause as indicated here:
The MDI adapter or receptacle shall meet the dimensional specifications for interface (TBD) 7-1-3: MPO adapter interface - opposed keyway configuration designation FOCIS 18 A-k-0, or interface 7-1-10 TBD: MPO active device receptacle, flat interface, as defined in IEC 61754-7-1 TBD ANSI/TIA-604-18. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4 TBD: MPO female plug connector, flat interface for 2 to TBD fibres designation FOCIS 18 P-2x16-1-0-2-2 as defined in IEC 61754-7-1 ANSI/TIA-604-18.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the first two sentences of the clause from:
"The MDI adapter or receptacle shall meet the dimensional specifications for interface (TBD) 7-1-3: MPO adapter interface - opposed keyway configuration, or interface 7-1-10 TBD: MPO active device receptacle, flat interface, as defined in IEC 61754-7-1 TBD. The plug terminating the optical fiber cabling shall meet the dimensional specifications of interface 7-1-4 TBD: MPO female plug connector, flat interface for 2 to TBD fibres, as defined in IEC 61754-7-1."
to:
"The MDI adapter or receptacle shall meet the dimensional specifications for designation FOCIS 18 A-k-0 as defined in ANSI/TIA-604-18. The plug terminating the optical fiber cabling shall meet the dimensional specifications of designation FOCIS 18 P-2x16-1-0-2-2 as defined in ANSI/TIA-604-18."

This change follows the recommendations in kolesar_3bs_01_1215_mmf, reviewed in the MMF ad hoc of 18th December, 2015.

Set text colour to black for 121.11.3.2.

See also comment #26.

Cl **1** *SC* **1.3** *P* **26** *L* **7** # 27

Kolesar, Paul — CommScope

Comment Type **T** *Comment Status* **A**

Add new reference to the recently published standard for the MPO-16 used in clause 121. The year of publication should be considered optional, depending upon the specificity desired. This is the first edition of the MPO-16 standard.

SuggestedRemedy

Add:
ANSI/TIA-604-18:2015 Fiber Optic Connector Intermateability Standard - Type MPO-16 (FOCIS 18)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add:
ANSI/TIA-604-18:2015 FOCIS 18-Fiber Optic Connector Intermateability Standard-Type MPO-16

See also comment #26

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 28

Mellitz, Richard — Intel Corporation

Comment Type **TR** *Comment Status* **A** *R_LM*

RLM of 0.95 was suggested in healey_3bs_02_1115.pdf and was adopted for the RLM parameter in table 120D-7 . The two parameters should match.

SuggestedRemedy

Change "Level separation mismatch ratio RLM(min)" to 0.95 in Table 120d-1

Response *Response Status* **C**

ACCEPT.
See also comments #117 and #78

Cl **120D** *SC* **120D.3.1.1** *P* **236** *L* **53** # 29

Mellitz, Richard — Intel Corporation

Comment Type **TR** *Comment Status* **A**

np needs to be adjusted for dp+nb+1

SuggestedRemedy

change text to:
...exception that the PRBS13Q test pattern is used and n_p is equal to 13.

Response *Response Status* **C**

ACCEPT.
[Editor's note: Page changed from 237 to 236]

Cl **120D** *SC* **120D.4** *P* **241** *L* **21** # 30

Mellitz, Richard — Intel Corporation

Comment Type **TR** *Comment Status* **A** *SNR_Tx*

Zc seems to have been chosen from incremental trending. If we compromise between the original value of 78.2ohms and 90ohms, it would still represent limits of a real package. Combined with 280ff Cd would required SNR_Tx to be 33.4dB for SND_Tx of 31dB. The aggregate seems to improve COM for most channels.

SuggestedRemedy

In Table 120D-7, change Zc=85

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
In Table 120D-7, change Zc=85 (black)

Cl **120D** *SC* **120D.4** *P* **241** *L* **50** # 31

Mellitz, Richard — Intel Corporation

Comment Type **TR** *Comment Status* **A**

Calculations were based on Rd=40 and since Rd=55 and np should be 13 if the Zc=85 ohms then readjustment is required to achieve Vfmin of 0.4v for the reference package.

SuggestedRemedy

In Table 120D-7, change Av=Afe=0.445 and Ane=0.6675

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #82

Cl **120D** *SC* **120D.4** *P* **242** *L* **6** # 32

Mellitz, Richard — Intel Corporation

Comment Type **TR** *Comment Status* **R** *SNR_Tx*

The specification of SNDR is 31dB. However the COM computation includes some reflection noise of the package which is included in SNDR.

SuggestedRemedy

In Table 120D-7, change SNR_Tx to 33.4dB

Response *Response Status* **C**

REJECT.
See resolution to Comment #119.

Cl **119** *SC* **119.2.3.5** *P* **93** *L* **2** # 33

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A**

There is quite a bit of functionality hiding behind the simple reference to 82.2.3.6. Most of the rate matching details are hidden behind the refernece.

SuggestedRemedy

Either copy the text from 82.2.3.6 or add a hint that the crossreference is worth following. Something like: "Idle control characters and the part they play in rate matching is identical to 82.2.3.6"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #19

Cl **119** *SC* **119.2.3.8** *P* **93** *L* **15** # 34

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **D**

There is quite a bit of functionality hiding behind the simple reference to 82.2.3.9. Most of the rate matching details are hidden behind the refernece.

SuggestedRemedy

Either copy the text from 82.2.3.9 or add a hint that the crossreference is worth following. Something like: "Ordered sets and the part they play in rate matching is identical to 82.2.3.9"

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

The behavior is identical to that of 82.2.3.9, so the reference is correct as stated.

Cl **119** *SC* **119.1.5** *P* **89** *L* **3** # 35

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A**

Figure 119-2 has a boxes called "64B/66B Encode" and "64B/66B Decode" but the corresponding text sections (119.2.4.1 and 119.2.5.7) are called "Transmit Process" and "Receive Process". The clock/rate matching function is not shown in the figure.

SuggestedRemedy

Split the transmit and receive process subsections into two pieces "rate matching" and "64b66b encode/decode". Add a "rate match" box to the top of figure 119-2 in between the CDMII and the 64b66b encode/decode blocks.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change the TX box title to "Encode and rate matching"
Also change the title of sub clause 119.2.4.1 from "Transmit process" to "Encode and rate matching"

Change also (on page 93, line 27):
The transmit process generates
to:
The PCS generates

Change the RX box title to "Decode and rate matching"
Also change the title of sub clause 119.2.5.7 from "Recieve process" to "Decode and rate matching"

Change also (on page 103, line 43):
The RS-FEC receive function forms 16
to:
The PCS forms 16

See also comment #18

Cl **119** *SC* **119.2.4.4** *P* **96** *L* **17** # 36

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A**

The text currently says "Room for the alignment markers is created by periodically deleting idle control characters from the CDMII data stream". This doesn't make it clear where this happens or that you can insert/delete anything that is legal for clock compensation to make this happen. The receive-side "alignment marker removal" section (119.2.5.4) doesn't mention rate matching and therefore is fine.

SuggestedRemedy

Add a reference to the transmit process (119.2.4.1) (or "rate match" section if the related comment goes through) to make it clear that rate matching is the same as clock compensation both in location and mechanism. "Room for the alignment markers is created by the transmit process (119.2.4.1)".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
Room for the alignment markers is created by periodically deleting idle control characters from the CDMII data stream
to:
Room for the alignment markers is created by the transmit PCS (see 119.2.4.1).

Cl **119** *SC* **119.2.4.5** *P* **99** *L* **33** # 37

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A**

The pre-fec distrubtion doesn't really use tx_scrambled as defined in 119.2.4.3- it really uses the data stream after alignment markers are inserted, so it is using the output of section 119.2.4.4 which doesn't have a name.

SuggestedRemedy

Define a tx_scrambled_am in 119.2.4.4 and then use this in the pre-FEC distribution in 119.2.4.5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

On Page 96, line 25, change:
The group of alignment markers shall be inserted once every 163 840 257-bit blocks.

To:
The group of alignment markers shall be inserted once every 163 840 257-bit blocks. The variable tx_scrambled_am is created by inserting the group of alignment markers in the variable tx_scrambled.

Change the variable to tx_scrambled_am on page 99, lines 32 and 36.

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **14** # 38

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A**

The decoded data from the RS decode is described to be put into rx_scrambled, but it really doesn't, since the alignment markers are still in the bitstream.

SuggestedRemedy

Define a rx_scrambled_am which gets the output of the RS decode function. Then the alignment marker removal section (119.2.5.4) takex rx_scrambled_am and produces rx_scrambled.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

On line 14 change to rx_scrambled_am.

On line 44 change:
The vector am_rx shall be removed prior to transcoding.
To:
The vector am_rx shall be removed from rx_scrambled_am to create rx_scrambled prior to transcoding.

Cl **45** *SC* **45.2.1.116a** *P* **44** *L* **8** # 39

Maki, Jeffery — Juniper Networks

Comment Type **TR** *Comment Status* **A**

Table 45-90a. CDAUI-16 chip-to-module recommended CTLE register bit definitions need to be per lane and not per module. PCB routing studies for CFP8 connectors show it to be problematic to match the length of all chip-to-module traces sufficiently for the TX links. The length variation between the bottom row TX lanes and top row TX lanes is more than 2 inches. (See the pink and yellow traces in the drawing with filename "CFP8 PCB Routing Example.png")

SuggestedRemedy

Define Register 1.499 to be per-lane for setting of the CTLE recommended value for this 16 lane interface.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Define Registers 1.400 through 1.415 as CDAUI-16 chip-to-module recommended CTLE, lane 0 through lane 15 with editorial license.
See also comment #136.

Cl **119** *SC* **119.2.3.2** *P* **91** *L* **35** # 40

Slavick, Jeff — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

The block_type field is used to identify blocks that contain a Start Character, Terminate Character or Ordered set.

SuggestedRemedy

Delete the word "character" after Terminate

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.3.2** *P* **92** *L* **1** # 41

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A** *Bucket*

Figure 119-3 is a duplicate of 82-5

SuggestedRemedy

Remove 119-3 and change all references to it to point to 82-5

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.5** *P* **99** *L* **31** # 42

Slavick, Jeff — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

We distribute 10 bits of data

SuggestedRemedy

Change "10 b" to "10-bit"

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.9** *P* **103** *L* **26** # 43

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

Redundant shall statement with the last paragraph of 119.2.1. Also this is the generator not the checker section.

SuggestedRemedy

Change the first paragraph of 119.2.4.9 to read "The PCS has the ability to generate a scrambled idle test pattern which is suitable for receiver tests and for certain transmitter tests.

Response *Response Status* **C**

ACCEPT.

[Editor's note: Subclause changed from 119.2.5.9 to 119.2.4.9]

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **35** # 44

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

What does "mark" mean when error indication is in affect?

SuggestedRemedy

Change "mark" to "discard"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The PCS does not discard these blocks, rather it marks them for discard by the next layer in the stack. Change the text to correct and clarify it as below:

Change:
This causes the PCS to mark all frames that are fully or partially within the two associated codewords.
To:
This causes the PCS to mark (set to EBLOCK_R) all blocks that contain data from the uncorrected codeword.

Cl **119** *SC* **119.2.5.4** *P* **104** *L* **39** # 45

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

The AM marker removal runs on rx_scrambled produced by the decoder block.

SuggestedRemedy

Change "The first 2056 message bits in every 8192nd codeword is the vector" to read "Every 8192nd codewords the first 2056 bits of rx_scrambled blocks is the vector"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change
"The first 2056 message bits in every 8192nd codeword is the vector"
to read
"Every 8192nd codewords the first 2056 bits of rx_scrambled_am blocks is the vector"

Cl **119** *SC* **119.2.5.8** *P* **106** *L* **5** # 46

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

What is the point of the scrambled idle checker? FEC statistics provide superior granularity of error rate (10b checking instead of 66b) and you need the FEC engine to be running to provide valid data to the output of the descrambler. If you can't link up a full 400G PHY, then use a PMA test pattern. (Scrambled Idle Generation is needed to enable PCS to generate valid FEC data streams)

SuggestedRemedy

Remove the scramble idle checker from clause 119.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
With editorial license.

A straw poll of the Task force was taken:
Do you support the removal of the scrambled idle error checker feature?
Yes 13
No 0
Abstain 19

Cl **119** *SC* **119.2.5.3** *P* **97** *L* **28** # 47

Slavick, Jeff — Avago Technologies

Comment Type **T** *Comment Status* **A**

Bypass error indication feature is not included. This is a very useful feature to enable the user to reduce latency (~25% of the FEC latency). When a link can run with an uncorrected error rate of 0 you can reduce latency by turning off the error indication feature. When segments in the link aren't running at the specified limits then an uncorrected error rate near 0 can be achieved. Designs supporting 25GE and 100GE RS-FEC designs (which include this feature) would likely support it for 400G as well, so adding the specification ensures the appropriate check is done to ensure MTTFPA. Correction of the FEC codewords still occurs, the FEC skips buffering the data to validate that the codeword was completely fixed before passing it onto the PCS decoder. It's safe to bypass this buffering since you're non-fixable error rate (uncorretable errors) is 0. This feature would be usable before bypass_correction is usable, and bypass correction is currently part of the RS-FEC's definition.

SuggestedRemedy

Add the following text to the end of 119.2.5.3
"The Reed-Solomon decoder may optionally provide the ability to bypass the error indication feature to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_indication_ability variable (see X). When the option is provided it is enabled by the assertion of the FEC_bypass_indication_enable variable (see X).

When FEC_bypass_correction_enable is asserted, the decoder shall not bypass error indication and the value of FEC_bypass_indication_enable has no effect.

When FEC_bypass_indication_enable is asserted, additional error monitoring is performed by the RS-FEC sublayer to reduce the likelihood that errors in a packet are not detected. The Reed-Solomon decoder counts the number of symbol errors detected on all PCS lanes in consecutive non-overlapping blocks of 8192 codewords. When the number of symbol errors in a block of 8192 codewords exceeds 5560, hi_ber shall be set to true and the Reed-Solomon decoder shall cause synchronization header rx_coded<1:0> of each subsequent 66-bit block that is delivered to the PCS decoder to be assigned a value of 00 or 11 for a period of 60 ms to 75 ms."

Change the definition of hi_ber in 119.2.6.2.2 to read "Boolean variable which indicates when the Symbol Error Rate being received has exceeded the threshold defined in 119.2.5.3 when the RS-FEC is operating in FEC_indication_bypass mode."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy taking account of comments #129 and #130 and changing "to be assigned a value of 00 or 11" to "to be assigned a value of 11" with editorial license

A straw poll of the Task force was taken:

Do you support the addition of a bypass indication feature?
Yes 8
No 0
Abstain 22

Cl **122** *SC* **122.11.3.2** *P* **184** *L* **22** # 48

Mazzini, Marco Cisco Systems

Comment Type **TR** *Comment Status* **R**

Referring to http://www.ieee802.org/3/bm/public/smfadhoc/meetings/apr30_13/kolesar_01_0413_smf.pdf, slide 6-10. Performance level D/3 is not appopriate for MPO female angled connectors. Into slide 9-10 a guidance of which the MDI should specify referring to IEC 61753-021-2 standard is given. Into slide 6 the appropriate Return loss is given too: for D/1 (APC) is >=60dB mated, >= 55dB unmated.

SuggestedRemedy

Replace performance Level D/3 with performance level D/1. Change Editor's note accordingly to D/1: row 26, 55dB instead of 35dB.

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.10** *P* **182** *L* **24** # 49

Mazzini, Marco Cisco Systems

Comment Type **T** *Comment Status* **R**

Set a value for Optical return loss into Table 122-12: referring to http://www.ieee802.org/3/bm/public/smfadhoc/meetings/apr30_13/kolesar_01_0413_smf.pdf, slide 6 about TIA , the appropriate value is 49dB.

SuggestedRemedy

Change "Optical return loss (min)" from TBD to 49 dB into Table 122-12

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.11.2.2** *P* **183** *L* **17** # 50

Mazzini, Marco Cisco Systems

Comment Type **T** *Comment Status* **R**

Change maximum discrete reflectance value to appopriate for MPO angled connector. Refer to http://www.ieee802.org/3/bm/public/smfadhoc/meetings/apr30_13/kolesar_01_0413_smf.pdf, slide 6

SuggestedRemedy

Change "-35 dB" to "-55 dB"

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.12.4.6** *P* **189** *L* **8** # 51

Mazzini, Marco Cisco Systems

Comment Type **T** *Comment Status* **R**

Change maximum discrete reflectance value to appopriate for MPO angled connectors. Refer to http://www.ieee802.org/3/bm/public/smfadhoc/meetings/apr30_13/kolesar_01_0413_smf.pdf, slide 6

SuggestedRemedy

In 122.12.4.6, OC2
Change "-35 dB" to "-55 dB"

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.11** *P* **179** *L* **31** # 52

Mazzini, Marco Cisco Systems

Comment Type **T** *Comment Status* **R**

Set a value for Optical return loss - proposed 26dB refer to http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_15/mazzini_01a_1215_smf.pdf, slide 6

SuggestedRemedy

In Table 122-11
Change "Optical return loss" from TBD to 26 dB

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.7.3** *P* **177** *L* **42** # 53

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **R**

Power budget should be updated including new values of MPI. Referring to http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_15/mazzini_01a_1215_smf.pdf, slide 7, with 26dB TX/RX reflectance and 55dB connector RL the maximum MPI penalty is < 0.2dB (deterministic upper bound).

SuggestedRemedy

In Table 122-8
Change "Power budget (for max TDP)" from 6 to 5.7 dB
Change "Maximum discrete reflectance" from -35 to -55 dB
Change "Allocation for penalties (for max TDP)" from 3 to 2.7 dB (2.5 for TDP + 0.2 for MPI)

Response *Response Status* **C**

REJECT.
See comment #55

Cl **122** *SC* **122.7.3** *P* **177** *L* **20** # 54

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **R**

Comment #75 (Dudek) against Draft1.0 was accepted with change to Receiver Sensitivity Inner OMA from -9.1 to -9.25dBm into Table 122-7. Still in agreement with the fact discrepancy was fixed, we believe is better to reduce TX OMA by 0.15dB and put Receiver sensitivity OMA inner back to -9.25dBm. This allow some TX OMA and power relaxation (see http://www.ieee802.org/3/bs/public/15_11/traverso_3bs_01a_1115.pdf). Referring to http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_15/mazzini_01a_1215_smf.pdf, slide 10 or a pictorial view of the power budget. In this way Average receiver power (min) should be reduced by 0.45dB.

SuggestedRemedy

In Table 122-7
Change "Average receive power, each lane (min)" from -4.9 to -5.4
Change "Receiver sensitivity (OMAinner), each lane (max)" from -9.1 to -9.25 dBm

Response *Response Status* **C**

REJECT.
See response to comment #55

Cl **122** *SC* **122.7** *P* **176** *L* **20** # 55

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **R**

Starting form Receiver Sensitivity Inner OMA of -9.25dBm (draft 1.0 value), considering 0.2dB MPI penalty (was 0.5dB) into the budget, implementation penalty of 4.8dB and channel loss of 3dB, OMA Outer and Launch power in OMA outer minus TDP can be re-calculated. Refer to http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_15/mazzini_01a_1215_smf.pdf, for MPI penalty.

SuggestedRemedy

In Table 122-6
Change "Outer Optical Modulation Amplitude (OMAouter), each lane (min)" from 0.2 to -0.25 dBm
Change "Average launch power, each lane (min)" from -1.9 to -2.35 dBm
Change "Launch power in OMAouter minus TDP, each lane (min)" from -0.8 to -1.25 dBm
Change "RINxxOMA (max)" to "RIN26OMA (max)"
Change "Optical return loss tolerance (max)" from TBD to 26 dB
Change "Transmitter reflectance (max)" from -20 to -26 dB

Response *Response Status* **C**

REJECT.
No consensus was reached during the SMF ad hoc on 15 December 2015 to make this change in parameter values. Different values are proposed by comment #84.

See also response to comments #177, against P802.3bs D1.0 in http://www.ieee802.org/3/bs/comments/P802d3bs_D1p0_comments_final_ID.pdf#page=46
As per consensus from SMF Ad Hoc on 6 October 2015: "There was agreement that the various reflection specifications should be dealt with as a group in association with a study of the penalty they cause."

Contributions addressing MPI penalty penalty allocation and reflection specifications are invited.
See also response to comment #97.

Cl **123** *SC* **123.7.3** *P* **200** *L* **18** # 56

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **A**

Allocation for penalty (for maximum TDP) of Table 123-9 doesn't include MPI then link budget doesn't include it. As presented at SMF ad-hoc meeting (refer to http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_15/mazzini_01a_1215_smf.pdf, slide 4), this should be harmonized across SMF PMD. Into same presentation (slide 8) a proposal to refer to next TIA TR-42.11 revision for LC connector return loss is given. This will allow to reduce MPI penalty over 400GBASE-FR8/LR8, assuming certain values of TX/RX reflectances. Need further discussion over LC return losses, definition of Transmitter and Receiver reflectances for FR8/LR8 (still TBD into Table 123-7 and Table 123-8), in order to define the correct MPI penalty (inside "Allocation for penalties") and power budget.

SuggestedRemedy

In Table 123-9
Change "Power budget (for maximum TDP") from 6.2dB to TBD for 400GBASE-FR8.
Change "Power budget (for maximum TDP") from 8.7dB to TBD for 400GBASE-LR8.
Change "Allocation for penalties (for maximum TDP)" from 2.2dB to TBD for 400GBASE-FR8.
Change "Allocation for penalties (for maximum TDP)" from 2.4dB to TBD for 400GBASE-LR8.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add an editor's note below Table 123-9:
[Editor's note: When the penalty due to MPI has been agreed, the values in Table 123-9 will be adjusted to include this penalty.]

Cl **122** *SC* **122.8.9** *P* **180** *L* **16** # 57

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **R**

From discussions occurred during Dec 15th ad-hoc call, seems Receiver sensitivity is defined assuming an ideal NRZ input signal and not assuming a PAM4 ideal signal. This is not quoted into 122.8.9.

SuggestedRemedy

Change "Receiver sensitivity, which is defined for an ideal input signal" into Receiver sensitivity, which is defined for an ideal NRZ input signal into 122.8.9 and into 123.8.9.

Response *Response Status* **C**

REJECT.
The comment description does not correctly reflect the discussions during the SMF ad hoc on 15 Dec 2015. The consensus was that the value of 4.7 dB given in http://www.ieee802.org/3/bs/public/adhoc/smf/15_12_01/king_01_1215_smf.pdf is the difference in sensitivity between an ideal PAM4 signal and an ideal NRZ signal for the same receiver. There was also consensus that the receiver sensitivity in the P802.3bs draft would not be defined to be for an NRZ signal and that therefore 4.7 dB was not an appropriate value to use.

Cl **122** *SC* **122.8.10** *P* **180** *L* **25** # 58

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **A**

Stressed receiver sensitivity is the only parameter ensuring interoperability across different PAM4 implementation technologies. It should be defined assuming a PAM4 signal, with the right amount of stress occurring on each the three slicer levels of the PAM4 receiver DUT. It cannot be an NRZ signal.

SuggestedRemedy

Add "Stressed Receiver sensitivity is defined for a stressed PAM4 input signal", into 122.8.10 and 123.8.10.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
A complete proposal for how the stressed receiver sensitivity test will be performed is requested, including the means to ensure "the right amount of stress occurring on each the three slicer levels".

Cl **120E** *SC* **120E.3.1** *P* **249** *L* **28** # 59

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **A**

In order to improve the CDAUI-8 C2M, a maximum VEC at TP1a should be specified. Assuming max p-p output voltage requirement and minimum eye height, eye VEC can be as high as 15.5dB. Refer to http://www.ieee802.org/3/bs/public/15_11/mazzini_3bs_01_1115.pdf, slide 12. Will be back with a proposal about Vertical eye closure (max) in the future.

SuggestedRemedy

Add a row into Table 120E-1
Define "Vertical eye closure (max)" with value TBD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
However, the Table will not be altered until a value is agreed.

Cl **120E** *SC* **120E.3.1.6.1** *P* **252** *L* **37** # 60

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **A**

Reference receiver for host output eye width and eye eight evaluation it's currently defined in 83E.3.2.1.1, Several contributions shown this reference receiver equalizer it's enough to deal with CDAUI-8 interface. Into http://www.ieee802.org/3/bs/public/15_11/mazzini_3bs_01_1115.pdf, slide 5-8, a proposal to use CTLE(2p1z) + LFEQ (1p1z) was given.
Need to define a new formula (instead of referrring to 83E-4), table (instead of Table83E-2) and figure (instead of Figure 83E-10), will do in the future.

SuggestedRemedy

Remove reference to 83E.3.2.1.1 into 120E.3.1.6.1.
Add formula:

H(f)=[(GP1P2)/Z1]x{(jf+Z1)/[(jf+P1)x(jf+P2)]}x{(jf-Z_LF)/(jf-P_LF)]

Where (for linear Boost):
G is the DC/LF Gain
P1 is the CTLE Boost Pole Freq 1
P2 is the CTLE Boost Pole Freq 2
Z1 is the CTLE Boost Zero Freq 1

and (linear De-emphasis):
Z_LF is the De-emphasis Zero Freq
P-LF is the De-emphasis Pole Freq

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #23

Cl **120E** *SC* **120E.1.1** *P* **247** *L* **53** # 61

Mazzini, Marco — Cisco Systems

Comment Type **T** *Comment Status* **A**

Referring to http://www.ieee802.org/3/bs/public/adhoc/logic/aug25_15/anslow_01_0815_logic.pdf (slide 26), for DFE-less links, seems the correct assumption is to keep random error model rather than burst one. If yes, according to http://www.ieee802.org/3/bs/public/15_11/mazzini_3bs_01_1115.pdf, slide 9, margins over CDAUI-8 are still good assuming 1E-5 BER.

SuggestedRemedy

Replace "..shall be less than 10-6 provided that the error statistics are sufficiently random." with "..shall be less than 10-5 provided that the error statistics are sufficiently random." into row 53.
Replace "All 3 PAM4 eyes, at 10-6 probability" with "All 3 PAM4 eyes, at 10-5 probability" on notes a,b of Table 120E-1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
On line 53, replace:
"shall be less than 10-6" with: "shall be less than 10-5"
In footnotes a,b of Table 120E-1 replace "All 3 PAM4 eyes, at 10-6 probability" with "All 3 PAM4 eyes, at 10-5 probability"
See also comment #113

Cl **119** *SC* **119.2.4.7** *P* **102** *L* **26** # 62

Gustlin, Mark — Xilinx

Comment Type **E** *Comment Status* **A**

There is a placeholder for a PCS block distribution diagram, at this time there is no plans on having this diagram.

SuggestedRemedy

Delete the figure title: Figure 119-9-PCS Block distribution.
And delete the TBD.

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.6** *P* **100** *L* **14** # 63

Gustlin, Mark Xilinx

Comment Type **E** *Comment Status* **A** *Bucket*

The two FEC codewords that are interleaved are currently labled as codeword0 and codeword1. When creating a detailed bit ordering diagram, I found that it would be clearer to lable them as codewordA and codewordB.

SuggestedRemedy

Change all instances of Codeword0 to CodewordA, and Codeword1 to CodewordB.

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.5.6** *P* **105** *L* **25** # 64

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

There is a bug in the 256B/257B to 64B/66B transcoding algorithm.
Scrambled is stated in point d2 and it is no longer scrambled.
Also in sub-point e2) g<3:0> has been used but it is not described how to generate g<3:0>.

SuggestedRemedy

Change:
d2) Let f_c<3:0> = rx_coded_c<5:2> be the scrambled first nibble (based on transmission order) of the block type field for rx_coded_c.
To:
d2) Let g<3:0> = rx_coded_c<5:2> be the first nibble (based on transmission order) of the block type field for rx_coded_c.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In b2) line 19, change:
rx_payloads<(64c+7):(64c+4)> = 0000 (an arbitrary value that is later replaced by s_c)
to:
rx_payloads<(64c+7):(64c+4)> is set to a value derived by cross-referencing rx_payloads<(64c+3):64c> using Figure 119-3. For example, if rx_payloads<(64c+3):64c> is 0xE then rx_payloads<(64c+7):(64c+4)> is 0x1. If no match to rx_payloads<(64c+3):64c> is found, rx_payloads<(64c+7):(64c+4)> is set to 0000.

Delete steps d2) and e2).

Change step h2) from:
If h<3:0> = 0000, rx_coded_c<1>=1 (invalidate synchronization header)
to:
If rx_payloads<(64c+7):(64c+4)> = 0000, rx_coded_c<1>=1 (invalidate synchronization header)

Change step a3) from:
Set c = 0 and h<3:0> = 0000.
to:
Set c = 0.

In b3) line 39, change:
rx_payloads<(64c+7):(64c+4)> = 0000 (an arbitrary value that is later replaced by s_c)
to:
rx_payloads<(64c+7):(64c+4)> = 0000

Cl **119** *SC* **119.2.5.8** *P* **106** *L* **8** # 65

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

This paragraph leaves out the transcoder and FEC decode functions.

SuggestedRemedy

Change the first part of the paragraph to:

The scrambled idle test-pattern checker utilizes the alignment marker lock state diagram, the PCS deskew state diagram, the FEC decoder, the descrambler and the transcoder operating as they do during normal data reception.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See comment #46, this paragraph is being deleted.

Cl **119** *SC* **119.2.4.8** *P* **103** *L* **1** # 66

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

There currently is no transmit bit ordering diagram.

SuggestedRemedy

Add in the transmit bit ordering diagram as shown in gustlin_3bs_02_0116 as figure 119-10. Remove the editors note and the TBD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add this statement as well (into section 119.2.4.8):
The transmit bit ordering is illustrated in Figure 119-10.

Also modify the diagram as:
Put codeword generation side by side but keep serial nature of data flow.
Add 10-bit symbol distribution to the bottom box.

Cl **119** *SC* **119.2.6.3** *P* **113** *L* **1** # 67

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

All content around the Hi BER mechanism is TBD in the draft.
Hi BER in 10GbE and 40/100GbE is a protection mechanism to prevent operating the link at such a poor BER where there becomes a danger of poor Mean Time To False Packet Acceptance (defined a < the age of the universe). So at these lower speeds the link is taken down at [Tilde]1e-4 BER to prtoect against this.

As was shown in sun_01_1215_logic in the logic ad hoc, with the currently defined mechanism for PCS synchronization, sync/lock is exited after 3 FEC codewords in a row are uncorrectable, and when correcting errors and marking uncorrectable errors, there is no MFFPA concerns since sync is lost long before any MTTFPA conerns come up.

SuggestedRemedy

Remove all references to Hi BER:
Delete the block in figure 119-2 that says BER monitor.

Delete this sentence on page 90:
When the receive channel is in test-pattern mode, the BER monitor process may be disabled

Delete this sentence on page 106:
The BER monitor state diagram is disabled during receive test-pattern mode. Hi_ber definition on page 107.

This editors note on page 110:
[Editor's note: The BER Monitor state diagram is TBD.]

Remove BER monitor from this sentence on page 110:
The PCS shall perform the functions of alignment marker lock, PCS synchronization, BER Monitor, Transmit, and Receive as specified in the respective state diagrams.

The place holder for BER monitor on page 113.

Variable in the receive state machine on page 115.

Hi BER entries in table 119-4.

SM4 from PICS table 119.6.6.1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Make the changes as stated in the suggested remedy, plus:
On page 104, line 19, change:
The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10-6.

To:
The probability that the decoder fails to indicate a codeword with t+1 errors as uncorrected is not expected to exceed 10-16.

[Editor's note: tilde character changed to [Tilde] in Comment text.]

Cl **119** *SC* **119.2.6.3** *P* **112** *L* **1** # 68

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

The PCS synchronization state diagram looks for 3 bad codewords in a row to declare out of lock. There are two codewords that are interleaved to form the PCS lanes, so it is not clear what 3 codewords in a row means.

SuggestedRemedy

The suggested remedy is to go out of lock if either codewordA or codewordB is uncorrectable for 3 times in a row, not if for example A is uncorrectable 2 time along with B being uncorrectable 1 in sequence. This is to prevent burst errors from prematurely taking down the interface since the two codewords are interleaved on a 10b basis.

Make the changes to the PCS sync SM (119-12) and associated variables as detailed in gustlin_3bs_03_0116.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Make the changes to the PCS sync SM (119-12) and associated variables as detailed in gustlin_3bs_03_0116, with the following edits:
From:
Synchronization lock, along with alignment marker lock, are restarted if three FEC codewords in a row are not correctable.
To:
Synchronization lock, along with alignment marker lock, are restarted if three consecutive FEC codewords from the same codeword (A or B) are uncorrectable.

Also in the SM add:
In the CW_BAD state, add a counter reset for each if statement when CW bad(A or B) is false.

Cl **119** *SC* **119.2.4.6** *P* **100** *L* **33** # 69

Gustlin, Mark Xilinx

Comment Type **T** *Comment Status* **A**

The numbering of bits for the FEC codewords is reversed from standard IEEE custom (msb first). The current description follows the precedence established by 802.3bj. But then the nubmering is reversed with a reversing function. This has led to confusion. Simplify this numbering, remove the reversal and stick with the precedence of 802.3bj without the reversal. This is also consistent with the proposed bit ordering diagram.

SuggestedRemedy

Make the changes as specified in gustlin_3bs_04_0116.

Response *Response Status* **C**

ACCEPT.

Cl **120** *SC* **120.5.10.2.3** *P* **139** *L* **27** # 70

Healey, Adam Avago Technologies

Comment Type **E** *Comment Status* **A**

"Gray coding" is used here where "Gray mapping" is used in 120.5.6.1.

SuggestedRemedy

Change "Gray coding" to "Gray mapping".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Gray coding is used more times in the draft than Gray mapping, which is only used in the title of 120.5.6.1 (also true for IEEE Std 802.3bj).
Change the title of 120.5.6.1 to "Gray coding for PAM4 encoded lanes"

Cl **120** *SC* **120.5.10.2.3** *P* **139** *L* **34** # 71

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

The PRBS13Q test pattern is intended to be used for PAM4 transmitter measurements in the same way that PRBS9 is used for PAM2 transmitter measurements. 120.5.10.1.2 does not require that the PRBS9 pattern generator seeds should be randomized or set to specific values. Either this requirement is unnecessary for PRBS13Q or is missing from PRBS9.

SuggestedRemedy

Table 94-11 (as referenced in the editor's note) specified a different seed per physical lane in order to avoid correlated crosstalk during receiver training. In this case, the test pattern is being used for transmitter measurements and not receiver training so the definition of the seed does not seem to be required. Remove the last sentence of the second paragraph and the editor's note.

Response *Response Status* **C**

ACCEPT.

Cl **120** *SC* **120.5.10.2.3** *P* **139** *L* **35** # 72

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

The description of the PRBS13Q test pattern is well-written. However, any possible ambiguity can be eliminated with an example of the first N PAM4 symbols produced by the test pattern generator.

SuggestedRemedy

Include an example of the intended test pattern generator output for a specified seed value.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add after the 2nd paragraph of 120.5.10.2.3:
"For example, if the PRBS13 generator used to create the PRBS13Q sequence is initialized to a seed value of 0000010101011 (with the leftmost bit in S0 and the rightmost in S12), the PRBS13Q sequence will begin with the following Gray coded PAM4 symbols: 10313202201111301031212312100121021210231311112"

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 73

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A** *R_LM*

The transmitter linearity test method defined in 94.3.12.5.1 can misinterpret linear distortion (e.g., settling time of the step) as non-linear level separation mismatch. This incorrectly degrades the R_LM value. Also, the normalization process for ES1 and ES2 forces the outer signal levels to be equal magnitude. Since this may not be case with the actual signal (especially since the mean value is removed), the normalization can actually introduce distortion.

SuggestedRemedy

Measured the signal levels from a PRBS13Q waveform. Define V_A, V_B, V_C, V_D to be average voltage corresponding to the 0, 1, 2, and 3 values, respectively, in the PRBS13Q test pattern. Redefine the normalized signal levels to be measured signal levels, minus the mean of the measured signal levels, and then divided by the largest signal level magnitude. If this method is adopted, the transmitter linearity test pattern defined in 120.5.10.2.4 is no longer required for CDAUI-8 chip-to-chip and more tests can be completed based on the PRBS13Q measurement alone.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
2 improved methods of determining ES1 & ES2 have been proposed: the remedy suggested here, and the "Calculating ES1 and ES2 using Least Squares algorithm" proposal made to the electrical Ad Hoc.
Both methods use PRB13Q test pattern and there is consensus that is a good direction to take. However consensus needs to be achieved on the details of the method.
No change to the draft.
See also comment #118

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 74

Healey, Adam — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

The parameter name "R_LM" is not correctly formatted.

SuggestedRemedy

Change "RLM" to italic text and "LM" to subscript in the parameter name.

Response *Response Status* **C**

ACCEPT.

Cl **120D** *SC* **120D.1** *P* **235** *L* **5** # 75

Healey, Adam — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

Missing space: "in120D.3.2.3".

SuggestedRemedy

Insert the missing space.

Response *Response Status* **C**

ACCEPT.

Cl **120D** *SC* **120D.3.1.1** *P* **236** *L* **53** # 76

Healey, Adam — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

A cross-reference to the definition of the PRBS13Q test pattern could be helpful.

SuggestedRemedy

Add a cross-reference.

Response *Response Status* **C**

ACCEPT.
Change:
"the PRBS13Q test pattern is" to:
"the PRBS13Q test pattern (see 120.5.10.2.3) is"
[Editor's note: Page changed from 237 to 236]

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 77

Healey, Adam — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

In Table 120D-1, the parameter names under "Output waveform" and "Output Jitter and linearity" are not aligned with the values.

SuggestedRemedy

Make necessary adjustments to achieve correct alignment.

Response *Response Status* **C**

ACCEPT.

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 78

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A** *R_LM*

The level separation mismatch ratio (R_LM) in Table 120D-1 is not aligned with the corresponding COM parameter in Table 120D-7.

SuggestedRemedy

In Table 120D-1, change the R_LM value to 0.95.

Response *Response Status* **C**

ACCEPT.
See also comments #117 and #28

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **26** # 79

Healey, Adam — Avago Technologies

Comment Type **E** *Comment Status* **A** *Bucket*

The heading is "Output jitter and linearity" but there are no "linearity" parameters defined in this table row.

SuggestedRemedy

Change heading to "Output jitter".

Response *Response Status* **C**

ACCEPT.

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **5** # 80

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

In Table 120D-1, the "Signaling rate per lane (range)" parameter references 94.3.12.2. The content of 94.3.12.2 is the following: "The 100GBASE-KP4 signaling rate shall be 13.59375 GBd +/- 100 ppm per lane." This material has no bearing on this CDAUI-8 parameter and the reference seems inappropriate.

SuggestedRemedy

Create a local subclause for "Signaling rate and range" that contains information relevant to CDAUI-8 and change the reference in Table 120D-1 to point to this new subclause. An alternative is to simply remove the reference.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Remove the reference.

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **7** # 81

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

There are multiple references to 94.3.12.3 (differential and common-mode voltage requirments). 94.3.12.3 states that the measurement of the transmitter peak-to-peak differential output voltage is to be based on QPRBS13 as defined in 94.2.9.3. For CDAUI-8, this measurement should be based on the PRBS13Q test pattern.

SuggestedRemedy

In the first paragraph of 120D.3.1.1, the exception is noted for the linear fit method. Expand this exception to include the signal level measurement defined in 94.3.12.3.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add footnote to:
"Differential peak-to-peak output voltage (max)",
"Common-mode voltage (max)", "Common-mode voltage (min),
and "AC common-mode output voltage (max, RMS)" cells of Table 120D-1 :
"Measurement uses the method described in 94.3.12.3 with the exception that the PRBS13Q test pattern is used."

Add sentence to 120E.3.1.2 "Signal levels" :
"Unless otherwise noted, differential and common-mode signal levels are measured with a PRBS13Q test pattern."

Cl **120D** *SC* **120D.4** *P* **241** *L* **50** # 82

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

The response to Draft 1.0 comment #53 was to incorporate slides 6 to 8 of the presentation healey_3bs_02_1115 with the exception of the single-ended termination resistance R_d. That value was set to 55 Ohms. However, the A_v, A_fe, and A_ne levels were not adjusted in accordance with that change. The result is that the transmitter modeled by COM has v_f values below the minimum value required for actual transmitters.

SuggestedRemedy

Using the calibration method defined in healey_3bs_02_1115 slide 5, the A_v, A_fe, and A_ne values should be 0.45, 0.45, and 0.65 V respectively.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change A_v, A_fe, and A_ne values to be 0.45, 0.45, and 0.63 V (black) respectively.
Change R_d color from magenta to black.

See also comment #31

Cl **120D** *SC* **120D.3.1.1** *P* **236** *L* **52** # 83

Healey, Adam — Avago Technologies

Comment Type **T** *Comment Status* **A**

There may be an additional exception to the linear fit method defined in 94.3.12.5.2. That subclause specifies that the D_p and N_p values for the linear fit calculation should be 2 and 16 respectively. These may not be the correct values for CDAUI-8.

SuggestedRemedy

The original premise for the D_p and N_p values is that they should span the inter-symbol interference that would be addressed by the reference transmitter and receiver. A "walk-back" effect for pre-cursor compensation must also be considered (see http://www.ieee802.org/3/maint/public/healey_1_0911.pdf). Based on this premise, the D_p value should be 1 plus the number of pre-cursor taps in the transmitter feed-forward equalizer and the N_p value should be D_p+1+N_b where N_b is the number of feedback taps from the COM calculation. For the current CDAUI-8 reference receiver, these values should be D_p = 2 and N_p = 13.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change "with the exception that the PRBS13Q test pattern is used"
to
"with the exceptions that the PRBS13Q test pattern, a D_p value of 2, and an N_p value of 13 are used"

Cl **122** *SC* **122.7.1** *P* **176** *L* **7** # 84

Lewis, David — Lumentum

Comment Type **T** *Comment Status* **R**

As proposed in traverso_3bs_01a_1115, the -DR4 link budget can be shifted down while maintaining adequate Rx sensitivity margin.

SuggestedRemedy

Change launch power in OMAouter minus TDP to -2.5 dBm.
Change outer modulation amplitude (OMAouter), each lane (min) to -1.5 dBm.
Change average launch power, each lane (min) to -4.0 dBm.

Response *Response Status* **C**

REJECT.
No consensus has been reached on these changes to the parameter values. Different values are proposed by comment #55

Cl **122** *SC* **122.7.3** *P* **177** *L* **1** # 85

Lewis, David — Lumentum

Comment Type **T** *Comment Status* **R**

As proposed in traverso_3bs_01a_1115, the -DR4 link budget can be shifted down while maintaining adequate Rx sensitivity margin.

SuggestedRemedy

Change average receive power, each lane (min) to -7 dBm.
Change receiver sensitivity (OMAinner), each lane (max) to -10.3 dBm.

Response *Response Status* **C**

REJECT.
No consensus has been reached on these changes to the parameter values. Different values are proposed by comment #54

Cl **122** *SC* **122.7.3** *P* **177** *L* **38** # 86

Lewis, David — Lumentum

Comment Type **T** *Comment Status* **R**

As proposed in traverso_3bs_01a_1115, the -DR4 link budget can be shifted down while maintaining adequate Rx sensitivity margin.

SuggestedRemedy

Change allocation for penalties (for max TDP) to 2.5 dB.
Change power budget (for max TDP) to 5.5 dB.

Response *Response Status* **C**

REJECT.
See response to comment #84

Cl **122** *SC* **122.8** *P* **178** *L* **4** # 87

Palkert, Tom — Luxtera

Comment Type **T** *Comment Status* **A**

SuggestedRemedy

DR4 section test procedures to be updated per attached presentation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Presentation does not provide a complete proposal for Clause 122 test procedures. The current form is not suitable for inclusion in Clause 122.
A complete proposal is invited to be discussed in an SMF Ad Hoc and a consensus view needs to be established

---

Cl **1** *SC* **1.4** *P* **26** *L* **34** # 88

D'Ambrosia, John — Independent

Comment Type **E** *Comment Status* **A** *Bucket*

Suspected reference in the following statement -
1.4.72f 400GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer
defined in Clause 82 for 400 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

The PCS for 400GbE BASE-R is defined in Clause 119

SuggestedRemedy

change text to following
1.4.72f 400GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 119 for 400 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

Response *Response Status* **C**

ACCEPT.

Cl **117** *SC* **117.1** *P* **76** *L* **41** # 89

D'Ambrosia, John — Independent

Comment Type **E** *Comment Status* **A** *Bucket*

The text below is partially correct, but it is also partially incomplete -

The CDMII is an optional logical interface between the MAC sublayer and the Physical Layer (PHY). The CDAUI-n interface may optionally be used to extend the CDMII.

It is true that the CDMII can be physically extended by the CDAUI-n, but this is done in conjunction with the CDXS sublayer.

SuggestedRemedy

Change text to -

The CDMII is an optional logical interface between the MAC sublayer and the Physical Layer (PHY). The CDXS sublayer in conjunction with the CDAUI-n interface may be used to optionally extend the CDMII.

Response *Response Status* **C**

ACCEPT.

Cl **117** *SC* **117.1.1** *P* **77** *L* **3** # 90

D'Ambrosia, John — Independent

Comment Type **E** *Comment Status* **A** *Bucket*

There is no mention of the CDXS / CDAUI-n under summary of major concepts

SuggestedRemedy

Add Item h}
h) The CDMII can be extended through the use of two CDXS sublayers and a physical instantiation of the CDAUI-n.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add Item h:
h) The CDMII can be extended through the use of two CDXS sublayers with a CDAUI-n between them.

Cl **122** *SC* **122.7.2** *P* **176** *L* **33** # 91

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

RINxxOMA and Optical return loss tolerance are TBD

SuggestedRemedy

Assuming 26 dB ROSA with 4 35 dB connector has an aggregate RL of 19.73 dB, so suggest to use 20 dB for RIN measurement and tolerance

Response *Response Status* **C**

REJECT.
See response to comment #97

Cl **122** *SC* **122.8.7** *P* **180** *L* **6** # 92

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

RIN test condition is TBD

SuggestedRemedy

Assuing 26 dB ROSA RL with 4 of 35 dB connectors has an aggregate RL of 19.73 dB so suggest to use 20 dB

Response *Response Status* **C**

REJECT.
See comment #97

Cl **122** *SC* **122.8.8** *P* **180** *L* **14** # 93

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Transmitter optical waveform need to be measured with a CRU

SuggestedRemedy

The clock recovery unit (CRU) used in the optical waveform measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.

There is currently no agreement as to whether or not a requirement for the transmitter optical waveform will be included.
Also, there is no consensus as yet on CRU corner frequency.

A straw poll of the Task force was taken:
Do you support setting the CRU bandwidth to:

10 MHz for all interfaces (including CDAUI-16)	2
4 MHz for all interfaces (including CDAUI-16)	1
4 MHz for all interfaces except CDAUI-16	0
2 MHz for all interfaces except CDAUI-16	5
I need more information	5
Abstain	23

Cl **122** *SC* **122.8.10** *P* **180** *L* **25** # 94

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Stress receiver sensitivity must tolerate low frequency jitter propagating from the transmitter downstream

SuggestedRemedy

Sinusoidal jitter componnet of stress receiver sensitivity is as following The sinusoidal jitter is used to test receiver jitter tolerance.

The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 87-13 and is illustrated in Figure 87-5.

see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
A complete proposal for how the stressed receiver sensitivity test will be performed has not been provided.

See also response to comment #5 against P802.3bs D1.0 in http://www.ieee802.org/3/bs/comments/P802d3bs_D1p0_comments_final_ID.pdf#page=1

Cl **120D** *SC* **120D.3.1.1** *P* **231** *L* **22** # 95

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

No definition of CRU requirement to measure the output waveform and jitter

SuggestedRemedy

Add footnote to table or subection to be referenced
"The clock recovery unit (CRU) used in the optical waveform measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement."
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120D** *SC* **120D.3.2.2** *P* **240** *L* **14** # 96

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Receiver jitter tolerance must test for full range of sinusoidal jiter componnet allowed to propagate down the link by the Golden PLL.

SuggestedRemedy

Replace Table 120-D-6 with Table 87-13 without identifying any specific test cases. Users will choose how many frequencies is required to gurantee interoperability
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
When the equivalent comment was made against draft 1.0 there was support for increasing the number of measurement frequencies rather than using Table 87-13, however no proposal based on discrete frequencies has been made. There is currently no consensus to change the draft.

Cl **122** *SC* **122.1** *P* **182** *L* **24** # 97

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Fiber optics cable plant RL is TBD

SuggestedRemedy

Assuing 26 dB ROSA RL with 4 of 35 dB connectors has an aggregate RL of 19.73 dB so suggest to use 20 dB

Response *Response Status* **C**

REJECT.
See response to comment #177, against P802.3bs D1.0 in http://www.ieee802.org/3/bs/comments/P802d3bs_D1p0_comments_final_ID.pdf#page=46
As per consensus from SMF Ad Hoc on 6 October 2015: "There was agreement that the various reflection specifications should be dealt with as a group in association with a study of the penalty they cause."
A complete proposal has not yet been made.

Cl **123** *SC* **123.7.1** *P* **198** *L* **39** # 98

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

RINxxOMA and Optical return loss tolerance are TBD

SuggestedRemedy

Assuming 26 dB ROSA with 4 35 dB connector has an aggregate RL of 19.73 dB, so suggest to use 20 dB for RIN measurement and tolerance

Response *Response Status* **C**

REJECT.
See comment #97

Cl **123** *SC* **123.7.1** *P* **198** *L* **42** # 99

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Transmitter reflectance is TBD

SuggestedRemedy

Suggest 26 dB

Response *Response Status* **C**

REJECT.
See comment #97

Cl **123** *SC* **123.7.1** *P* **198** *L* **28** # 100

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Differece in launch OMA is TBD

SuggestedRemedy

Suggest 3 dB

Response *Response Status* **C**

REJECT.
No justification has been provided and the proposed value is not consistent with values in existing Clauses.

Cl **123** *SC* **123.7.2** *P* **199** *L* **28** # 101

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Differece in receive OMA is TBD

SuggestedRemedy

Suggest 3 dB

Response *Response Status* **C**

REJECT.
No justification has been provided and the proposed value is not consistent with values in existing Clauses.

Cl **123** *SC* **123.7.2** *P* **199** *L* **31** # 102

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Receive reflectance is TBD

SuggestedRemedy

Suggest 26 dB

Response *Response Status* **C**

REJECT.
See comment #97

Cl **120E** *SC* **120E.3.1.6** *P* **251** *L* **3** # 103

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

Host output eye must be measured with a reference CRU

SuggestedRemedy

The clock recovery unit (CRU) for the eye measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120E** *SC* **120E.3.2.1** *P* **252** *L* **31** # 104

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

Module output must be measurd with a reference CRU

SuggestedRemedy

The clock recovery unit (CRU) for the eye measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Duplicate of comment #109

Cl **120E** *SC* **120E.3.3.3.1** *P* **255** *L* **20** # 105

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

10 MHz CRU adds extra burden to the host SerDes see
http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf

SuggestedRemedy

Replace 10 Mhz with 4 MHz
Also change Table 120E-4 reference to Table 88-13 with Table 87-13
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120E** *SC* **120E.3.4.1.1** *P* **257** *L* **43** # 106

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

10 MHz CRU adds extra burden to the host SerDes see
http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf

SuggestedRemedy

Replace 10 Mhz with 4 MHz
Also change Table 120E-4 reference to Table 88-13 with Table 87-13
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **123** *SC* **123.7.2** *P* **199** *L* **31** # 107

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Receive reflectance is TBD

SuggestedRemedy

Suggest 26 dB

Response *Response Status* **C**

REJECT.
See comment #97

Cl **120E** *SC* **120E.3.1.6** *P* **251** *L* **3** # 108

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

Host output eye must be measured with a reference CRU

SuggestedRemedy

The clock recovery unit (CRU) for the eye measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Duplication of comment #103

Cl **120E** *SC* **120E.3.2.1** *P* **252** *L* **31** # 109

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R** *CRU bandwidth*

Module output must be measurd with a reference CRU

SuggestedRemedy

The clock recovery unit (CRU) for the eye measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120E** *SC* **120E.3.3.3.1** *P* **255** *L* **20** # 110

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

10 MHz CRU adds extra burden to the host SerDes see
http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf

SuggestedRemedy

Replace 10 Mhz with 4 MHz
Also change Table 120E-4 reference to Table 88-13 with Table 87-13
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120D** *SC* **120D.5.4.3** *P* **245** *L* **22** # 111

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A**

The current channel operating margin of 'Greater than or equal to 2dB' does not take into account several potential non-idealities in a typical PAM4 receiver.

SuggestedRemedy

Change the COM margin to 3dB. An updated presentation will be submitted in support of this comment.

Response *Response Status* **C**

ACCEPT.

Straw Poll
Change COM margin to 3dB 8
Leave COM margin at 2dB 3

Cl **120E** *SC* **120E.1** *P* **246** *L* **52** # 112

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A**

Although the draft text mentions that 'the lanes are AC-coupled within the module', the AC coupling frequency is not specified.

SuggestedRemedy

Please add the line 'the low-frequency 3dB cutoff of the AC coupling within the module shall be less than 50kHz'.

Response *Response Status* **C**

ACCEPT.

Cl **120E** *SC* **120E.1.1** *P* **247** *L* **53** # 113

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A**

The current draft sets the BER limit at 10^-6. The CDAUI-8 FEC does not need the BER to be so low.

SuggestedRemedy

Change the BER limit to 10^-5. An updated presentation will be submitted in support of this comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #61

Cl **120E** *SC* **120E.4.2** *P* **258** *L* **47** # 114

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A**

The current eye width and height measurement method does not allow for a large enough pre-cursor in the module TX necessary to overcome the channel loss. The receiver may need a large pre-cursor but the eye width and height could be too low with the larger pre-cursor.

SuggestedRemedy

modify the step 2) in 120E.4.2 to allow a pre-cursor term to be added to the reference receiver. A presentation will be submitted in support of this comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
However developing a solution needs more consensus building.

Cl **120E** *SC* **120E.3.3.3.1** *P* **254** *L* **53** # 115

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **R** *CRU bandwidth*

The reference CRU bandwidth is currently set at 10MHz. Several implementation styles may find this setting too high.

SuggestedRemedy

Change the reference CRU bandwidth to 4MHz. A presentation will be submitted in support of this comment

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120E** *SC* **120E.3.4.1.1** *P* **257** *L* **16** # 116

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **R** *CRU bandwidth*

The current reference CRU bandwidth of 10MHz may be too high for several implementation styles.

SuggestedRemedy

Change the reference CRU bandwidth to 4MHz. A presentation will be submitted in support of this comment.

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 117

Hegde, Raj — Broadcom Corporation

Comment Type **E** *Comment Status* **A** *R_LM*

The Level Seperation mismatch ratio RLM(min) value in Table 120D-1 does not match the same in the COM Parameters Table 120D-7 (Page 242 Line 5)

SuggestedRemedy

Change the RLM (min) value in Table 120D-1 from 0.92 to 0.95

Response *Response Status* **C**

ACCEPT.
See also comments #28 and #78

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **18** # 118

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A** *R_LM*

Currently, the entry in the Reference column for RLM(min) in Table 120D-1 points to 94.3.12.5.1 for the transmitter linearity measurement method. This measurement method allows for large asymmetry between -1/3 and +1/3 levels.

SuggestedRemedy

Change the measurement method to tighten the allowed asymmetry in the TX output. Note that this topic was discussed in a presentation at the 12/07/15 Electrical Ad-hoc meeting. An updated presentation will be submitted in support of this comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #73

Cl **120D** *SC* **120D.3.1.1** *P* **237** *L* **24** # 119

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **R** *SNR_Tx*

In Table 120D-1, Signal-to-noise-and-distortion ratio (min) is set at 31dB. With PAM4 transmitters having a richer variety of transitions and more mechanism to generate distortion, a relaxed budget would allow for ease of implementation. This topic was discussed in a presentation at the Electrical Ad-hoc on 11/30/15.

SuggestedRemedy

Lower the limit to 29dB. An updated presentation will be submitted in support of this comment.

Response *Response Status* **C**

REJECT.
Change COM SNR_Tx value to 29dB for Test 1 (small package), and 31.1dB for Test 2 (large package), in black.
Change the SNDR limit to 29dB.
See also Comments #32, and #122.

Straw Poll
Accept above as comment resolution 2
Make no change to the draft 1
Room count 14
Insufficient consensus for a change at this time, further analysis required.

Cl **120D** *SC* **120D.3.2.1** *P* **239** *L* **35** # 120

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **D**

In Table 120D-5, for Receiver Interference Tolerance parameters, the performance metric used is RS-FEC Symbol Error Ratio. In CDAUI-8, the FEC error count may not be available to all the receivers.

SuggestedRemedy

Use Bit Error Ratio for that particular lane as the performance metric. Change 'RS-FEC Symbol Error Ratio' to 'Bit Error Ratio' This topic was addressed in a presentation at the Electrical Ad-hoc on 12/07/15.
An updated presentation will be submitted in support of this comment.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **120D** *SC* **120D.3.2.2** *P* **240** *L* **13** # 121

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **D**

In Table 120D-6, for Receiver Jitter Tolerance parameters, the performance metric used is RS-FEC Symbol error ratio. In CDAUI-8, the FEC error count may not be available to all the receivers.

SuggestedRemedy

Use Bit Error ratio as the performance metric instead. Change 'RS-FEC Symbol error ratio' to 'Bit error ratio' An updated presentation will be submitted in support of this comment.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **120D** *SC* **120D.4** *P* **242** *L* **7** # 122

Hegde, Raj — Broadcom Corporation

Comment Type **T** *Comment Status* **A** *SNR_Tx*

Updates to the COM table 120D-7:
1) The transmitter signal-to-noise ratio (SNR_TX) at 31dB doesn't accomodate for higher levels of distortions in PAM4.
2) The CDAUI-8 FEC does not require the detector error ratio to be at 10^-6.

SuggestedRemedy

1) Relax the SNR_TX to 29dB
2) Increase the detector error ratio to 10^-5.

An updated presentation in support of these comments will be submitted

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Increase the detector error ratio to 10^-5 as there seems to be consensus on this (see comment #61),
Increase the SER in Tables 120D-5 and 120D-6 to 10-4.
See resolution to Comment #119 for SNR_Tx.

Cl **119** *SC* **119.2.4.6** *P* **99** *L* **50** # 123

Nicholl, Gary — Cisco Systems

Comment Type **T** *Comment Status* **R**

Shouldn't we also specify the values of "t" and "m" in the sentence "The PCS sublayer shall implement RS(544,514)" I think it is important to know that RS FEC we are using is based on 10bit symbols and has the ability to correct up to 15 symbols per FEC codeword.

SuggestedRemedy

Change "The PCS sublayer shall implement RS(544,514)" to "The PCS sublayer shall implement RS(544,514,15,10). After this is defined once you can shorten it to RS(544,514) in future references.

Response *Response Status* **C**

REJECT.

It is stated that is it a 10-bit symbol:
Galois Field GF(2^10) where the symbol
size is 10 bits.

And t=15 is stated in sub clause 119.2.5.3.
This is all consistent with the descriptions in clause 91.

Cl **119** *SC* **119.2.4.6** *P* **99** *L* **50** # 124

Nicholl, Gary — Cisco Systems

Comment Type **T** *Comment Status* **A**

I am not sure this is technically correct "The PCS interleaves two FEC codewords, therefore each k-symbol message corresponds to one half of a group of 40 interleaved 257-bit blocks produced by the transcoder (with the exception of the alignment marker blocks)". This makes it sound like the alignment marker blocks are not FEC encoded, which I don't beleive is the intent ? Also due to the 10bit preFEC interleaving each FEC code word does not contain 20 (one half of 40) 257-bit blocks produced by the transcoder.

SuggestedRemedy

Please clarify.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
The PCS interleaves two FEC codewords, therefore each k-symbol message corresponds to one half of a group of 40 interleaved 257-bit blocks produced by the transcoder (with the exception of the alignment marker blocks)

to:
The PCS distributes a group of 40 257-bit blocks on a 10-bit round robin basis to two 5140-bit blocks, therefore each 514-symbol message corresponds to one half of a group of 40 257-bit blocks produced by the transcoder (with the exception of the alignment marker blocks being directly inserted periodically into the data stream)

[Editor's note: line 50 added to the comment]

Cl **119** *SC* **119.2.4.6** *P* **99** *L* **52** # 125

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

"Each code is based on the generating " ..We seem to be a bit inconsistent in using the terms FEC codeword, FEC code or FEC block. I think we should pick one term and use it consistently throughout the document. I recommend FEC codeword.

SuggestedRemedy

Change "Each code is based on the generating " to " Each codeword is based on the generating "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Each code is based
to:
The RS(544,514) code is based

and change (page 101 line 22):
The coefficients of the generator polynomial for each code are presented in Table 119-2. Example codewords for each code are provided in Annex 91A.
To:
The coefficients of the generator polynomial for the RS(544,514) code are presented in Table 119-2. Example codewords for the RS(544,514) code are provided in Annex 91A

Cl **119** *SC* **119.2.4.7** *P* **102** *L* **15** # 126

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **A**

Suggesting adding some text to explain what the pseudo code above actually does.

SuggestedRemedy

Add some text to get across the message that the individual PCS lanes on the PMA service interface are comprised of an interleave of 10b RS FEC symbols from the two FEC codewords. perhaps include the disagram on slide 6 of http://www.ieee802.org/3/bs/public/15_11/gustlin_3bs_03_1115.pdf. It would also help to explain why the data from the two FEC codewords is played out in such a stange looking order.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Once the data has been FEC encoded, two FEC codewords are interleaved before the data is distributed to each PCS lane.
To:
Once the data has been FEC encoded, two FEC codewords are interleaved on a 10-bit basis before the data is distributed to each PCS lane.

In addition, see the diagram as added in comment #66 which should clear up any confusion.

Cl **119** *SC* **119.2.5.1** *P* **103** *L* **46** # 127

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **A** *Bucket*

Add "alignment" in front of markers.

SuggestedRemedy

Change "Note that alignment marker lock is achieved before FEC codewords are processed and therefore the markers are processed in a high error probability environment" to "Note that alignment marker lock is achieved before FEC codewords are processed and therefore the alignment markers are processed in a high error probability environment..

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.5.1** *P* **103** *L* **52** # 128

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **A** *Bucket*

I thought we were using the term "PCS Lane" rather than "FEC Lane" Also a proposed change in the order of the text. Also change "FEC receive function" to "PCS receive function" to be consistent with the rest of the Clause.

SuggestedRemedy

Change "The FEC receive function shall support a maximum Skew of 180 ns between FEC lanes and a maximum Skew Variation of 4 ns" to "The PCS receive function shall support a maximum Skew of 180 ns, and maximum Skew Variation of 4 ns, between PCS Lanes."

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **22** # 129

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

As detailed in "http://www.ieee802.org/3/bs/public/adhoc/logic/dec11_15/sun_01_1215_logic.pdf" there are no practical options to bypass error correction. Remove any reference to "error correction bypass" in the document".

SuggestedRemedy

Remove lines 22 to 28 "The Reed-Solomon decoder may provide the option to perform error detection without error correction to reduce the delay contributed by the RS-FEC sublayer. The presence of this option is indicated by the assertion of the FEC_bypass_correction_ability variable (see 119.3). When the option is provided, it is enabled by the assertion of the FEC_bypass_correction_enable variable (see 119.3). NOTE-The PHY may rely on the error correction capability of the RS-FEC to achieve its performance objectives. It is recommended that acceptable performance of the underlying link is verified before error correction is bypassed. "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Also remove the MDIO variable from table 119-3 and 119-4. And RF6 from 119.6.4.2. Fix the numbering in 119.6.4.2.
With editorial license to clean up any impacted text.

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **31** # 130

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

Remove the reference to "FEC correction bypass"

SuggestedRemedy

Change "When the Reed-Solomon decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled)." to "When the Reed-Solomon decoder determines that a codeword contains errors that were not corrected "....

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.5.3** *P* **104** *L* **33** # 131

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

I don't think it is technically correct to include the word "two" in "within the two associated codewords" Why are there "two" associated FEC codewords ? The previous part of the same sentence, only refers to the FEC decoder determinering that there are errors in a "single" FEC codeword. There is no mention of "two associated FEC codewords" . [Commenter's comment. This FEC codeword interleaving really complicates the description!]

SuggestedRemedy

Change "within the two associated codewords,.." to "within the associated codeword,.."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
When the Reed-Solomon decoder determines that a codeword contains errors (when the bypass correction feature is enabled) or contains errors that were not corrected (when the bypass correction feature is not supported or not enabled), it shall ensure that, for every 257-bit block within the two associated codewords,
To:
When the Reed-Solomon decoder determines that a codeword contains errors that were not corrected (and the error indication bypass feature is not supported or not enabled), it shall ensure that, for every 257-bit block that contains data from the uncorrected codeword,

Cl **119** *SC* **119.2.5.4** *P* **104** *L* **40** # 132

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **A**

Is this the first time we have used the term 'message' bits ? I don't think the word 'message' is required.

SuggestedRemedy

Change "The first 2056 message bits in every 8192nd codeword" to "The first 2056 bits in every 8192nd codeword"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #45

Cl **119** *SC* **119.2.4.4** *P* **99** *L* **23** # 133

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

The note "163 840 257-bit blocks between AM insertions" is somewhat ambiguous. Do the "163 840 x 257-bit blocks" include the alignment markers and 136 bit pad ? I don't believe they do, but that is not the impression that Figure 119-7 gives. Also are the "163 840 x 257-bit blocks" at the aggregrate or the PCS lane level. At this point in the block diagram (Figure 119-2) we have no distributed the data into 16 x PCS lanes, so I presume the reference is to the aggregate data stream which is not what Figure 119-7 infers.

SuggestedRemedy

Please clarify. If as I suspect that the alignment marker insertion occurs on the aggregate data stream before distribution to PCS lanes, then I would redraw the figure to make this clear. Also need to clarify whether the "'163 840 x 257-bit blocks" include the alignment markers and 136 bit pad or not.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
To make the text clearer change the following (pg 96 line 25).
Change:
The group of alignment markers shall be inserted once every 163 840 257-bit blocks.
To:
The group of alignment markers shall be inserted so they appear every 163 840 257-bit blocks

Cl **119** *SC* **119.2.6.3** *P* **110** *L* **2** # 134

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

Given that the alignment marker lock operates independently on each PCS lane and each PCS lane is an interleave of 10but symmbols from two different FEC coderwords, the following sentence is a little ambiguous "Each alignment marker lock process looks for two valid alignment markers 8192 FEC codewords apart to gain alignment marker lock"

SuggestedRemedy

Please clarify what is meant by " 8192 FEC codewords apart" on a PCS lane which comprises an interleave of two separate codewords. Perhaps it would be better to identify the alignment marker spacing per PCS lane in terms of 10-bit RS symbols instead ?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Each alignment marker lock process looks for two valid alignment markers 8192 FEC codewords apart to gain alignment marker lock
to:
Each alignment marker lock process looks for two valid alignment markers 278 528 10-bit Reed-Solomon symbols apart (on a per PCS lane basis) to gain alignment marker lock

Cl **119** *SC* **119.2.6.3** *P* **110** *L* **3** # 135

Nicholl, Gary Cisco Systems

Comment Type **T** *Comment Status* **A**

Two comments on this sentence "Once in lock, a lane will go out of alignment marker lock when three FEC blocks in a row are not correctable." Firstly use 'codeword' instead of 'block', and secondly what does 'three FEC blocks' mean on an individual PCS lane this is comprised of an interleave of two separate codeword ? Doesn't the term FEC codeword only have significance at the aggregate data stream and not at the individual PCS lane level ? If the intent is to use feedback from the aggregate FEC decode to all 16x alignment lock state machines, then it is impossible for an indivudal PCS lane to go out of alignment lock as is suggested in the text.

SuggestedRemedy

Please clarify.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
Once in lock, a lane will go out of alignment marker lock when three FEC blocks in a row are not correctable.

To:
Once in lock, a lane will go out of alignment marker lock only when the PCS synchronization state machine signals restart_lock.

Cl **45** *SC* **45.2.1.116a** *P* **44** *L* **2** # 136

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

The current text only specifies a single recommened CTLE setting register for all 16 lanes of a CDAUI-16 chip-to module interface. In keeping with all CAUI-4 module implementations there should be a separate recommended CTLE rgister for each individual CDAUI-16 lane. A single register (and CTLE setting) for all 16 lanes is too restrictive. The whole point of the MLD protocol was to allow board designers flexibility in routing of the indivudal lanes of a CAUI-4 or CDAUI-16 interface.

SuggestedRemedy

Please add a 'recommended CTLE setting' register for each indiviudal lane of the CDAUI-16 chip-to-module interface.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #39

Cl **119** *SC* **119.1.5** *P* **89** *L* **3** # 137

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

Figure 119-2. Don't we need a "postFEC Interleave" block in the Rx data path corresponding to the "preFEC distribution" block in the Tx data path.

SuggestedRemedy

Add a "postFEC Interleave" block into Figure 119-2.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add a block after the FEC decode in the RX path called: Post FEC Interleave.

Add a sublayer paragraph after the Reed-Solomon decoder sublayer with details, with editiorial license. This will move some of the text out of 119.2.5.3.

Cl **119** *SC* **119.2.1** *P* **90** *L* **11** # 138

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **A**

I thought we were referring to this '16 encoded bit streams' as PCS Lanes (see Clause 120). If this is the case then it might be clearer to also refer to them here. In fact we use the term "PCS Lane" on line 32 of the same page.

SuggestedRemedy

Change "When communicating with the PMA, the 400GBASE-R PCS uses 16 encoded bit streams. Per direction (RX or TX), these serial streams originate from a common clock but may vary in phase and skew dynamically." to
"When communicating with the PMA, the 400GBASE-R PCS uses 16 encoded bit streams, where each bit stream is referred to as a PCS Lane (PSCL). Althought the 16 PCS lanes for each direction (TX and RX) originate from a common clock, they may vary in phase and skew dynamically".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
"When communicating with the PMA, the 400GBASE-R PCS uses 16 encoded bit streams. Per direction (RX or TX), these serial streams originate from a common clock but may vary in phase and skew dynamically."
to:
"When communicating with the PMA, the 400GBASE-R PCS uses 16 encoded bit streams (also known as PCS lanes). Per direction (RX or TX), the PCS lanes originate from a common clock but may vary in phase and skew dynamically."

Cl **119** *SC* **119.2.1** *P* **90** *L* **39** # 139

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

There is no mention of the reverse of the process mentioned in line 20, i.e. "The data stream is distributed to two FEC codewords "

SuggestedRemedy

Add some text to make it clear that the "the data stream from the two FEC codewords are inteleaved" before going on to mention that "Next the PCS removes alignment markers, descrambles the data, transcodes the data back to 64B/66B and then decodes the 64B/66B encoded data."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See the response to comment #8

Cl **119** *SC* **119.2.3.1** *P* **91** *L* **20** # 140

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **D**

This is very confusing "The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. " Especially when binary values are shown in Figure 119-3 in the order of transmission (so you have to transpose the hex values but not the binary values). This means the binary value of a data control block is actually 0x10 whereas I had always heard it refered to as 0x01.

SuggestedRemedy

No proposed resolution, just saying :)

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

No proposed remedy.
This is consistent with the lower Ethernet rates. See 49.2.4.1, 82.2.3.1, etc.

Cl **119** *SC* **119.2.4.4** *P* **96** *L* **9** # 141

Nicholl, Gary Cisco Systems

Comment Type **ER** *Comment Status* **A** *Bucket*

It probably makes sense to clarify (or remind everyone) that we are dealing with 16 PCS lanes.

SuggestedRemedy

Change "In order to support deskew and reordering of individual PCS lanes " to "In order to support deskew and reordering of the 16 individual PCS lanes"

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.4** *P* **96** *L* **34** # 142

Nicholl, Gary Cisco Systems

Comment Type **E** *Comment Status* **A** *Bucket*

For clarity perhaps we should add PMA service interface to the end of "What is shown in Table 119-1 is how the alignment markers 34 appear on the PCS lanes."

SuggestedRemedy

Change "What is shown in Table 119-1 is how the alignment markers appear on the PCS lanes." to " The format shown in Table 119-1 is how the alignment markers appear on the PCS lanes at the PMA service interface"

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.4** *P* **97** *L* **4** # 143

Nicholl, Gary Cisco Systems

Comment Type **TR** *Comment Status* **A**

The encoding description in the header for Table 119-1 is incorrect. There are no BIP3 or BIP7 octets.

SuggestedRemedy

Remove the head description {M0,M1,M2, BIP3,M4,M5,M6, BIP7} from Table 119-1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #10.

Cl **119** *SC* **119.2.4.4** *P* **98** *L* **25** # 144

Nicholl, Gary — Cisco Systems

Comment Type **E** *Comment Status* **A** *Bucket*

Figure 119-6. The aligment marker comprises of 13 x 10bit FEC symbols per PCS lane.
Isn't that unlucky ??

SuggestedRemedy

No proposed remedy, except don't run 400G on Friday the 13th !

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

See response to comment #146

Cl **00** *SC* **0** *P* *L* # 145

Anslow, Pete — Ciena

Comment Type **T** *Comment Status* **A**

120E.3.3.3.1 and 120E.3.4.1.1 allow a test pattern of "Pattern 5, Pattern 3, or a valid 400GBASE-R signal" as found in Table 122-9.
Pattern 5 is scrambled idle, but pattern 3 is "TBD to replace "PRBS31""
The properties of a PRBS31Q pattern defined as per 120.5.10.2.3 "PRBS13Q test pattern" but using a PRBS31 sequence in place of PRBS13, were analysed in http://www.ieee802.org/3/bs/public/adhoc/logic/dec11_15/anslow_01_1215_logic.pdf and found to be adequate for this purpose.

SuggestedRemedy

Define a PRBS31Q test pattern in a subclause of 120.5.10.2 as per 120.5.10.2.3 but with a PRBS31 pattern in place of PRBS13.
In Tables 122-9 and 123-10 define pattern 3 as "PRBS31Q".
Make appropriate changes to Clause 45 to allow this pattern to be controlled.
All with editorial license.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy including a checker.

Cl **119** *SC* **119.2.4.4** *P* **96** *L* **40** # 146

Anslow, Pete — Ciena

Comment Type **T** *Comment Status* **D**

The alignment marker encodings in Clause 119 are TBD.
A proposed set of markers was analysed in http://www.ieee802.org/3/bs/public/adhoc/logic/dec11_15/anslow_01_1215_logic.pdf and discussed at the 11 December Logic Ad Hoc call, where it was noted that there is a "shoulder" on the 4:1 interleaved lanes clock content characteristic. On the call it w3as proposed to change the common part of the marker to be 48 bits long to reduce this effect.
Marker encoding with 48-bit common part (taken from AM6 for 100GbE as it has more transitions than AM0) and 48-bit unique part has been analysed with significantly improved results. It is intended to show these results in the January 8 Logic Ad Hoc.

SuggestedRemedy

Change the common part of the alignment markers to be the first three bytes of AM6 for 100GbE followed by their inverse: "0x9A, 0x4A, 0x26, 0x65, 0xB5, 0xD9".
Set the unique part of the alignment markers to be the first three bytes of the unique markers proposed in anslow_01_1215_logic.pdf followed by their inverse:
0x9E, 0xEB, 0x27, 0x61, 0x14, 0xD8
0x50, 0x74, 0x88, 0xAF, 0x8B, 0x77
0xB4, 0xB7, 0xEA, 0x4B, 0x48, 0x15
0xE4, 0xFB, 0xF1, 0x1B, 0x04, 0x0E
0xDC, 0x58, 0xEE, 0x23, 0xA7, 0x11
0xBD, 0xA9, 0xBF, 0x42, 0x56, 0x40
0x97, 0x67, 0x77, 0x68, 0x98, 0x88
0x24, 0x35, 0xA5, 0xDB, 0xCA, 0x5A
0x57, 0x64, 0x51, 0xA8, 0x9B, 0xAE
0x28, 0xF9, 0x3E, 0xD7, 0x06, 0xC1
0xCB, 0xD1, 0xAD, 0x34, 0x2E, 0x52
0x5E, 0x1E, 0x38, 0xA1, 0xE1, 0xC7
0x19, 0x98, 0xF9, 0xE6, 0x67, 0x06
0x84, 0xEC, 0x20, 0x7B, 0x13, 0xDF
0x13, 0xA4, 0xED, 0xEC, 0x5B, 0x12
0x3F, 0x8A, 0xBE, 0xC0, 0x75, 0x41

This makes the AMs 96 bits long, which will fit in 6 x 257-bit blocks with 6 bits set to the free running PRBS9.
Make the above changes with editorial license.

Proposed Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

[Editor's note: page changed from 119 to 96]

Cl **120D** *SC* **120E.1.1** *P* **247** *L* **51** # 147

Anslow, Pete Ciena

Comment Type **T** *Comment Status* **A**

120E.1.1 says "The bit error ratio (BER) when processed according to Clause 120 shall be less than 10-6 provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.223) of less than 6.2 × 10-13 for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and Clause 119."
Firstly, 6.2 × 10-13 should be 6.2 × 10-11.
Secondly, with a BER of 1E-6 and random errors, the resulting FLR would be 4E-50. Even with a BER of 1E-5 and random errors, the resulting FLR would be 4E-34 which is still unmeasureable.

SuggestedRemedy

Change the content of 120E.1.1 to be just: "The bit error ratio (BER) shall be less than XXX." where "XXX" is 10-6 or as changed by other comments.

Response *Response Status* **C**

ACCEPT.

Cl **120C** *SC* **120C.3.2** *P* **229** *L* **43** # 148

Dawe, Piers Mellanox

Comment Type **T** *Comment Status* **A**

Chip-to-module CDAUI-16 is FEC protected with a BER spec of 1e-6, so extrapolating the module output to 1e-15 as in chip-to-module CAUI-4 is irrelevant. The spec in 109B.3.2.1.2, Eye opening using measurement method B, is more appropriate, and allows the legacy non-FEC method as an option.

SuggestedRemedy

Change "A CDAUI-16 module output shall meet all specifications in 83E.3.2 with the exception that the signaling rate per lane is 26.5625 Gbd ± 100 ppm." to:
A CDAUI-16 module output shall meet all specifications in 83E.3.2 with the exception of eye height, eye width, and vertical eye closure and signaling rate. A CDAUI-16 module output shall meet the eye height, eye width, and vertical eye closure specified in 109B.3.2.1 for a PHY that includes an RS-FEC sublayer. The signaling rate of each lane is 26.5625 GBd ± 100 ppm."
In 120C.4, change "The CDAUI-16 chip-to-module measurement methodology is as defined in 83E.4 with the following exceptions:" to "The CDAUI-16 chip-to-module measurement methodology is as defined in 83E.4 and 109B.4 with the following exceptions:"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change:
"A CDAUI-16 module output shall meet all specifications in 83E.3.2 with the exception that the signaling rate per lane is 26.5625 Gbd ± 100 ppm." to:
"A CDAUI-16 module output shall meet all specifications in 83E.3.2 with the following exceptions:
- The signaling rate per lane is 26.5625 Gbd ± 100 ppm.
- The eye height, eye width, and vertical eye closure are as specified in 109B.3.2.1 for a PHY that includes an RS-FEC sublayer. "

In 120C.4, add an exception:
"- The eye height, eye width, and vertical eye closure are measured as specified in 109B.3.2.1 for a PHY that includes an RS-FEC sublayer. "
Remove editor's note.

Cl **120E** *SC* **120E.3.1** *P* **249** *L* **35** # 149

Dawe, Piers Mellanox

Comment Type **T** *Comment Status* **D**

The C2M CAUI-4 host output 20% to 80% transition time min is 10 ps. Here for C2M CDAUI-8, the host compliance board is the same, the signalling rate is a little higher, a good transmitter should be a little faster and may be using some FFE to get a reasonable opening of a multilevel eye. So a slightly lower limit should apply. I can't see how a very fast host output would ever be worse than a compliant slow output. We could consider removing this spec or changing to a slew rate spec, but if we don't:

SuggestedRemedy

Change magenta TBD to magenta 9. Update the PICS.

Proposed Response *Response Status* **Z**

This comment was WITHDRAWN by the commenter.

It conflicted with the commenters duplicate comment #151 on the same item.

Cl **120E** *SC* **120E.3.2.1** *P* **252** *L* **32** # 150

Dawe, Piers Mellanox

Comment Type **T** *Comment Status* **A** *Transition time*

We should spec or test the module output for the worst case, which is when it's driving a high-loss host, which won't output a fast maximum-amplitude signal. That's why 83E.3.2.1 has 19 ps here.

SuggestedRemedy

Change 12 ps to 19 ps.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change "The crosstalk generator is
calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of
12 ps." to "The crosstalk generator is
calibrated at TP1a with target differential peak-to-peak amplitude of 900 mV and target transition time of
19 ps." (19ps in black)

Change 12 ps to 19 ps (black) for module output crosstalk aggressor transition time.

Cl **120E** *SC* **120E.3.1** *P* **249** *L* **35** # 151

Dawe, Piers Mellanox

Comment Type **T** *Comment Status* **A**

The minimum host output transition time in CAUI-4 and CEI-28G-VSR is 10 ps. Here for C2M CDAUI-8, the driver could be faster and may be using more FFE to get a reasonable opening of a multilevel eye, so a lower limit could apply. It seems that the practical effect of this spec is to stop hosts using high output emphasis (but with PAM4, the eye mask controls that too), and to deter implementers of very fast (=good) drivers with low loss host lanes.

SuggestedRemedy

We could change magenta TBD to magenta 10 ps, same as CAUI-4, or move to a slew rate spec, or consider deleting the row, as unnecessary, or leave it as it is for another cycle.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
1) Change transition time value in Table 120E-1 to 10ps (black).
2) Change transition time value in Table 120E-2 to 9.5ps (black).
3) Change PICS item TH10 (Host transition time) to 10ps (black).
4) Change PICS item TM8 (Module transition time) to 9.5ps (black).
Give editorial license to update any other affected text.

Cl **120E** *SC* **120E.3.2** *P* **252** *L* **11** # 152

Dawe, Piers Mellanox

Comment Type **T** *Comment Status* **A** *Transition time*

The minimum module output transition time in CEI-28G-VSR is 9.5 ps. Here for C2M CDAUI-8, the transmitter should be a little faster and may be using some FFE to get a reasonable opening of a multilevel eye, so a lower limit should apply. We would expect the module to look faster than the host (lower cmpliance board loss). On the other hand, the observation filter is a little slower than in OIF. It seems that the practical effect of this spec is to stop modules using high output emphasis (but with PAM4, the eye mask controls that too), and to deter implementers of very fast (=good) modules. So it should not be too restrictive.

SuggestedRemedy

We could change magenta TBD to magenta 10 ps, or move to a slew rate spec, or leave it as it is for another cycle.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
See response to comment #151

Cl **120E** *SC* **120E.4.2** *P* **258** *L* **54** # 153

Dawe, Piers — Mellanox

Comment Type **T** *Comment Status* **R**

"Calculate the time center of the middle eye width (TCmid) as the mid-point in time between MIDCDFR and MIDCDFL with a value of 10^-6.": there are more practical ways to find the decision time: a real CDR should not take that many measurements to get its timing, and the measurement will be more reproducible at a higher probability.

SuggestedRemedy

TCmid should be either half way between the mean crossing times as usual, or, if it can be shown to be an improvement on that, half way between the 10^-3 contours, as in 10GBASE-R.

Response *Response Status* **C**

REJECT.
The method used to determine Tcmid is based on the method used to determine eye height and width in Annex 83E, which was based on a 10^-6 probability.

Cl **120E** *SC* **120E.3.3.3** *P* **254** *L* **42** # 154

Dawe, Piers — Mellanox

Comment Type **T** *Comment Status* **A**

The difference between Eye width and ESMW is too large

SuggestedRemedy

Increase ESMW to e.g. 0.35 UI (0.05 UI less than Eye width), or 0.4 UI.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Set the value of ESMW in Table 120E-4 to 0.4 UI (in black)

Cl **123** *SC* **123.8.8** *P* **202** *L* **42** # 155

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Transmitter optical waveform need to be measured with a CRU

SuggestedRemedy

The clock recovery unit (CRU) used in the optical waveform measurement has a corner frequency of 4 MHz and a slope of 20 dB/decade. When using a clock recovery unit as a clock for BER measurements, passing of low- frequency jitter from the data to the clock removes this low-frequency jitter from the measurement.
see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93.
[Editor's note: This comment was sent after the close of the comment period.]

Cl **123** *SC* **123.8.10** *P* **202** *L* **53** # 156

Ghiasi, Ali — Ghiasi Quantum LLC

Comment Type **TR** *Comment Status* **R**

Stress receiver sensitivity must tolerate low frequency jitter propagating from the transmitter downstream

SuggestedRemedy

Sinusoidal jitter componnet of stress receiver sensitivity is as following The sinusoidal jitter is used to test receiver jitter tolerance.

The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table 87-13 and is illustrated in Figure 87-5.

see http://www.ieee802.org/3/bs/public/15_09/ghiasi_3bs_01b_0915.pdf for background material and http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf plan to consolidate these two presentation for Atlanta as ghiasi_3bs_01_0116.pdf

Response *Response Status* **C**

REJECT.
Consensus on change of CRU bandwidth has not been achieved. See comment #93.
[Editor's note: This comment was sent after the close of the comment period.]