

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120E SC 120E.3.1.6 P 372 L 41 # r02-1
 Anslow, Peter Ciena Corporation

Comment Type T Comment Status X

Comment r01-43 against D3.1 added:
 "so that the symbols on each lane are not correlated within the PMD" in 120E.3.1.6,
 120E.3.2.1, 120E.3.3.2.1 and 120E.3.4.1.1.
 But the pattern in question is being used for measurement of:
 Host output eye width and eye height
 Module output eye width and eye height
 Host stressed input test
 Module stressed input test
 which have nothing to do with the PMD sublayer

SuggestedRemedy

In 120E.3.1.6, 120E.3.2.1, 120E.3.3.2.1 and 120E.3.4.1.1 delete "within the PMD"

Proposed Response Response Status O

CI 121 SC 121.7 P 221 L 16 # r02-2
 King, Jonathan Finisar Corporation

Comment Type TR Comment Status X

The changes in Draft 3.2 to the TDECQ reference equalizer and reference receiver
 bandwidth mean that transmitters that just passed D3.1 TDECQ will have a D3.2 TDECQ
 value which is 0.9 dB higher.

Similarly for clauses 122 and 124

SuggestedRemedy

Subject to task force review, implement the changes in king_3bs_01_0617, with editorial
 license

Proposed Response Response Status O

CI 119 SC 119.2.6.3 P 170 L 19 # r02-3
 Gustlin, Mark Xilinx, Inc.

Comment Type T Comment Status X

I = 139264 is incorrect for 200GE, it should be 278528, same as for 400GE.

SuggestedRemedy

Change "Each alignment marker lock process looks for two valid alignment
 markers i x 10-bit Reed-Solomon symbols apart (on a per PCS lane basis, where i = 139
 264 for a 200GBASE-R PCS and i = 278 528 for a 400GBASE-R PCS)" to "Each alignment
 marker lock process looks for two valid alignment
 markers 278 528 x 10-bit Reed-Solomon symbols apart on a per PCS lane basis"

Proposed Response Response Status O

CI 119 SC 119.2.5.3 P 164 L 10 # r02-4
 Koehler, Daniel

Comment Type E Comment Status X

Defines the assertion time for hi_ser as a time from 60ms to 75ms which differs from the
 variable definition in 119.2.6.2.2 which defines deassertion when less than threshold within
 8192 codewords.

SuggestedRemedy

Update 119.2.6.2.2 variable definition to include the time.

Proposed Response Response Status O

CI 119 SC 119.2.6.2.2 P 167 L 25 # r02-5
 Koehler, Daniel

Comment Type E Comment Status X

Assertion and Deassertion of hi_ser is defined as depending on 8192 codewords. However
 according to 119.2.5.3 once asserted it should stay asserted for 60ms to 75ms which is not
 reflected in this variable definition.

SuggestedRemedy

Change wording similar to ...this bit is set to one if ... exceeds the threshold ... and once
 asserted is set to zero after 60ms to 75ms and no longer exceeding the threshold.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 119 SC 119.2.6.3 P 172 L 2 # r02-6
Koehler, Daniel

Comment Type T Comment Status X

Adding hi_ser in the Fig. 119-13 seems unintended. It forces the LOSS_OF_ALIGNMENT state (LOA) which creates ambiguities for the RSFEC decode process up to the possibility of a dead-lock the link would never recover from. Reasons of doubt: a) When in LOA state restart_lock is forced false. If now during hi_ber the link is reset by the link partner the statemachine of Fig. 119-12 will enter the 5_BAD state eventually as markers are most likely no longer at expected position. Now we have an ambiguity what state the restart_lock variable should become. Fig. 119-13 enforces false, where now Fig. 119-12 enforces true. Which one wins ? (neither is a solution) b) But the main problem is now Fig. 119-13 which does not allow deskew as LOA state enforces pcs_enable_deskew=false. Hence the deskew process cannot align the lanes in such situation causing the RSFEC decoder receiving data from unaligned lanes causing permanent uncorrectable codewords which by definition in 119.2.5.3 create 16 symbol errors per codeword. This is now a dead-lock, as the hi_ser will never deassert as the threshold will be permanently exceeded hence the link will never come up again. It may be argued that the RSFEC decode process is not active when align_status is down but then also hi_ser measurement stops which then means definition of hi_ser deassertion is incorrect in 119.2.6.2. and e.g. needs to be defined purely based on time deasserting after 60..75ms.

SuggestedRemedy

I think the intention was to enforce CDMII local fault signaling and link status down when hi_ser occurs similar to the reaction to hi_ber done for 100G (Clause 82) while maintaining all RSFEC decode process to continue operating normally while hi_ser is asserted to keep monitoring. Proposed Remedy: remove the the or hi_ser from Fig. 119-13. Instead add it to Fig. 119-15 (Receive state diagram) to enforce RX_INIT state producing local fault to CDMII. In addition change definition of PCS_Status in 119.2.6.2.2 to: A boolean variable that is true when align_status is true and hi_ser is false and is false otherwise.

Proposed Response Response Status O

CI 116 SC 116.5 P 119 L 33 # r02-7
Slavick, Jeff Broadcom Limited

Comment Type TR Comment Status X

Table 116-8 lists N/A for SP2 and SP5 which are the PMD interface skew points. For 400G-DR4 that is a 53Gbd interface.

SuggestedRemedy

In Table 116-8 53Gbd column, change the SP2 N/A to 21 and the SP5 N/A to 191

Proposed Response Response Status O

CI 120 SC 120.5.7 P 196 L 15 # r02-8
Slavick, Jeff Broadcom Limited

Comment Type T Comment Status X

This section is defining how Gray mapping is done in the transmit and receive directions. The first two paragraphs are related to the transmission and the last to the reception. However, only the last paragraph qualifies the direction of data flow.

SuggestedRemedy

Combine the first two paragraphs to read as follows:
For output lanes encoded as PAM4 (for 200GBASE-R, where the number of output lanes is 4, or for 400GBASE-R, where the number of output lanes is 4 or 8), the PMA transmit process shall map consecutive pairs of bits {A, B}, where A is the bit arriving first, to a Gray-coded symbol as follows:

Proposed Response Response Status O

CI 116 SC 116.3.3 P 111 L 42 # r02-9
Slavick, Jeff Broadcom Limited

Comment Type T Comment Status X

The inter-sublayer service interface is applicable to both 200G and 400G

SuggestedRemedy

Delete "for the 400GBASE-R sublayers"

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120D SC 120D.3.2.1 P 360 L 27 # r02-10
Hidaka, Yasuo Fujitsu Laboratories of

Comment Type TR Comment Status X

For Rx ITT of 100GBASE-KR4 in 93.8.2.3, the return loss of the test setup in Figure 93C-4 measured at TP5 replica was specified to meet the requirements of Equation (93-2), but it is missing for 120D. As explained in hidaka_3cd_01a_0517.pdf and hidaka_060717_3cd_adhoc-v2.pdf, missing return loss allows use of a bad test channel for Rx ITT, which will cause interoperability problems between compliant channel and compliant Rx. As explained in hidaka_3cd_02_adhoc-v2.pdf, the return loss of the test channel for Rx ITT is important, because it may improve margin for interoperability. Since we had defined return loss of test channel for Rx ITT of Clause 93 as well as 83D, we should do the same for Annex 120D.

SuggestedRemedy

Add the following to the list of additional considerations:

i) The return loss of the test setup in Figure 93C-4 measured at TP5 replica meets the requirements of Equation (93-2).

Add a new row of "Return loss of test setup at TP5 replica" to Table 120D-6 with a value of "Equation (93-2)" in "Min" columns.

Proposed Response Response Status O

CI 120D SC 120D.3.2.1 P 360 L 38 # r02-11
Hidaka, Yasuo Fujitsu Laboratories of

Comment Type TR Comment Status X

The COM value for Rx ITT should be the max value, not the target value. For instance, even if the requirement for Rx ITT compliance is 3dB, a SerDes vendor may use 2dB to have an extra margin for some reason such as a customer request. If a device passes Rx ITT with a 2dB test channel, it is not required to test it again with a 3dB test channel to claim the compliance. However, if it is defined as the target value, it must be tested again with a 3dB test channel to claim the compliance. A numerical error in the computation of calibration is a minor issue. Although it was defined as the target value in Table 83D-5, it was wrong unfortunately. It was defined as the max value in Table 92-8, Table 93-6, Table 94-15, Table 110-6, Table 110-7, Table 110-8, Table 111-4, Table 111-5, and Table 111-6.

SuggestedRemedy

Specify "COM including effects of broadband noise" as the max value.
Remove the "Target" columns from Table 120D-6.

Proposed Response Response Status O

CI 120B SC 120B.3.2 P 337 L 23 # r02-12
Hidaka, Yasuo Fujitsu Laboratories of

Comment Type T Comment Status X

The COM value for Rx ITT should be the max value, not the target value. For instance, even if the requirement for Rx ITT compliance is 3dB, a SerDes vendor may use 2dB to have an extra margin for some reason such as a customer request. If a device passes Rx ITT with a 2dB test channel, it is not required to test it again with a 3dB test channel to claim the compliance. However, if it is defined as the target value, it must be tested again with a 3dB test channel to claim the compliance. A numerical error in the computation of calibration is a minor issue. Although it was defined as the target value in Table 83D-5, it was wrong unfortunately. It was defined as the max value in Table 92-8, Table 93-6, Table 94-15, Table 110-6, Table 110-7, Table 110-8, Table 111-4, Table 111-5, and Table 111-6.

SuggestedRemedy

Change the third item in the list of exceptions from:

The target values for the parameter "COM including effects of broadband noise" in Table 83D-5 are 3dB.

to:

The parameter "COM including effects of broadband noise" in Table 83D-5 has the max values of 3dB. There is no target values for the parameter "COM including effects of broadband noise".

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120B SC 120B.3.2 P 337 L 34 # r02-13
Hidaka, Yasuo Fujitsu Laboratories of

Comment Type T Comment Status X

Specifying "Applied pk-pk sinusoidal jitter" as the target value is wrong. For instance, a SerDes vendor may have additional sinusoidal jitter to have an extra margin for some reason. If a device passes Rx ITT with this additional sinusoidal jitter, it is not required to test it again with the sinusoidal jitter in this standard spec. Although it was defined as the target in Table 83D-5, it was wrong unfortunately.

SuggestedRemedy

Change the seventh item in the list of exceptions from:

The "Applied pk-pk sinusoidal jitter" for Test 1 and Test 2 in Table 83D-5 is according to Table 87-13.

to:

The "Applied pk-pk sinusoidal jitter" for Test 1 and Test 2 in Table 83D-5 has max the max values according to Table 87-13. There is no target values for the parameter "Applied pk-pk sinusoidal jitter".

Proposed Response Response Status O

CI 120D SC 120D.4 P 363 L 8 # r02-14
Hidaka, Yasuo Fujitsu Laboratories of

Comment Type TR Comment Status X

As explained in hidaka_061417_3cd_01_adhoc.pdf, the limit of variation of compliant channels will grow, if we use a single reference value for the COM impedance parameters, and the single reference value is different from the nominal value. In order to minimize the variation of compliant channels, we should use the nominal value as the single reference value, or we should use multiple reference values. Reduction of variation helps to improve margin for interoperability, which is not guaranteed in the current specification. When we change the COM impedance parameters, we should also consistently change A_v, A_fe, A_ne to get the same signal amplitude at TP0a from reference Tx in COM, and we should also change the COM value to avoid changing the pass / fail status of existing channels. The consistent changes required to A_v, A_fe, and A_ne were reported in hidaka_060717_3cd_adhoc-v2.pdf slide 9. The consistent change required to COM value was reported in hidaka_061417_3cd_01_adhoc.pdf slide 3-8.

SuggestedRemedy

Change the following COM parameter values in Table 120D-8:

Z_c from 90 ohm to 95 ohm
R_d from 55 ohm to 50 ohm
A_v from 0.44 V to 0.418 V
A_fe from 0.44 V to 0.418 V
A_ne from 0.63 V to 0.604 V

For clarification of the intention of the value, in the parameter column of Table 120D-8, change

"Transmission line characteristic impedance"

to
"Transmission line nominal characteristic impedance".

In the first paragraph of 120D.4, P362, L9, change from:

"shall be greater than or equal to 3 dB"

to

"shall be greater than or equal to 3.1 dB".

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

Cl 1 SC 1.4 P34 L 3 # r02-15
Grow, Robert RMG Consulting

Comment Type E Comment Status X

Insert locations do not follow 802.3 sort order. Though this could be fixed during the next revision, getting these definitions closer to the correct sort order location will help not overlook this during the revision. Our publication editors have recently stated that subclause numbering is not substantive, so if no additional recirculations are required this comment can be passed to the editors for consideration during publication preparation.

SuggestedRemedy

1.4.72b through 1.4.72i belong after 1.4.64aa 2.5GBASE-T inserted by IEEE Std 802.3bz.
1.4.72j through 1.4.72r belong after

Proposed Response Response Status O

Cl 78 SC 78.1.4 P103 L 16 # r02-16
Grow, Robert RMG Consulting

Comment Type E Comment Status X

Misleading editing instruction table has been modified by most amendments to 802.3-2015, and the inserted rows in IEEE Std 801.2bv are not at the bottom of the table (have no relevance to the specified insert point).

SuggestedRemedy

Delete the parenthetical "(as modified by IEEE Std 802.3by-2016)" from the instruction.

Proposed Response Response Status O

Cl 78 SC 78.2 P103 L 38 # r02-17
Grow, Robert RMG Consulting

Comment Type TR Comment Status X

There are no specifications for EEE timing prameters Tx, Tq, and Tr.

SuggestedRemedy

Add rows to Table 78-2 for the various port types and interfaces of P802.3bs.

Proposed Response Response Status O

Cl 124 SC 124.8.9 P302 L 42 # r02-18
Wertheim, Oded Mellanox Technologie

Comment Type T Comment Status X

The jitter specification for the 100G per lane 400GBASE-DR4 receiver uses the same frequency corner as the 50G per lane 400GAUI-8 but with half the peak-to-peak jitter as the jitter mask is defined in UIs.
This requires the 400GBASE-DR4 transceiver PMA to implements a de-jitterizer, which requires to add PLL to handle the low frequency jitter and a large jitter buffer which adds unnecessary complexity, cost and power to the transceiver. Moreover, since the low frequency jitter isn't bounded in host transmitter, in theory an unlimited jitter buffer is required in order to handle the low frequency jitter.

SuggestedRemedy

Double the peak to peak jitter value for the 400GBASE-DR4 receiver:
Add an exception to 124.8.9 Stressed receiver sensitivity:
... with the following exceptions:
- The sinusoidal jitter is used to test receiver jitter tolerance:
o $f < 40\text{KHz}$, Not specified
o $40\text{ kHz} < f < 4\text{ MHz}$, $4 * 10^5 / f$
o $4\text{ MHz} < f < 10\text{ LB}$, 0.1

Consequently change the 400GBASE-DR4 TDECQ .

Proposed Response Response Status O

Cl 120E SC 120E.3.3.2.1 P379 L 28 # r02-19
Le Cheminant, Greg

Comment Type T Comment Status X

Test equipment cannot achieve the required transition time for the aggressor patterns when measured through the compliance boards with the specified oscilloscope 33 GHz 4th order BT response. This does not represent realistic approximation of the transmitter transition time when measured through the same channel and oscilloscope without equalization. (A presentation will be submitted to the ad hoc call covering this)

SuggestedRemedy

Increase the aggressor transition time that a value that better approximates a real transmitter measured through the same channel and oscilloscope response.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120E SC 120E.3.4.1.1 P 381 L 53 # r02-20
Le Cheminant, Greg

Comment Type T Comment Status X

Test equipment cannot achieve the required transition time for the aggressor patterns when measured through the compliance boards with the specified oscilloscope 33 GHz 4th order BT response. This does not represent realistic approximation of the transmitter transition time when measured through the same channel and oscilloscope without equalization. (A presentation will be submitted to the ad hoc call covering this)

SuggestedRemedy

Increase the aggressor transition time that a value that better approximates a real transmitter measured through the same channel and oscilloscope response.

Proposed Response Response Status O

CI 120E SC 120E.3.3.2 P 378 L 41 # r02-21
Le Cheminant, Greg

Comment Type T Comment Status X

Test equipment (BERT pattern generators) cannot achieve the specified EW(1E-5) through the specified compliance board channel when measured with the specified reference receiver. The resulting eye is somewhat narrower, which will overstress the DUT

SuggestedRemedy

Relax the specification for the EW in the both the Host and Module input tests to a value which can be obtained in the specified test setup (A presentation on this will be offered on the ad hoc call)

Proposed Response Response Status O

CI 120E SC 120E.3.4.1 P 380 L 44 # r02-22
Le Cheminant, Greg

Comment Type T Comment Status X

Test equipment cannot achieve the required transition time for the aggressor patterns when measured through the compliance boards with the specified oscilloscope 33 GHz 4th order BT response. This does not represent realistic approximation of the transmitter transition time when measured through the same channel and oscilloscope without equalization. (A presentation will be submitted to the ad hoc call covering this)

SuggestedRemedy

Relax the specification for the EW in the both the Host and Module input tests to a value which can be obtained in the specified test setup (A presentation on this will be offered on the ad hoc call)

Proposed Response Response Status O

CI 120E SC 120E.3.2.2 P 376 L 49 # r02-23
Healey, Adam Broadcom Ltd.

Comment Type T Comment Status X

The "Far-end pre-cursor ratio" is the ratio p_{pre}/p_{max} where p_{pre} is a residual inter-symbol interference (ISI) term. There is also pre-cursor equalization that may be employed by the transmitter to reduce the measured "far-end pre-cursor ratio". There has been some confusion as to whether this specification refers to the transmitter equalization or the residual ISI. This is clear from the text of 120E.3.2.2 but it may be better to refer to the parameter defined in this subclause as the "far-end pre-cursor ISI ratio".

SuggestedRemedy

Change "far-end pre-cursor ratio" to "far-end pre-cursor ISI ratio" here (2 instances), in Table 120E-3 (1 instance), and in 120E.3.3.2.1 (1 instance, page 379, line 44). On page 377, line 26, change "The pre-cursor p_{pre} ..." to the "Theu pre-cursor ISI p_{pre} ..."

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 45 SC 45.2.3.47k.3 P 75 L 45 # r02-24
Slavick, Jeff Broadcom Limited

Comment Type TR Comment Status X

The definition of this bit in Clause 45 is at odds with the definition in Clause 119.

SuggestedRemedy

Change 45.2.3.47k.3 to read:

When read as a one, bit 3.801.4 indicates that the local PCS has detected a degradation of the received signal. This bit reflects the state of FEC_degraded_SER (see 119.2.5.3).

Proposed Response Response Status O

CI 120D SC 120D.3.2 P 360 L 39 # r02-25
Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

There is need to limit the variability of the test 1 and test 2 channel. Return loss was suggested as a method to control variability. Additional precision can be improved by measuring the effective pulse reflection from a unit interval pulse.

SuggestedRemedy

Add a row to table 120D-6 which specifies the maximum effective return loss from a UI pulse. Specify this maximum effective return loss at -18 dB. Refer to an added new annex on how to compute the effective pulse return per presentation (name TBD)

Proposed Response Response Status O

CI 120D SC 120D.3.1.1 P 353 L 14 # r02-26
Mellitz, Richard Samtec, Inc.

Comment Type TR Comment Status X

Package differences between COM computations and those which pass device electrical parameters may increase the risk of interoperability. An additional return loss metric more tightly tied to signaling will help reduce this risk.

SuggestedRemedy

Insert a row in table 120D-1 snff 120D-5 for maximum effective return loss. Specify this maximum effective return loss at -7.5 dB.

Specify a new Annex on how to compute the effective pulse return loss per presentation (name TBD)

Proposed Response Response Status O

CI 120 SC 120.5.7 P 196 L 13 # r02-27
Dawe, Piers J G Mellanox Technologie

Comment Type T Comment Status X

According to <http://www.atis.org/glossary/definition.aspx?id=5055> and Wikipedia, a Gray code is a binary numeral system and/or cyclic. PAM4 isn't. This subclause defines Gray coding with PAM4 coding.

SuggestedRemedy

Change heading from "Gray coding for PAM4 encoded lanes" to "Gray and PAM4 coding". For consistency with the next paragraph, change "Gray-coded symbol" to "Gray-coded PAM4 symbol". Change "four Gray-coded levels" to "four PAM4 levels". In 120.5.11.2.1, 120.5.11.2.2 and 120.5.11.2.3, change "Gray coding" to "Gray and PAM4 coding" (6 changes in all).

Proposed Response Response Status O

CI 121 SC 121.7.1 P 221 L 25 # r02-28
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

PAM4 optics is still new and raw, we are still debugging the specification methodology, and we have seen far too little experimental information showing technical and economic feasibility. It looks like this PMD can be made to work but as measurements with the new TDECQ method and with new receiver designs become available, we expect the optical power levels can be reduced and the spec as in this draft will be uneconomic.

SuggestedRemedy

Bring more evidence for what optical power levels and TDECQ limits are right; in particular, TDECQ measurements with SSPRQ, and correlation to actual receiver performance. Based on evidence, reduce all the optical power levels for 200GBASE-DR4 by 0.5, 1 or 1.5 dB (with other adjustments for other reasons). Review the TDECQ limit.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

Cl 121 **SC 121.7.1** **P 221** **L 32** # **r02-29**
Dawe, Piers J G Mellanox Technologie

Comment Type **T** **Comment Status** **X**

After the change in reference receiver bandwidth, we need to either increase the TDECQ limits and make consequent changes including to budget and unstressed sensitivity; and/or change the definition (zero basis) of TDECQ.

SuggestedRemedy
Changing the zero point of TDECQ seems easy to do in the short term and less confusing in the long term. See another comment.

Proposed Response **Response Status** **O**

Cl 122 **SC 122.7.1** **P 221** **L 36** # **r02-30**
Dawe, Piers J G Mellanox Technologie

Comment Type **E** **Comment Status** **X**

Table 121-6 and 124-6 say Extinction ratio, each lane (min) while tables 122-9 and 122-10 say Extinction ratio (min)

SuggestedRemedy
Can they be made consistent?

Proposed Response **Response Status** **O**

Cl 121 **SC 121.8.5.1** **P 226** **L 49** # **r02-31**
Dawe, Piers J G Mellanox Technologie

Comment Type **TR** **Comment Status** **X**

Using the same pattern on the aggressor lanes (correlated crosstalk) is very unusual. Does what we gain in correctly handling the spectrum of the deterministic part of the crosstalk outweigh what we lose in inconsistency vs. UI- and sub-UI phasing? As D3.1 comment 13 points out, using the conventional uncorrelated crosstalk can simplify the PMA. It should be possible to calculate the relative measurement accuracy of the two approaches.

SuggestedRemedy
Work out which is better; change the crosstalk patterns here and the related pattern generator options in Clause 120 as appropriate.

Proposed Response **Response Status** **O**

Cl 121 **SC 121.8.5.3** **P 228** **L 9** # **r02-32**
Dawe, Piers J G Mellanox Technologie

Comment Type **T** **Comment Status** **X**

"the oscilloscope is set up to capture samples from all symbols in the complete pattern without averaging": this implies 65,535, maybe times a few: is that really enough? Actual measurements seem to have around a million samples or more. We don't need to give right guidance but we should not give bad guidance or hint at bad practice.

SuggestedRemedy
We should either give good advice, or just say that the number of samples should be large enough that it does not materially affect the result.

Proposed Response **Response Status** **O**

Cl 121 **SC 121.8.5.3** **P 229** **L 11** # **r02-33**
Dawe, Piers J G Mellanox Technologie

Comment Type **TR** **Comment Status** **X**

The bandwidth for the noise enhancement calculation is still 19.34 GHz while that for the signal is now 13.28125 GHz. This difference over-estimates the equalizable part of the penalty but not the unequalizable part, which seems bad.

SuggestedRemedy
Change 19.34 GHz to 13.28125 GHz.

Proposed Response **Response Status** **O**

Cl 121 **SC 121.8.5.3** **P 229** **L 34** # **r02-34**
Dawe, Piers J G Mellanox Technologie

Comment Type **TR** **Comment Status** **X**

The change of the reference bandwidth from 19.34 GHz to 13.28125 means that an ideal signal (fast, no noise or jitter, no emphasis) has a TDECQ that is far from zero. We could live with this and change many other numbers including "results in at least half of the dB value of the stressed eye closure (SECQ)" but doing so makes the budget hard to understand. In the remedy I assume the offset is 0.5 dB; this should be checked.

SuggestedRemedy
In Eq. 121-12, change 1 to 0.891, which is 0.5 dB less. Add a NOTE to explain that this number represents the TDECQ of an ideal signal (fast edges, no noise or jitter, no emphasis).
Or, change 1 to a new parameter, value 0.891, add to the "where" list.
Or, modify equation to TDECQ = 10 log10(...) - TDECQ0 where TDECQ0 is 0.5 ...

Proposed Response **Response Status** **O**

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 121 SC 121.8.5.3 P 229 L 42 # r02-35
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Updating D3.0 comment 140:

It seems that it is possible to make a bad transmitter (e.g. with a noisy or distorted signal), use emphasis to get it to pass the TDECQ test, yet leave a realistic, compliant receiver with an unreasonable challenge (up to 2.5/2 dB worse than the SRS test?) With some of the changed low-bandwidth TDECQ being used to equalize the reference receiver's own bandwidth, this issue becomes more apparent.

SuggestedRemedy

Define TDECQrms = $10 \cdot \log_{10}(A_{\text{RMS}}/(s \cdot 3 \cdot Q_t \cdot R))$ where A_RMS is the standard deviation of the measured signal after the 13.28125 GHz filter response. s is close to the standard deviation of a fast clean signal with OMA=0.5 and without emphasis, observed through the 13.28125 GHz filter response, according to what level of dirty-but-emphasised signal we decide is acceptable. Require that TDECQrms shall not exceed the limit for TDECQ.

Proposed Response Response Status O

CI 122 SC 122.7.1 P 252 L 14 # r02-36
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

PAM4 optics is still new and raw, we are still debugging the specification methodology, and we have seen far too little experimental information showing technical and economic feasibility. As measurements with the new TDECQ method and with new receiver designs become available, it may be that optical power levels can be reduced and the spec as in this draft would be uneconomic.

SuggestedRemedy

Bring more evidence for what optical power levels and TDECQ limits are right; in particular, TDECQ measurements with SSPRQ, and correlation to actual receiver performance. Based on evidence, consider reducing all the optical power levels in this clause except the -30 dBm signal detect limit by 0.5 or 1 dB (with other adjustments for other reasons). Review the TDECQ limits.

Proposed Response Response Status O

CI 124 SC 124.7.1 P 298 L 4 # r02-37
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

PAM4 optics is still new and raw, we are still debugging the specification methodology, and we have seen too little experimental information showing technical and economic feasibility. As measurements with the new TDECQ method and with new receiver designs become available, it may be that optical power levels can be reduced and the spec as in this draft would be uneconomic.

SuggestedRemedy

Bring more evidence for what optical power levels and TDECQ limits are right; in particular, TDECQ measurements with SSPRQ, and correlation to actual receiver performance. Based on evidence, reduce all the optical power levels for 400GBASE-DR4 by 0.5 or 1 dB (with other adjustments for other reasons). Review the TDECQ limit.

Proposed Response Response Status O

CI 124 SC 124.8.5 P 302 L 4 # r02-38
Dawe, Piers J G Mellanox Technologie

Comment Type E Comment Status X

Most of these definitions identify the pattern to use by reference to Table 124-10. 124.8.5 (TDECQ) and 124.8.9 (SRS) don't, leaving the associated rows in the table without effect.

SuggestedRemedy

For consistency, should 124.8.5 and 124.8.9 identify the pattern too?

Proposed Response Response Status O

CI 121 SC 121.8.7 P 302 L 20 # r02-39
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

With the lower receiver bandwidth, measuring RIN in approximately the signaling rate (twice as much) seems too much; 1/2 to 3/4 would be better. A T-spaced equalizer cannot independently adjust for good ISI and RIN filtering, so can an adequate estimate of RIN can be obtained as a by-product of the TDECQ procedure? While a T/2-spaced equalizer could enhance the RIN, it would not choose to do so if RIN were a problem.

SuggestedRemedy

Review; simplify RIN measurement to a Qsq measurement (see 68.6.7) or eliminate as appropriate. Remove 120.5.11.2.4 Square wave (quaternary) test pattern, and associated registers.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 124 SC 124.8.9 P 302 L 46 # r02-40
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Following up on D3.0 comment 153 and D3.1 comment 55: if the jitter corner frequency for 26.5625 GBd (NRZ and PAM4) is 4 MHz, the low frequency ends of the jitter masks must align or be in the right order if expressed in time vs. frequency, i.e. should scale with signalling rate if in UI. If this is not done, the required depth of the LF jitter buffer in the 2:1 muxes in a 400GBASE-DR4 module is unbounded and the low frequency jitter generation requirements on the module become unreasonable. Compare 87.8.11.4 and 88.8.10: 4 MHz for 10.3125 GBd, 10 MHz for 25.78125 GBd. History: anslow_3bs_04_0316 does not contain reasoning, refers to ghiasi_3bs_01_0316 which does not address wander and buffering. ghiasi_3bs_01a_0116.pdf#page=15 shows FIFOs but does not establish a workable spec. Slide 14 shows they can be avoided: this is what we have for 400GAUI-8 or 400GAUI-16 with 400GBASE-xR8. I have no evidence that the problems described in the second sentence have been considered or solved by the committee.

SuggestedRemedy

Add another exception for the SRS procedure, with a table like Table 121-12 replacing second row after the header row:

80 kHz < f <= 250 kHz 4e5/f

250 kHz < f <= 500 kHz 1e11/f^2

1 MHz < f <= 4 MHz 2e5/f

Or, with the UIs doubled vs. Table 121-12:

f < 40 kHz Not specified

40 kHz < f <= 4 MHz 4e5/f

4 MHz < f <= 10 LB 0.1

Increase the TDECQ limit to share the burden appropriately between transmitter and receiver.

This option means the 100G/lane receiver has to tolerate no more timing slew rate (in ps/us) than that agreed for 50G/lanes.

Or, increase jitter by 50% and corner frequency by 33%:

f < 40 kHz Not specified

40 kHz < f <= 6 MHz 4e5/f

5.333 MHz < f <= 10 LB 0.075

and add an exception in 124.8.5 that the CRU corner frequency is 5.333 MHz. Increase the TDECQ limit to share the burden between transmitter and receiver.

To do the job properly with the first option, in 124.8.5 we should add another exception to the CRU with a corner frequency of 4 MHz and a slope of 20 dB/decade (in 121.8.5.1): add a pole at 250 kHz and a zero at 500 kHz. I am advised that this can be done in hardware (in software, anything is possible).

Proposed Response Response Status O

CI 120D SC 120D.2 P 352 L 31 # r02-41
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Now that the return loss spec has been tightened (Eq 120D-2), the allowed return loss of the test fixture (in 93.8.1.1) is too close to the limit and ruins the measurement. Per 93.8.1.1, "The effects of differences between the insertion loss of an actual test fixture and the reference insertion loss are to be accounted for in the measurements"

SuggestedRemedy

Tell the user to de-embed the test fixture return loss, or tighten the TF RL spec?

Making the IC implementer responsible for the test fixture seems appropriate, as the test fixture is custom designed for that IC and the IC is soldered onto it.

Proposed Response Response Status O

CI 120D SC 120D.3.1.1 P 353 L 24 # r02-42
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Signal-to-noise-and-distortion ratio (min) 31.5 dB is too high (increased by D3.1 comment 22, so even worse than before) - probably can't measure the IC through the test fixture and cables. I suspect there is double counting of jitter in SNDR and as jitter, in COM.

SuggestedRemedy

Remove the double counting. Reduce the SNDR limit to something that can reasonably be measured, or change the measurement method.

Proposed Response Response Status O

CI 120D SC 120D.3.1.1 P 353 L 26 # r02-43
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Following D3.1 comments 22 and 36: transmitter Output residual ISI SNR_ISI (min) 34.8 dB is still too high - probably can't measure the IC through the test fixture and cables, even test equipment fails this limit. The warning NOTE in 120D.3.1.7 shows the issue, but doesn't solve it.

SuggestedRemedy

It may be necessary to move away from the SNR_ISI method.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120D SC 120D.3.1.1 P 354 L 36 # r02-44
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Following D3.1 comment 41: the low frequency RL at 14.25 dB is insignificant for signal integrity compared with the 8.7 dB at 6 GHz. This RL is much tighter than CEI-56G-MR at low (and high) frequency (although apparently looser between 4 and 9 GHz).

SuggestedRemedy

Change 14.25 - f to 12 -0.625f

Proposed Response Response Status O

CI 120D SC 120D.4 P 363 L 28 # r02-45
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Because COM accounts for channel return loss only erratically (depends on frequency and high Z / low Z), C2C needs a channel RL spec. (Clause 137, 200GBASE-KR4, has a normative channel RL spec already, 100GBASE-KR4 and C2C XLAUI/CAUI-10 have recommendations.)

SuggestedRemedy

Add a channel return loss spec, e.g. copy the one from Clause 137. This should be normative for channels with COM less than 4, recommended for other channels.

Proposed Response Response Status O

CI 120E SC 120E.3.1 P 371 L 20 # r02-46
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

Building on D3.0 comment 119: The host is allowed to output a signal with 900 mV peak-to-peak amplitude but only 32 mV eye height - a very bad signal. If the module is exactly like the reference receiver, that would work, but with a good but slightly different receiver the eye will collapse.

SuggestedRemedy

We need some other spec to protect the module from such unexpected signals. A vertical eye closure spec will probably work. I'll try to bring a presentaitaion.

Proposed Response Response Status O

CI 120E SC 120E.3.2 P 376 L 7 # r02-47
Dawe, Piers J G Mellanox Technologie

Comment Type TR Comment Status X

It turns out that meeting the five module output specs simultaneously with good tolerances is not feasible (near and far end eye height and width, far-end pre-cursor ratio). And, according to my understanding of healey_3bs_01a_0317, a far-end pre-cursor ratio of 1%, 2% or 9% provides a healthy COM for a C2C receiver but a C2M receiver after a COM package with a now obsolete Cd has a problem with 9%, so the 2.5% limit in the draft seems arbitrary.

This is a follow-up to D3.1 comment 42.

SuggestedRemedy

Decrease the limit for far-end eye height from 70 mV to 45 mV.

Widen the pre-cursor ratio limit from +/-2.5% to +/-3.5%.

Consider increasing the loss in the software channel (moving the "far end" to after a reasonable package loss), and making a small adjustment to the far-end eye height and width to compensate.

If the loss is not increased, consider if an asymmetrical pre-cursor ratio limit would be more effective.

Review the way this works for a reasonable variety of channels.

Review what range of CTLE peaking is consistent with the insertion loss budget.

Proposed Response Response Status O

CI 120E SC 120E.4.1 P 383 L 3 # r02-48
Dawe, Piers J G Mellanox Technologie

Comment Type T Comment Status X

This refers to 92.11.3 where 92.11.3.1 has a FOM_ILD spec of 0.13 dB for the mated compliance boards. OIF CEI-56G-VSR-PAM4 has a limit of 0.1 dB. As PAM4 is so sensitive to reflections (ILD), it would be advisable to follow OIF CEI-56G-VSR-PAM4 if that is feasible. This comment is a revision of D3.1 comment 44 (no consensus then).

SuggestedRemedy

If feasible, add FOM_ILD spec, limit 0.1 dB.

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120E SC 120E.5.4.2 P 388 L 20 # r02-49
Dawe, Piers J G Mellanox Technologie
Comment Type E Comment Status X
The PICS entries should be in the order the requirements appear, which is the order in Table 120E-3, then others.
SuggestedRemedy
Order the PICS entries as in Table 120E-3, then the items which aren't in the table.
Proposed Response Response Status O

CI 120E SC 120E.5.4.2 P 388 L 24 # r02-50
Dawe, Piers J G Mellanox Technologie
Comment Type E Comment Status X
Missing PICS item
SuggestedRemedy
Add PICS item for far-end pre-cursor ratio
Proposed Response Response Status O

CI 122 SC 122.8.4 P 258 L 6 # r02-51
Dudek, Michael Cavium
Comment Type E Comment Status X
This is a very long "run on" sentence.
SuggestedRemedy
Break the sentence into three. "The OMAouter is measured using a test pattern specified for OMAouter in Table 122-15. It is the difference between the average optical launch power level P3, measured over the central 2 UI of a run of 7 threes, and the average optical launch power level P0, measured over the central 2 UI of a run of 6 zeros, as shown in Figure 122-3. For the test the sum of the optical power from all of the lanes not under test is below -30 dBm, or if other lanes are operating, a suitable optical filter may be used to separate the lane under test.
Proposed Response Response Status O

CI 120E SC 120E.3.4.1.1 P 382 L 28 # r02-52
Dudek, Michael Cavium
Comment Type T Comment Status X
Wrong reference. The error counters aren't described in 119.2.5.3.
SuggestedRemedy
Change the reference to 119.3.1 (as was done in section 120E.3.3.2..1 in draft 3.1)
Proposed Response Response Status O

CI 120D SC 120D.3.2.1 P 360 L 26 # r02-53
Dudek, Michael Cavium
Comment Type T Comment Status X
It would be advantageous to allow the use of the PRBS31Q pattern for the interference tolerance test just as it is allowed for the jitter tolerance test.
SuggestedRemedy
Add an additional bullet (new bullet h) and renumber h)) (modified version of the jitter tolerance bullet.) "As an alternative to using the scrambled idle test pattern and measuring FEC symbol error ratio it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10. Note that this requirement can be somewhat more stringent than using the scrambled idle test pattern and measuring FEC symbol error ratio, and therefore failing this test requirement with the PRBS31Q pattern does not necessarily imply a failure of the interference tolerance test.
Proposed Response Response Status O

CI 120E SC 120E.3.3.2.1 P 379 L 53 # r02-54
Dudek, Michael Cavium
Comment Type T Comment Status X
Wrong reference. We shouldn't be referring to the PRBS31 test pattern section when using the PRBS31Q pattern..
SuggestedRemedy
Change the reference from 120.5.11.1.1 to 120.5.11.2.2. Also on page 382 line 23
Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120D SC 120D.4 P 362 L 28 # r02-55
Dudek, Michael Cavium

Comment Type TR Comment Status X

Using a single set of supposed worst case values for the die impedance and package impedance has been shown to not result in worst case COM for various channels. (See e.g. Hidaka_3cd_01a_0317, Dudek_3bs_02_0517). Using these supposed worst case values tends to favor certain channels while penalizing other channels. Using nominal values for Rd and Zc reduces the amount of "favoring" and "penalizing" and therefore the nominal values should be used unless multiple sets of different values are used.

SuggestedRemedy

In table 120D-8 Change Zc to 95 Ohm, Zd to 50 Ohm and change Av to 0.416. (See dudek_3bs_01a_0517 for the change to Av).

Proposed Response Response Status O

CI 120D SC 120D.4 P 362 L 9 # r02-56
Dudek, Michael Cavium

Comment Type TR Comment Status X

Variations in package impedance and die impedance while still meeting the Tx and Rx specifications (including return loss) cause worse COM for some channels than is obtained with the values used in the COM test for the channel resulting in a "hole" in the budget. (See e.g. Hidaka_3cd_01a_0317, Dudek_3bs_02_0517). This hole is around 0.5dB.

SuggestedRemedy

Change the required value of COM for the channel from 3.0dB to 3.5dB while leaving the calibration of the interference tolerance test at 3.0dB COM. As an alternative the burden to close the budget could be shifted from the channel to the Rx by using 3.0dB as the channel COM and 2.5dB COM for the interference tolerance test calibration or could be shared as long as there is 0.5dB difference between them.. Change PICS CC1 to this revised value.

Proposed Response Response Status O

CI 120D SC 120D.3.2.1 P 360 L 17 # r02-57
Dudek, Michael Cavium

Comment Type TR Comment Status X

Variations in the test equipment output impedance will interact with the Rx input impedance of the DUT to create non-reproducibility in the Interference tolerance test. This should be reduced (as was done for Clause 93) by imposing a return loss specification on the test equipment.

SuggestedRemedy

Apply the same return loss specification for the test equipment as was used in Clause 93. Add an extra bullet to the list. "The return loss of the test setup in Figure 93C-4 measured at TP5 replica meets the requirements of Equation (93-2)."

Proposed Response Response Status O

CI 120D SC 120D.3.1.1 P 353 L 36 # r02-58
Dudek, Michael Cavium

Comment Type TR Comment Status X

The return loss specification is too tight at high frequencies for the package used in COM with the allowance for the test fixture return loss. (particularly for the short package) A presentation will be made either in an ad hoc or at the Berlin meeting (or both)

SuggestedRemedy

Change the second half of equation 120D-2 to "10.65 -0.4f

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI 120D SC 120D.3.1.7 P 357 L 38 # r02-59
Dudek, Michael Cavium

Comment Type E Comment Status X

There are a lot of "where" parameters which are split into two paragraphs which don't read well.

SuggestedRemedy

Combine the paragraphs and create a list of the where's. It would look like.
ISlscursors are computed from the linear fit pulse response, $p(k)$ in accordance with 120D.3.1.3, using Equation (120D-8), where:
 t_p is the index of the linear fit pulse where $p(t_p)$ equals p_{max} .
 M is the oversampling ratio of the measured waveform and linear fit pulse as defined in 85.8.3.3.4
 N_p is the linear fit pulse length given in 120D.3.1.3.
 N_b is given in Table 120D-8.

Proposed Response Response Status O

CI 120D SC 120D.3.2 P 359 L 33 # r02-60
Dudek, Michael Cavium

Comment Type TR Comment Status X

The Differential input return loss for the receiver should have stayed the same as the differential return loss of the transmitter to reduce the variability between the system performance of a channel measured by COM with a single package and die impedance and the result with a real receiver which is measured with a test system with a different (better) return loss.

SuggestedRemedy

Change the Differential input return loss (min) in table 120D-5 to use equation 120D-2. and refering to 120D.3.1.1. Also change the PICs reference in RC1.

Proposed Response Response Status O

CI 120D SC 120D.5.4.1 P 365 L 39 # r02-61
Dudek, Michael Cavium

Comment Type T Comment Status X

Wrong equation

SuggestedRemedy

Change equation 93-3 to equation 120D-2.

Proposed Response Response Status O

CI 120E SC 120E.3.3.2.1 P 379 L 28 # r02-62
Dudek, Michael Cavium

Comment Type TR Comment Status X

The module output is tested with counter-propagating signals with a 19ps transition time 880mV amplitude (see 120E.3.2.1). The Host stressed input test should be calibrated with the same counter propagating signals. The amplitude is the same but the risetime is 12ps.

SuggestedRemedy

Align these risetimes. I recommend that both are set to 19ps, as it is likely that the stress test will be most difficult for high loss hosts which will have slower output risetimes.

Proposed Response Response Status O

CI 120E SC 120E.3.4.1.1 P 381 L 53 # r02-63
Dudek, Michael Cavium

Comment Type T Comment Status X

The host output is tested with counter-propagating signals with a 900mV amplitude and a slew time of 12ps between +/-0.27V (see 120E.3.1.6). The Module stressed input test should be calibrated with the same counter propagating signals. The amplitude is the same however a 20-80% transition time of 12ps is used instead of the slew time. 20 to 80% would be equivalent to the slew time from +/-0.27V but it would be better to use the same metric for both.

SuggestedRemedy

Change "target amplitude of 900 mV peak-to-peak differential and 20% to 80% target transition time of 12 ps as measured at TP4. " to ""target amplitude of 900 mV peak-to-peak differential and slew time of 12 ps between +/- 0.27 V. at TP4

Proposed Response Response Status O

IEEE P802.3bs D3.2 200 Gb/s & 400 Gb/s Ethernet 2nd Sponsor recirculation ballot comments

CI **120C** SC **120C.5.3** P **346** L **1** # **r02-64**
Maki, Jeffery Juniper Networks, Inc.

Comment Type **TR** Comment Status **X**

No where in 120C.5.3 Major capabilities/options is it listed that FEC is mandatory.
Furthermore, what FEC code is mandatory is not listed.

SuggestedRemedy

List the mandatory FEC code to make a compliant chip-to-module interface. Item:
FEC200; Feature: 200GBASE-R RS-FEC; Subclause: 119; Value/Comment: Device
implements Clause 119 RS-FEC for 200GBASE-R; Status: M; Support: Yes [] Item:
FEC400; Feature: 400GBASE-R RS-FEC; Subclause: 119; Value/Comment: Device
implements Clause 119 RS-FEC for 400GBASE-R; Status: M; Support: Yes []

Proposed Response Response Status **O**

CI **120E** SC **120E.5.3** P **387** L **1** # **r02-65**
Maki, Jeffery Juniper Networks, Inc.

Comment Type **TR** Comment Status **X**

No where in 120E.5.3 Major capabilities/options is it listed that FEC is mandatory.
Furthermore, what FEC code is mandatory is not listed.

SuggestedRemedy

List the mandatory FEC code to make a compliant chip-to-module interface. Item:
FEC200; Feature: 200GBASE-R RS-FEC; Subclause: 119; Value/Comment: Device
implements Clause 119 RS-FEC for 200GBASE-R; Status: M; Support: Yes [] Item:
FEC400; Feature: 400GBASE-R RS-FEC; Subclause: 119; Value/Comment: Device
implements Clause 119 RS-FEC for 400GBASE-R; Status: M; Support: Yes []

Proposed Response Response Status **O**