

PAM Modulation for 400G SMF

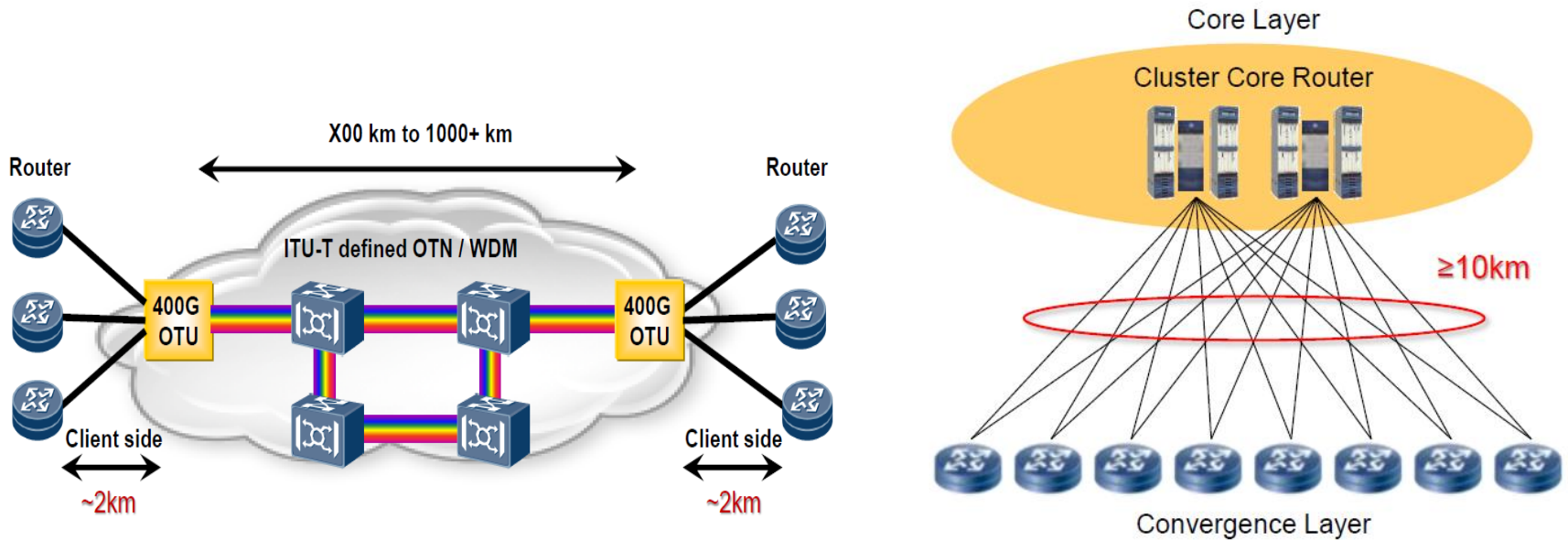
Sudeep Bhoja – Inphi
Frank Chang – Inphi

IEEE P802.3bs 400 Gb/s Ethernet Task Force, May 2014

400GE Reach Objectives

- IEEE 400G SMF has 3 reach objectives 500m, 2km, 10km
 - 2km - 10km, Client Optics, 6.3dB link loss budget
 - 500m – 2km, Inside Data Center, 4dB link loss budget
 - 1, 2 or 3 PMDs?

400G 2km - 10km Client Optics



http://www.ieee802.org/3/400GSG/public/13_07/song_400_01a_0713.pdf

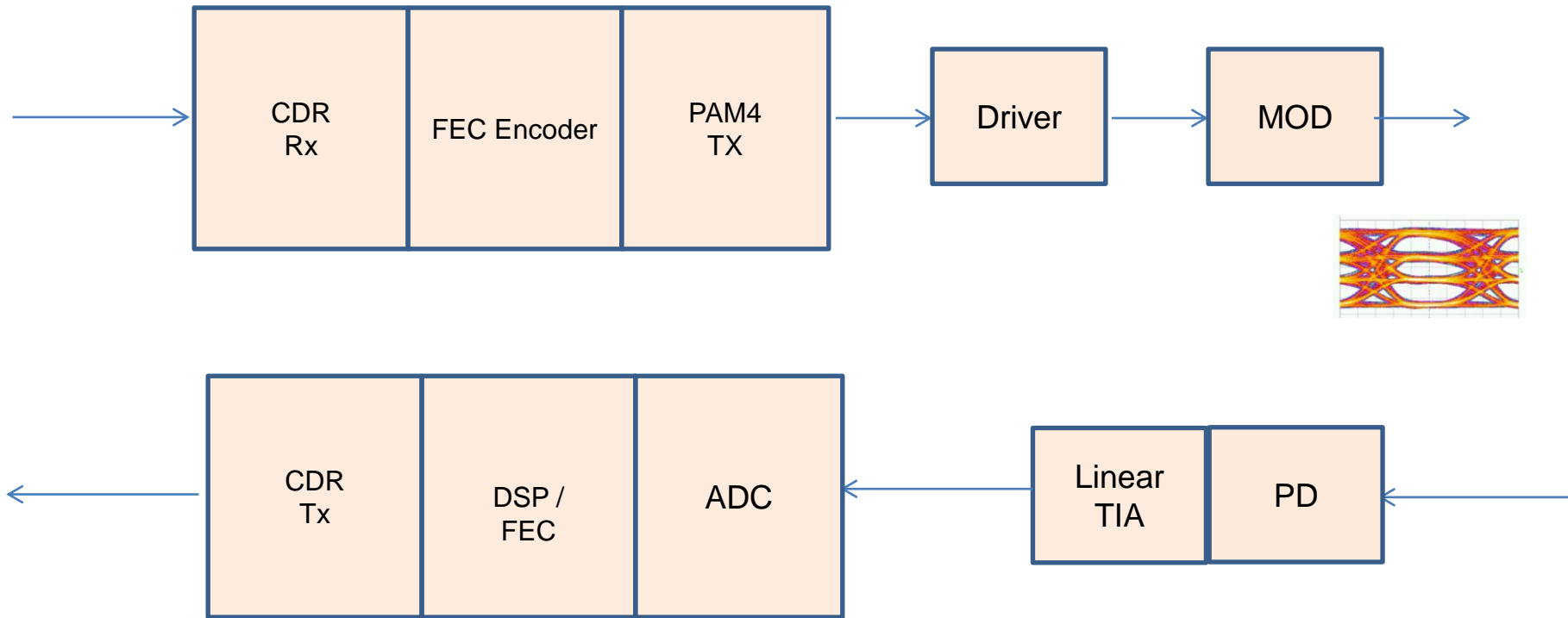
- Router to Router interconnect
- Router to OTN Transport interconnect
- CFP LR4 successfully deployed at 100G
- Multi-generational interoperability? Long term PMD?

400G 500m - 2km Data Center Optics

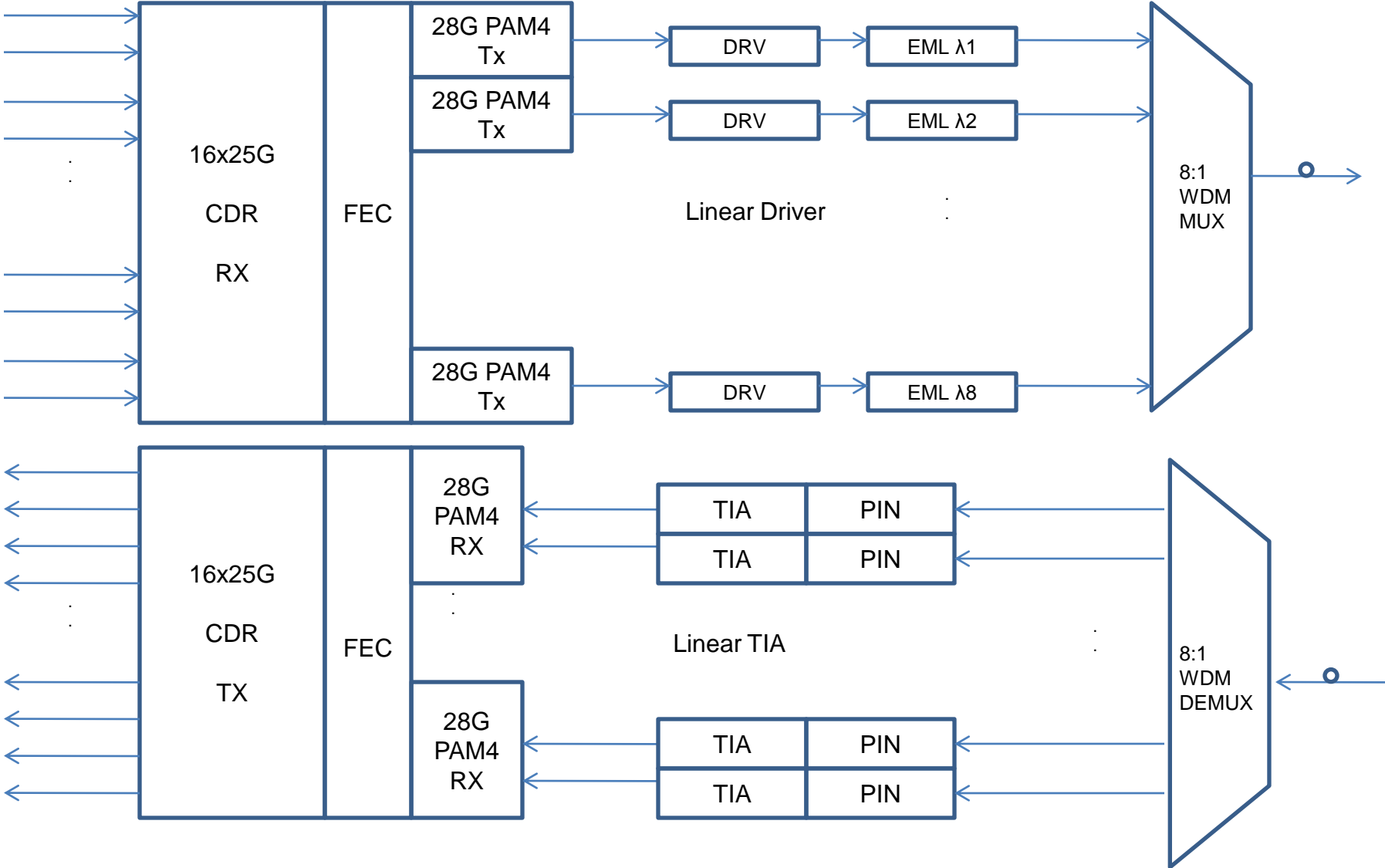


- Multiple MSAs, CLR4, PSM4, CWDM to address 100G cost challenges
- Data center requirement: 400G cost < 4x100G cost
- Support 400G uplinks **and** 4x100G leaf and spine breakout?

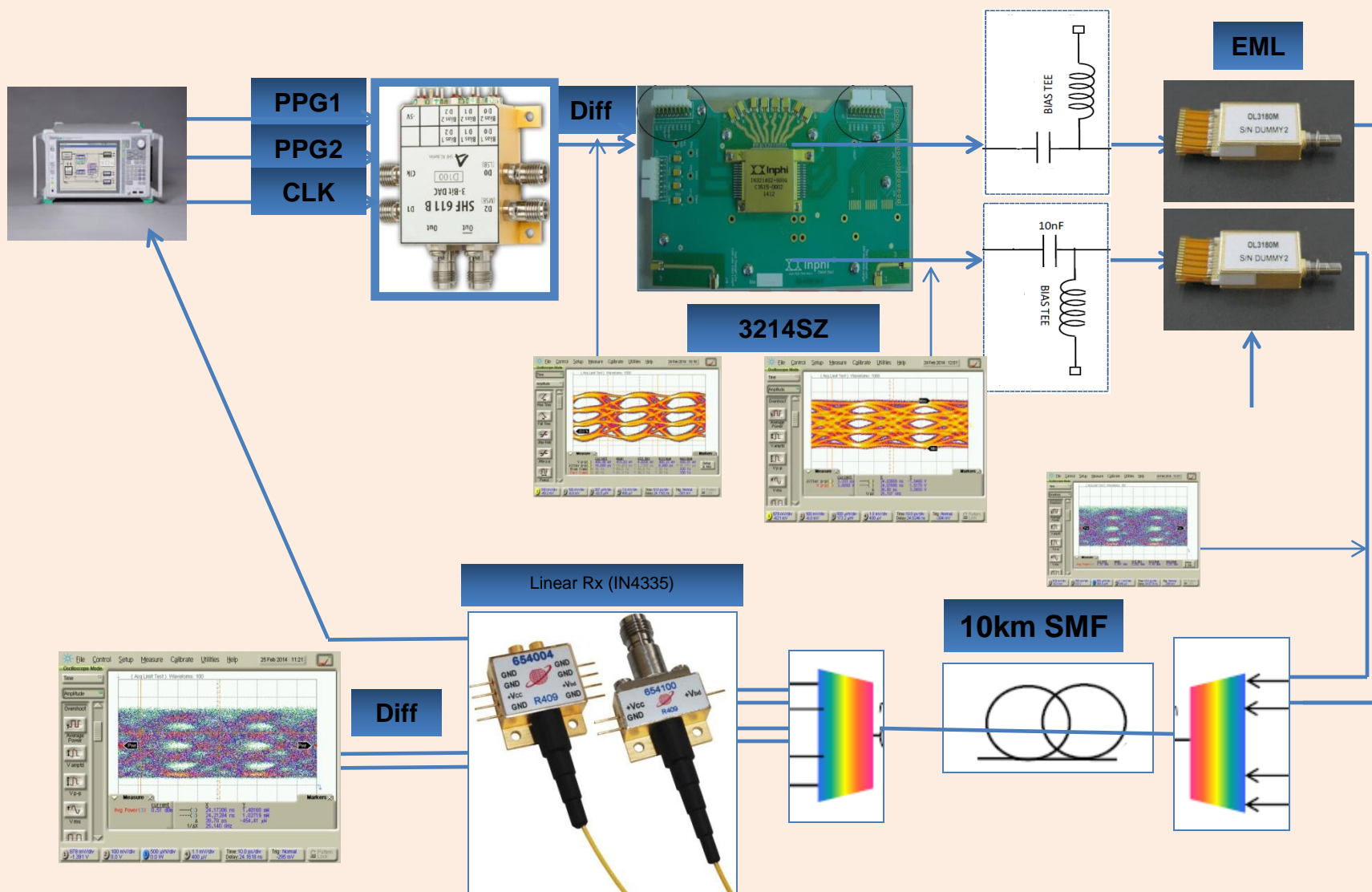
PAM4 TX & RX block diagrams



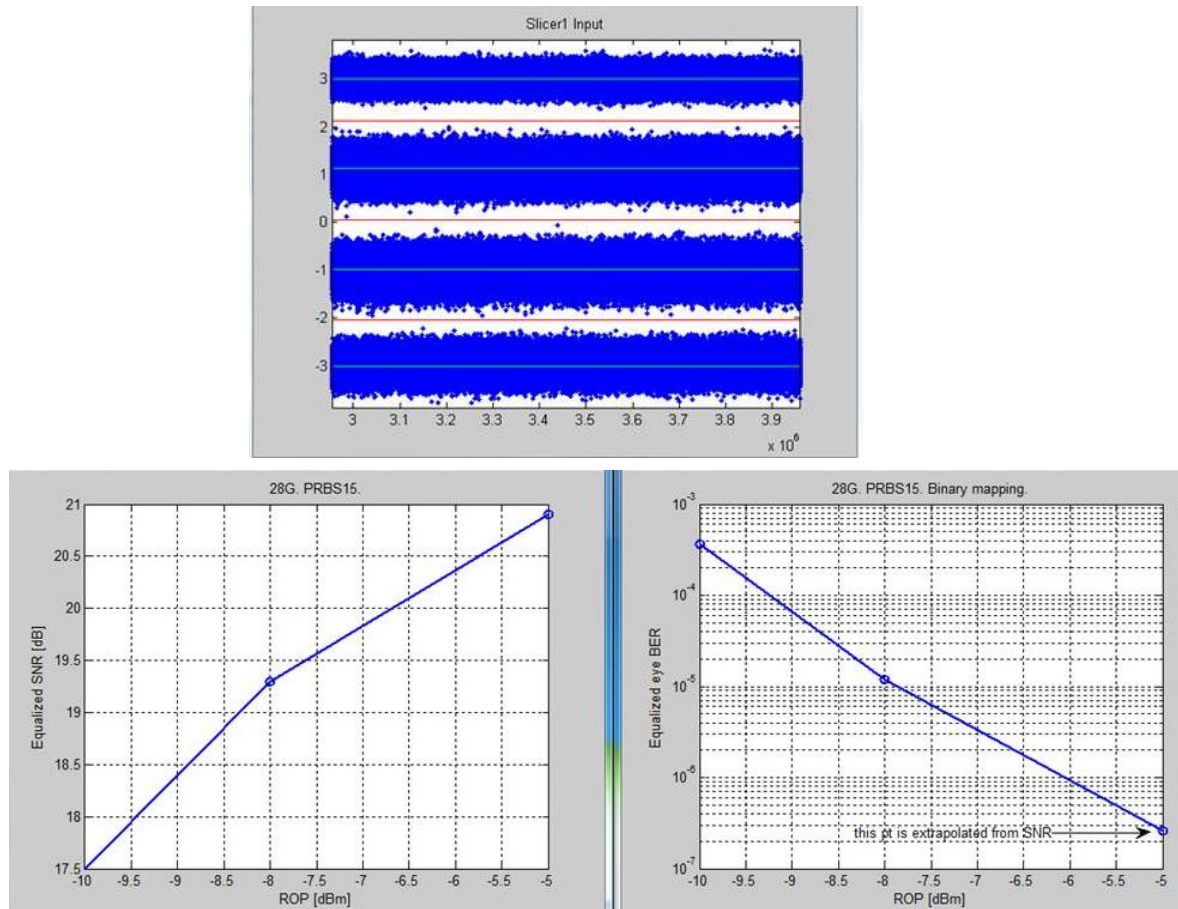
400G Using 8λ 56Gb/s PAM4



8λ 56Gb/s PAM4 Experimental Setup (10km)



8λ 10km Experimental DSP Results

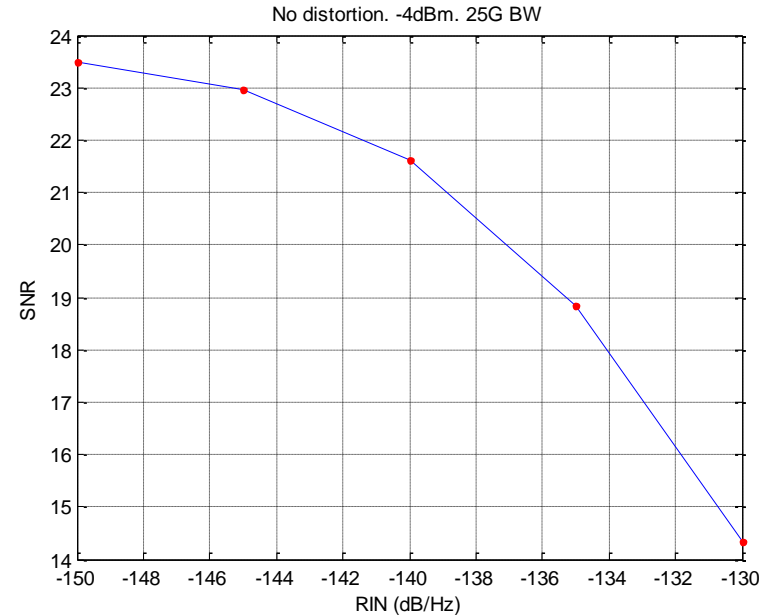
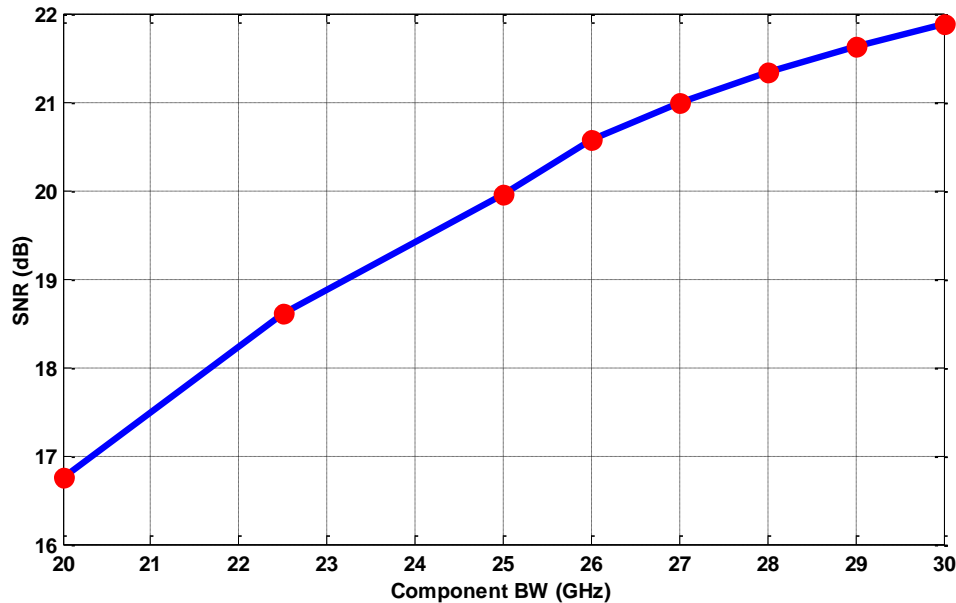


- Sensitivity better than -10dBm for $3E-4$ BER
- 4.2dB loss for 8λ Mux/Demux pair
- 6.3dB link loss budget can be supported

400G using 4 λ PAM4 (500m)

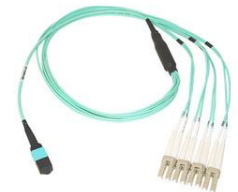
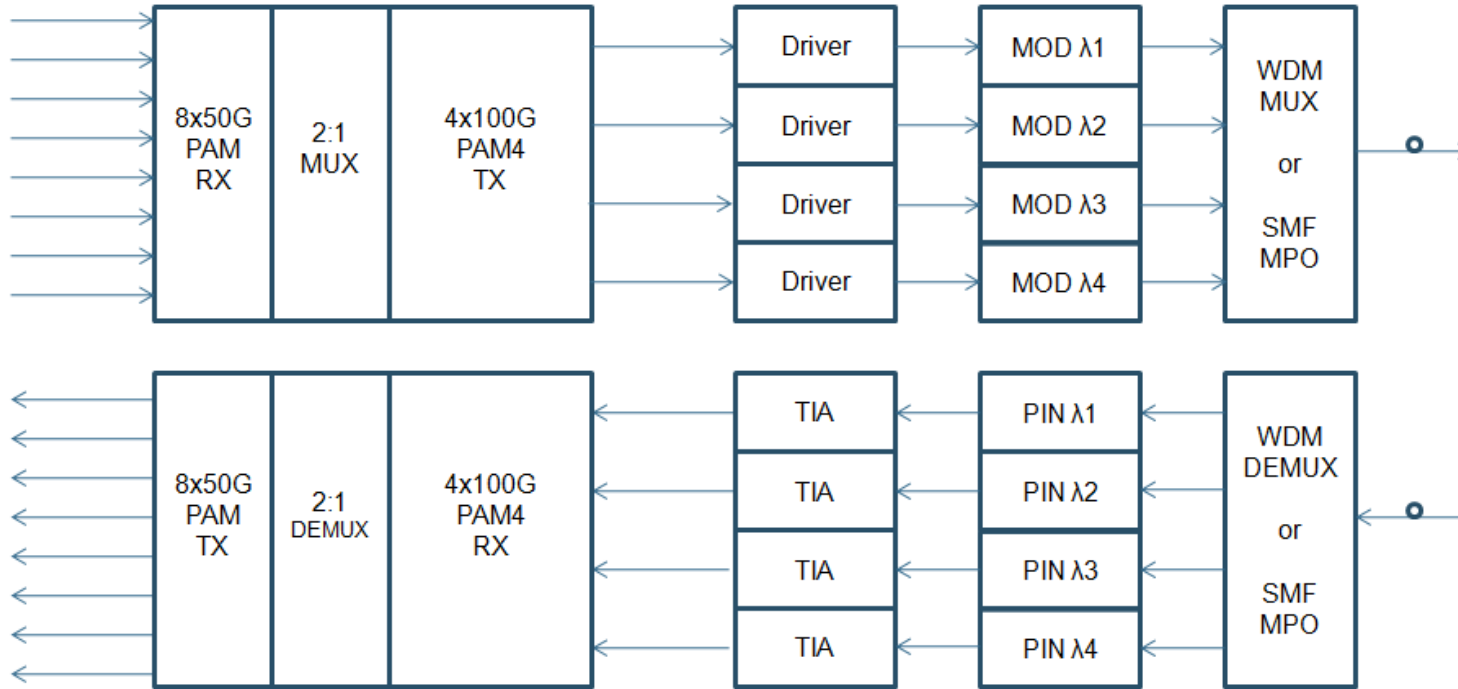
- 400G: Direct Detection 56GBaud PAM4
 - Modulation Speed: 28G \rightarrow 56GBaud
 - Higher Order Modulation: NRZ \rightarrow PAM4
 - Single λ Rate: 25G \rightarrow 100G
 - 4 λ : 100G \rightarrow 400G
- 56GBaud PAM4 lowers size, cost, power by shifting complexity to ICs

4λ PAM4 Simulation Results



- 4dB optical link budget can be supported
 - 25-30G component bandwidth, 20-22dB SNR
 - Improving RIN from -140 to -145 results in 1.35dB SNR gain
 - FEC gain can tradeoff optical specs
- Moore's law is alive and well
 - IC technology exists: 56GS/s ADC, DSP's, Linear TiA, Drivers etc.
 - 56G Optics, packaging and interconnect technology challenging

(100Gx4) 400G 4λ Solution



- 4x100G Optical: 4x (56GBaud PAM4)
- 4x100G Electrical: 8x (28GBaud PAM4)
- Supports 400G uplinks **and** 4x100G leaf and spine breakout

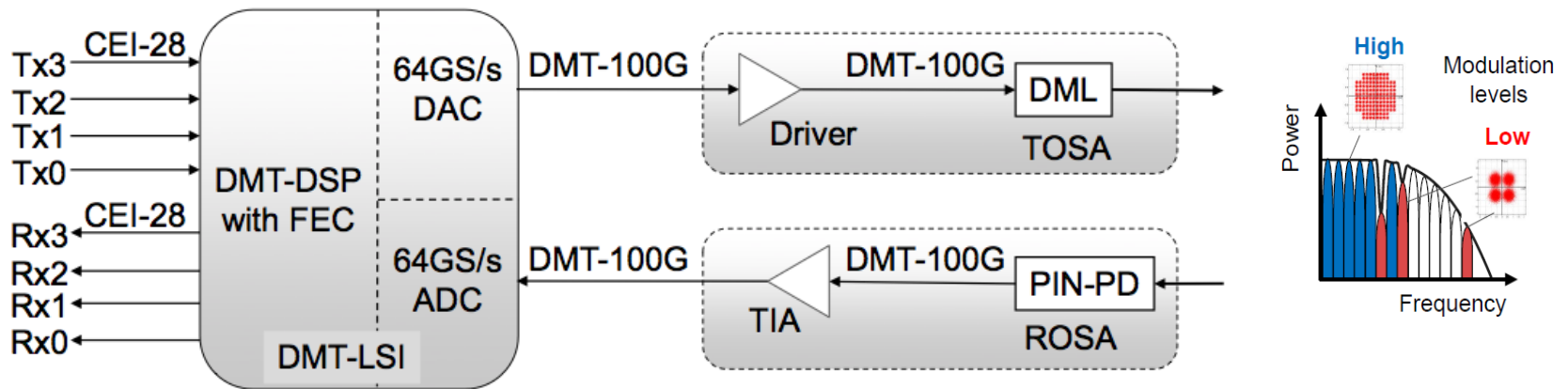
56GBaud PAM4 100Gb/s PAM-4 4λ 400G (4x100G)

400G PAM4 Options

	8λ	4λ
Time To Market	✓✓	
Electrical Interface	25Gb/s or 50Gb/s	25Gb/s or 50Gb/s
Optical Baud Rate (PAM4)	28Gbaud	56Gbaud
Optics Cost, Laser, Lenses, etc.	2x Optics BOM	✓✓
Optics Design, MUX/DMUX	8 channels	4 channels ✓
FEC Coding gain	8dB	9dB
High Speed Integrity and Package Design	✓✓	
ASIC Design	✓✓	✓
High Speed Modulator Design	✓✓	
Test Infrastructure	✓	Need high speed test gear

Higher Order Modulation using DMT

Optical DMT (Discrete Multi-Tone)



Note: Based on tanaka_01a_1112 and tanaka_01_0113, IEEE P802.3bm

DMT Experimental Results - 1

- Neophotonics, http://www.ieee802.org/3/400GSG/public/14_01/way_400_01a_0114.pdf

10km SMF, 4lambda 1294, 1299, 1304.5, 1308nm

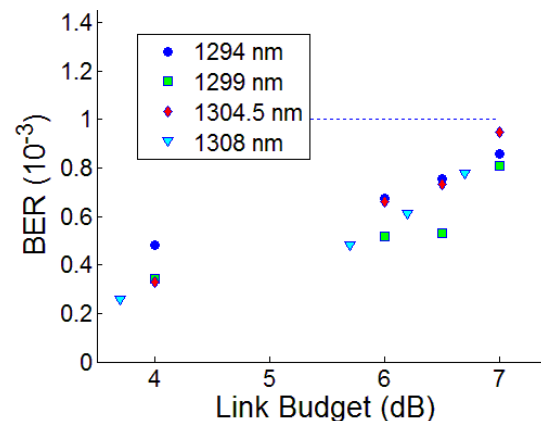
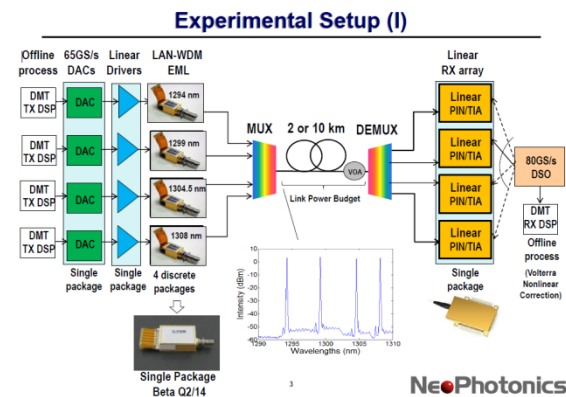
64Gs/s DAC, 80GS/s ADC,

176 subcarriers, 512 point IFFT

Volterra kernels: order = 3, memory depth = 4

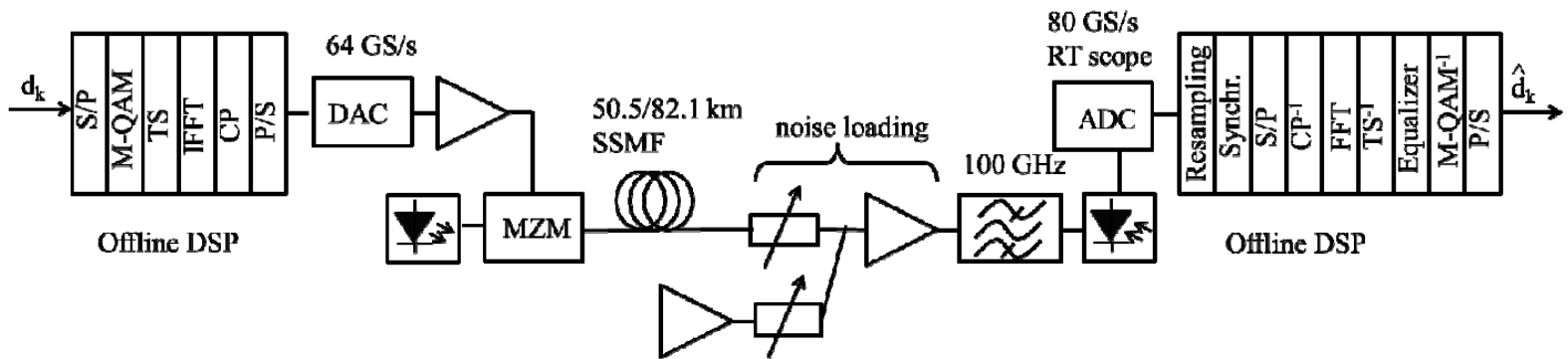
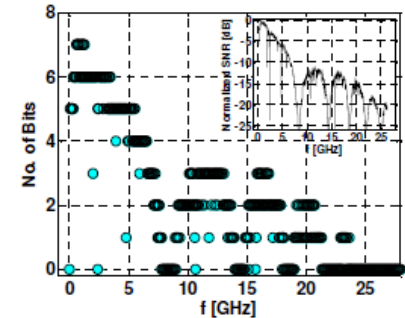
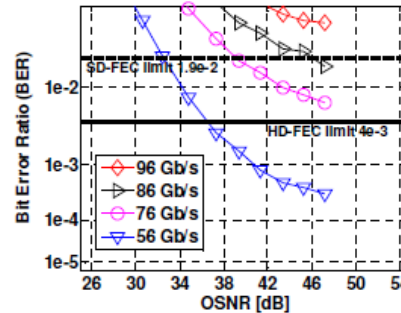
1E-3 BER demonstrated at 400G

Addition of SOA presents significant SNR penalty



DMT Experimental Results - 2

- Adva, OFC 2014, Tu2G.7, Annika Dochann, et al
- 1550nm, EDFA
- 64GS/s 8 bit DAC with BW of 13GHz
- Driver 30G BW
- MZM 40G BW
- 30G Real time Scope
- 2048 point IFFT



Source: OFC 2014, Tu2G.7, Annika Dochann, et al

DMT Experimental Results - 3

- Source: Fujitsu, OFC 2014 M2I.4
- 1310nm 40km, 80km with SOA, 0.33dB/km
- DML, 18GHz BW, 10dBm
- NLE 31 taps compensates for non-linearity
- Achieves 80km, 1E-3 BER

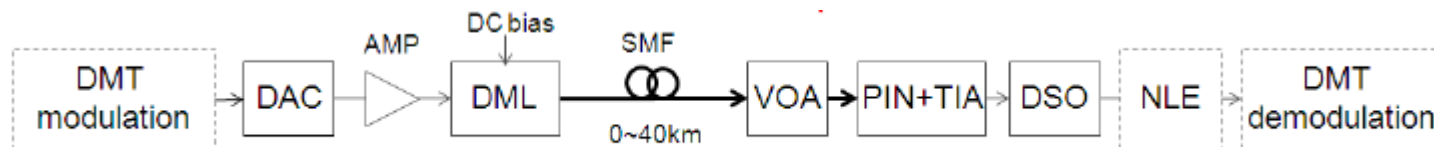


Fig. 1. Experimental setup for 0~40km transmission

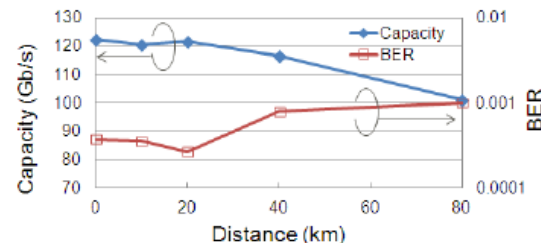


Fig. 12. Capacity and BER for 0~80km transmission

PAM4 vs. DMT IC Comparison

	PAM4	DMT	Complexity
Equalizer	FFE, DFE	IFFT,FFT	
Complexity (Multiply-Acc)	x	10x	Dominated by FFT/IFFT complex multiplications
DAC resolution	2 bits	8 bits	DMT Clipping issues
ADC Power	x	1.5 - 2x	ENOB, Peak to avg. ratio
FEC	x	x	DMT higher coding gain?
Non Linear Canceller	n/a	Volterra	DMT is more sensitive to non-linearity
Bandwidth	32G	20G	PAM requires higher BW
Serdes	x	x	
Total IC Power	Y	2.5Y	

- CMOS Power consumption estimates
 - 1.5W for PAM4, 3.5W for DMT per 100G

Summary

- 10km telecom Client Optics and 500m cost optimized data center are different
- Experimentally demonstrated 56Gb/s PAM4
- Simulated 112Gb/s PAM4, good progress towards experimental demonstration
- Investigated tradeoffs between 8λ 56Gb/s PAM4 and 4λ 112Gb/s PAM4
- Investigated tradeoffs between PAM4 and DMT
- DMT IC power is $>2x$ PAM4 IC power