400GBASE-SR16

May 2014

Jonathan King, Finisar Corp

John Petrilla, Avago Technologies

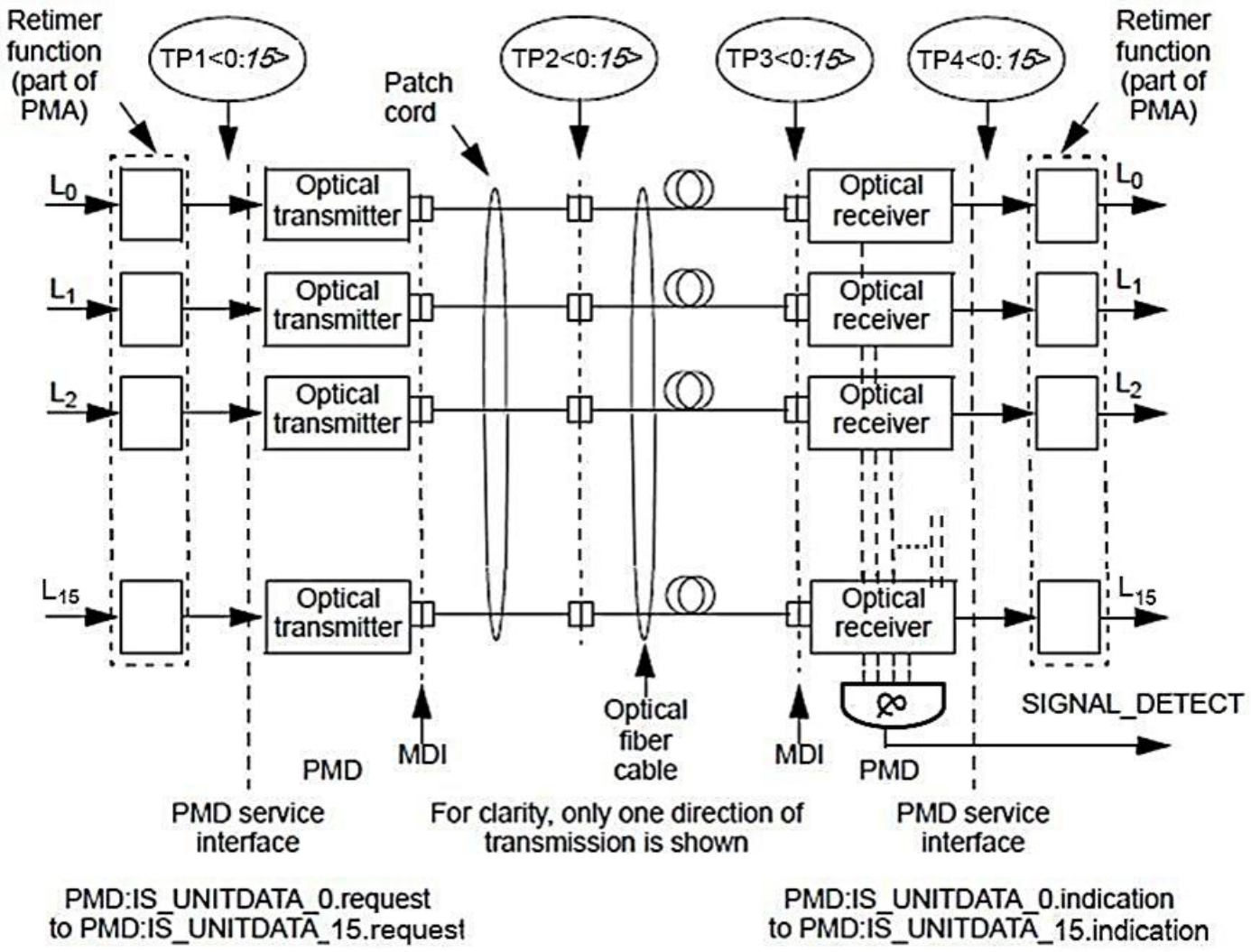
Background

- 400G Ethernet (1st generation) is likely to use a 16 lane 25 Gb/s electrical interface (in each direction).
  - 16x25G most favoured electrical interface in a straw poll at 29th April 2014 Ethernet Alliance 400Gb/s Subcommittee meeting.
- Lowest cost, lowest power, PMDs tend to have a 1:1 mapping of electrical lanes to optical lane.
- Low initial volume for 400G MMF modules, probably dominated by breakout applications.
- 2x16 fibre connector: physical contact and expanded beam ferrules are in development.
  - "400G Optical Interconnection Options", Nathan Tracy, 29th April 2014, Ethernet Alliance 400Gb/s Subcommittee meeting.

Re-use of 100GBASE-SR4 specs

- The 100GBASE-SR4 specs define PMD with four parallel optical fibres (for each direction), and provide FEC supported reach of 100 m on OM4.
- Re-use of 100GBASE-SR4 specs for a 400G:
  - requires no gearbox
  - supports breakout applications relatively easy
  - needs no new optical components (same optics work for first generation 400G Ethernet on MMF)
  - minimizes investment cost and development time scales
  - could be implemented as four 100GBASE-SR4 modules, or a single 400GBASE-SR16 module.

400GBASE-SR16 block diagram



Characteristics of 25Gb/s lanes for 100GBASE-SR4

Transmitter	Value	Unit
Center wavelength (range)	840 to 860	nm
RMS spectral width	0.6	nm
Average launch power, each lane (max)	2.4	dBm
Average launch power, each lane (min)	-9.1	dBm
Optical Modulation Amplitude (OMA), each lane (max)	3	dBm
Optical Modulation Amplitude (OMA), each lane (min)	-7.1	dBm
Launch power in OMA at max TDP (min)*	-3	dBm
Extinction ratio	2	dB

Receiver	Value	Unit
Average receive power, each lane (max)	2.4	dBm
Average receive power, each lane (min)	-11	dBm
Receive power, each lane (OMA) (max)	3	dBm
Stressed receiver sensitivity, each lane (OMA) (max), at BER=5×10^{-5}	-5.6	dBm
Informative receiver sensitivity, each lane (OMA) (max)*, at BER=5×10^{-5}	-11.2	dBm

*Though not explicit specs for 100GBASE-SR4, these values underpin the 8.2 dB link budget and 1.9dB channel insertion loss budget of 100GBASE-SR4, and reflect expected performance of 25Gb/s components.

Target BER

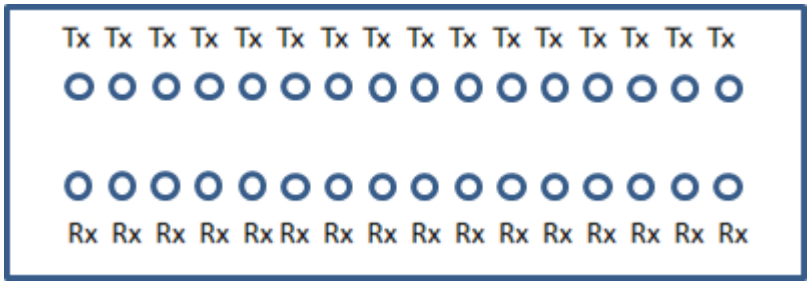
- 802.3bs targets a BER at the MAC/PLS service interface of better than or equal to 10^{-13} , *(anslow_400_02_1113).*
- 100GBASE-SR4 target is 5×10^{-5} at the PMD/PMA interface

  ‘provided that the error statistics are sufficiently random that this results in a frame loss ratio (FLR) (see 1.4.210a) of less than 6.2×10^{-10} for 64-octet frames with minimum inter-packet gap when processed according to Clause 91’.
- Following *anslow_01a_1112_mmf :*
  - A pre-FEC BER of $5x10^{-5}$, with random error statistics, and no errors contributed by electrical traces, results in a Frame Loss Ratio of 6.2×10^{-10}, equivalent to a corrected BER of $6.7x10^{-13}$.
    - Equivalent Q = 3.89
  - A pre-FEC BER of $3.8x10^{-5}$, with random error statistics, and no errors contributed by electrical traces, results in a Frame Loss Ratio of 6.2×10^{-11} , equivalent to a corrected BER of $1x10^{-13}$.
    - Equivalent Q = 3.96

Concluding remarks

- A 400Gb/s PMD which re-uses 100GBASE-SR4 optical lane specifications:
  - allows FEC supported 100m reach over OM4
  - minimizes technical risk
    - no new optics needed
    - optical 2x16 connectors available well within the time frame of 802.3bs project
  - is compatible with early adopter breakout applications
  - apparently almost meets 802.3bs target BER of 10^{-13}
    - some further work needed here.

Appendix : Proposed MDI lane assignments



- Lowest cost/smallest form factor is enabled with separate rows for Tx and Rx lanes
- Tx ‘on top’, closest to heat-sink for best thermal management, critical in many form factors, including board mounted optics