

PAM4 MODULATION FOR THE 400G ELECTRICAL INTERFACE



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IEEE 802.3bs 400Gb/s Task Force
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San Diego, CA

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- Sudeep Bhoja, Inphi
- Nathan Tracy, TE
- Megha Shanbhag, TE
- Mike Furlong, Clariphy
- Scott Powell, Clariphy
- Howard Frazier, Broadcom
- Vasu Parthasarathy, Broadcom
- Will Bliss, Broadcom

- **Scenario**

- Data rate: 50Gbps
- Transcoding: 64/66
- Signaling: PAM4
- Signaling rate: 25.78125Gsps

- **Targets**

- Low power scheme
- Extendable to higher loss channels

- **Analysis**

- Uncoded performance (no FEC)

- **Source**

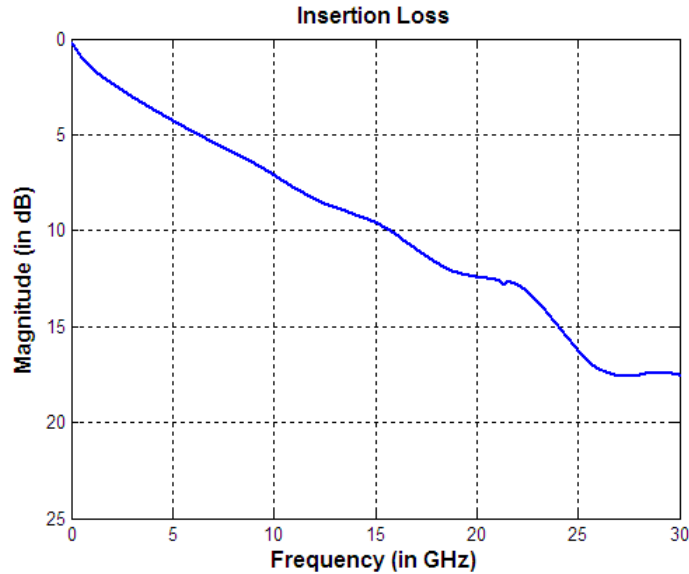
- OIF 2014.142.00 (56G VSR)
- Nathan Tracy, TE Connectivity

- **Channel 1**

- Next generation 28Gbps high density SMT IO
- IL: 9.2dB loss @14GHz
- XT: 5 FEXT, 0 NEXT

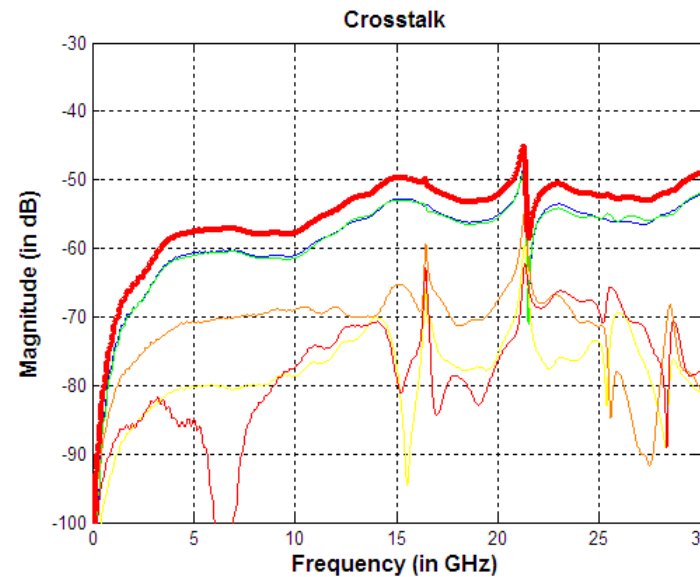
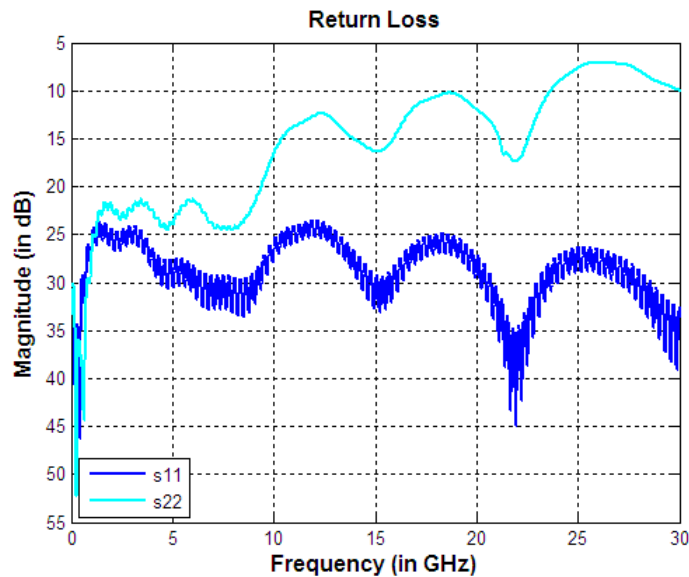
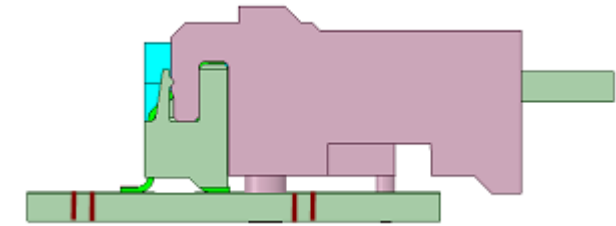
- **Channel 2**

- Next generation 28Gbps press-fit stacked IO
- IL: 9.1dB loss @14GHz
- XT: 11 FEXT, 0 NEXT



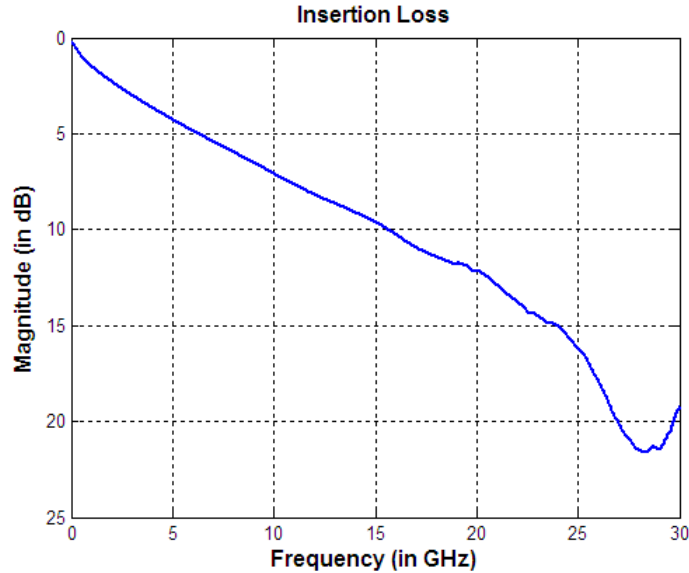
■ Host PCB

- 2.86mm thick, 23 Layers(12 GND planes)
- 2 Layer route out (Layer 10,12)
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 8mil stub on signal vias
- 7.3 dB stripline trace loss added



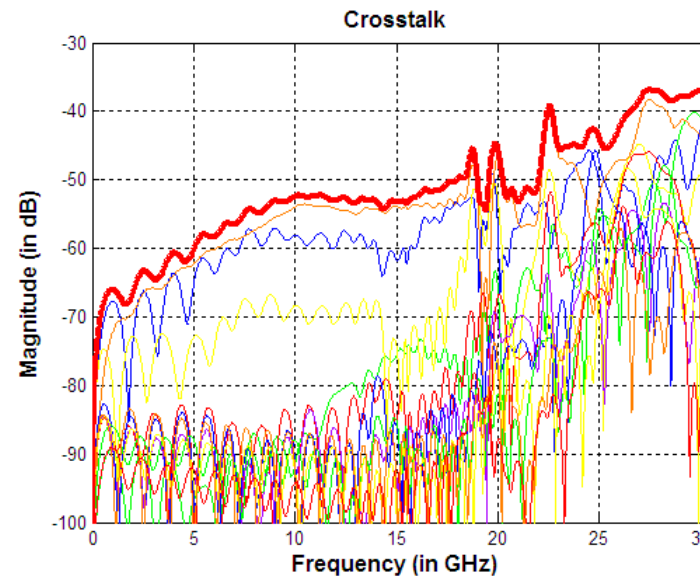
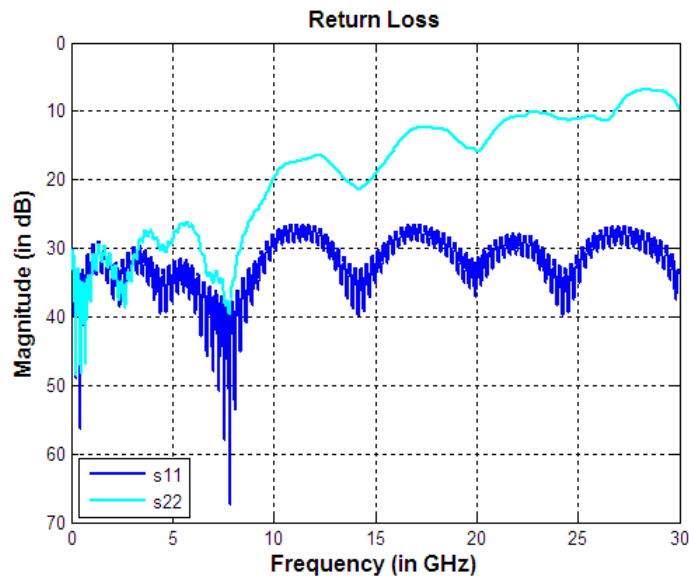
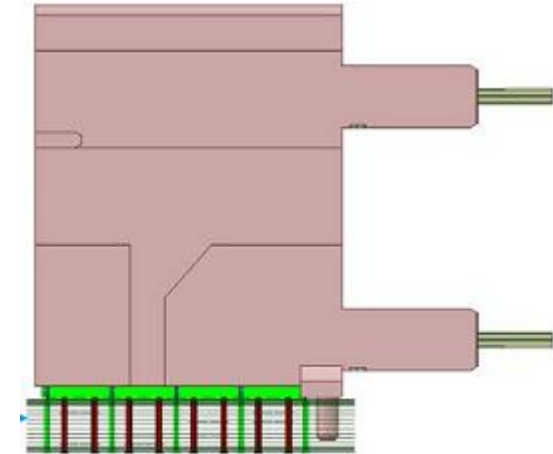
■ Module PCB details

- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 1.2 dB microstrip trace loss added



Host PCB

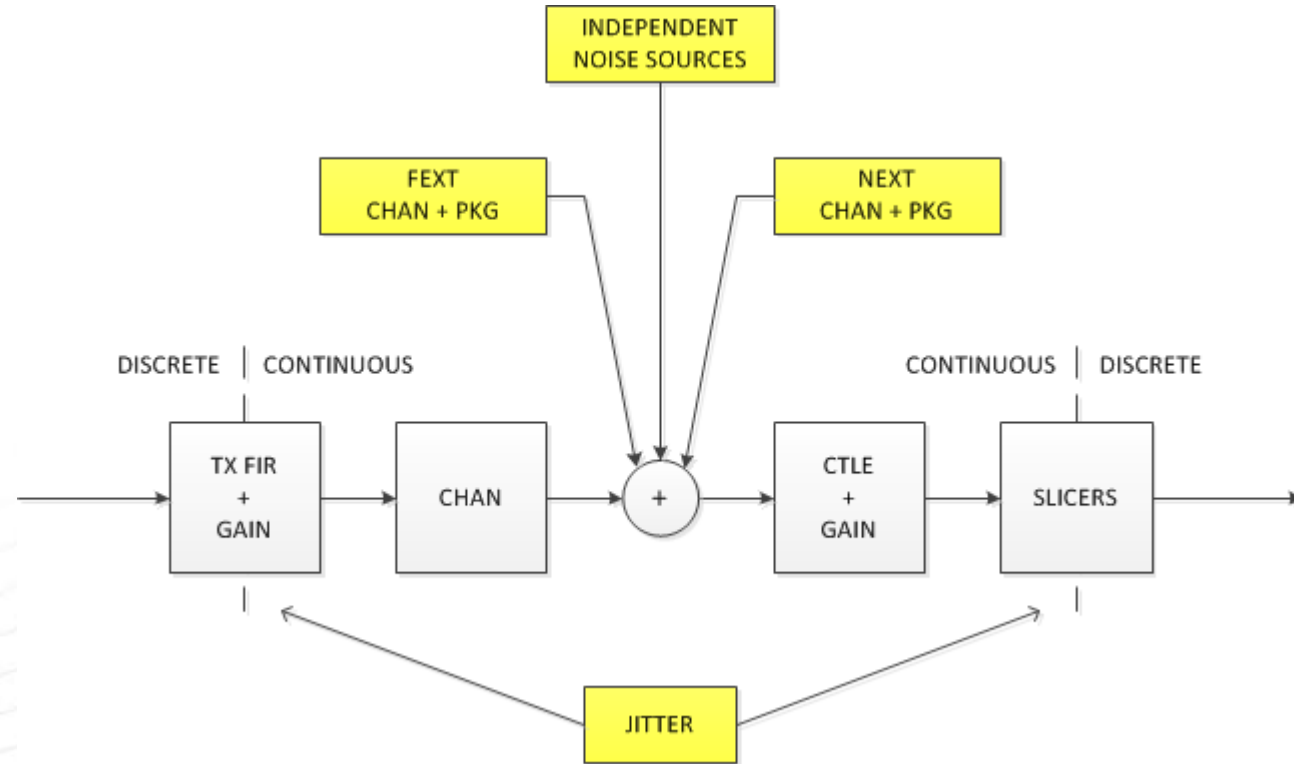
- 3.425mm thick, 26 Layers (15 GND Planes)
- 4 Layer route-out (Layers 7, 11, 17, 21)
- EM-888 Material (Dk=3.8, Loss Tangent=0.012)
- 8mil stub on signal vias
- 7.3 dB stripline trace loss added



Module PCB details

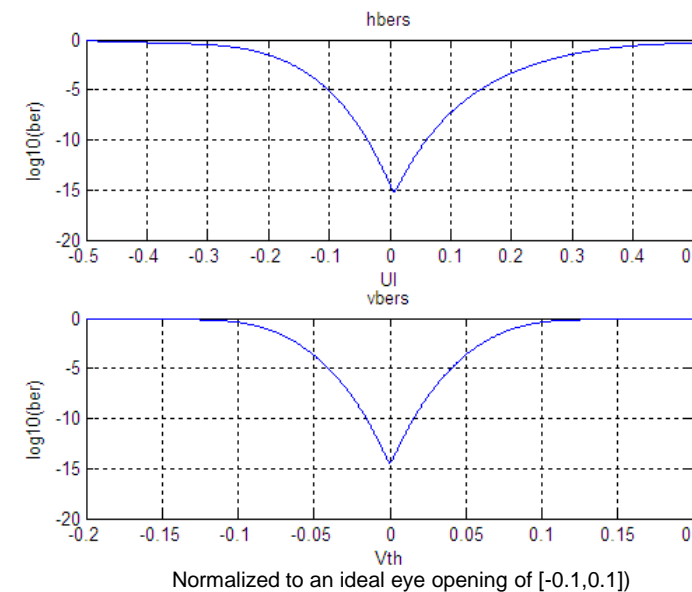
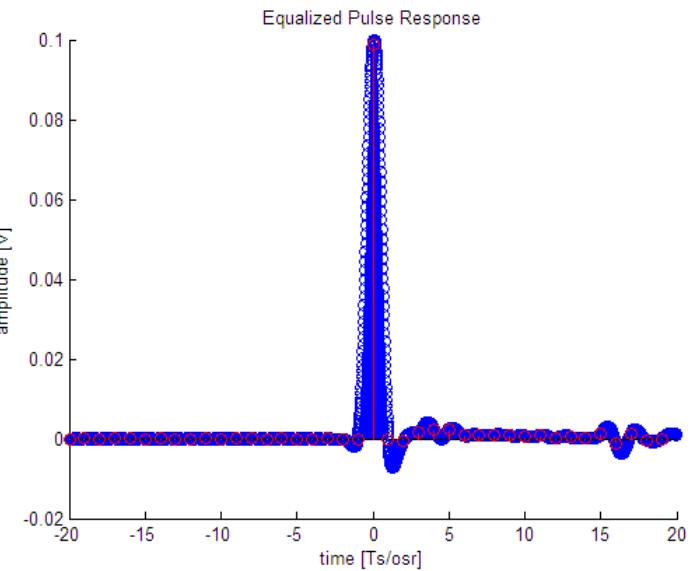
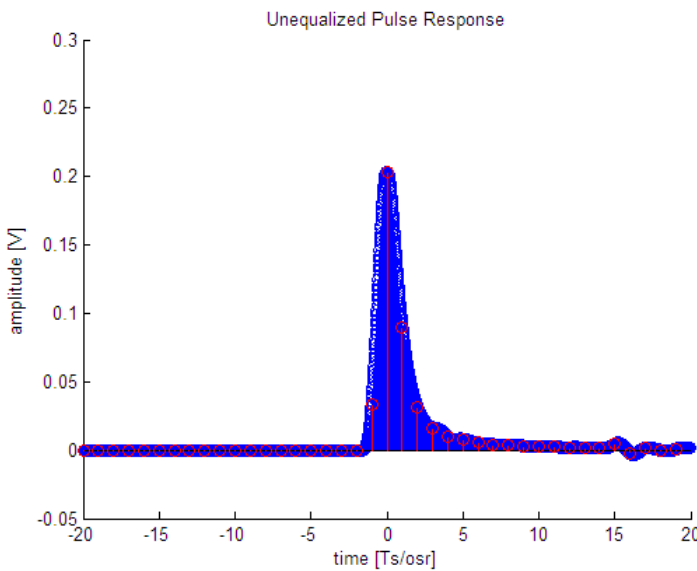
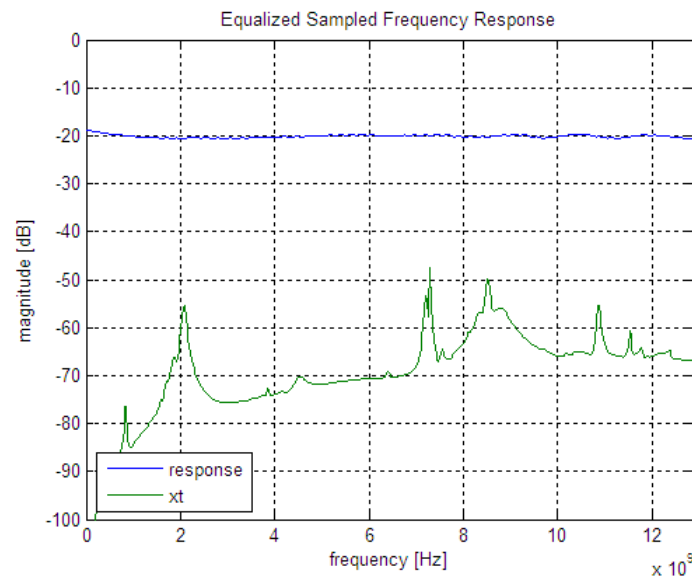
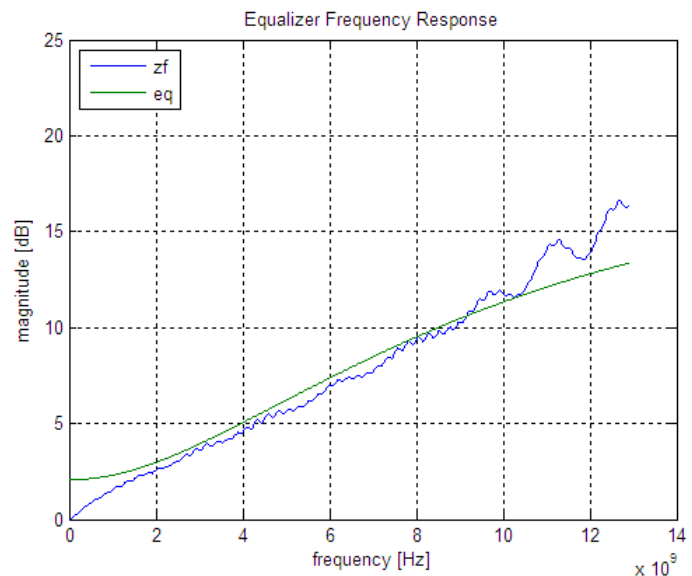
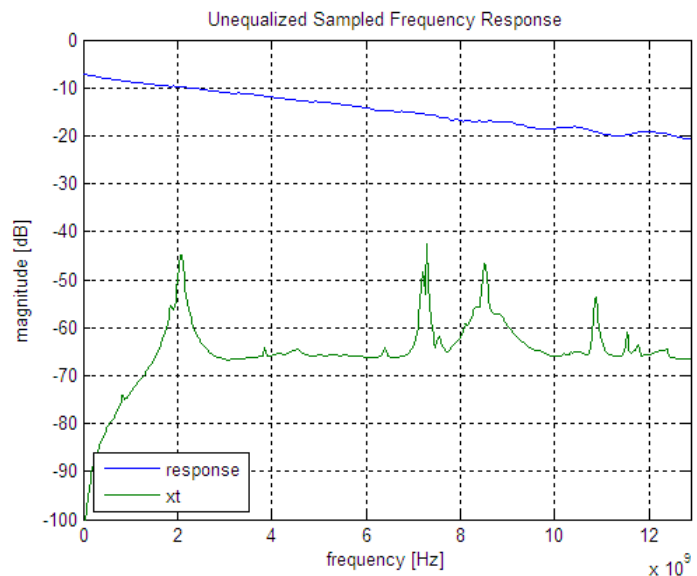
- 1mm thick, 6 layer PCB (4 GND Planes)
- Microstrip trace route-out from 0.35x1.4mm mating pads
- Nelco 4000-13SI Material (Dk=3.32, Loss Tangent=0.010)
- 1.2 dB microstrip trace loss added

- Signaling: PAM4
- Signaling rate: 25.78125Gbps
- No coding
- CTLE
 - 2 real zeros
 - 2 real poles @ 25GHz
- TXFIR
 - Option 1: 3 coefs, 1 pre, 1 post
 - Option 2: 5 coefs, 1 pre, 3 post

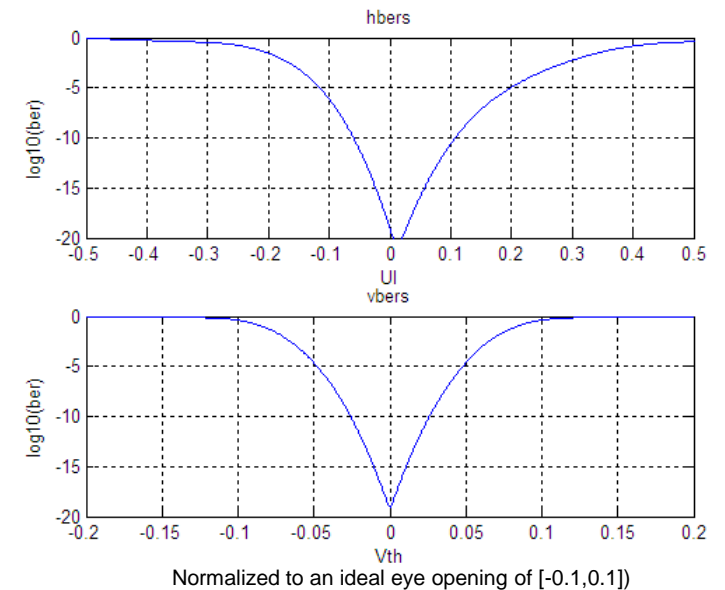
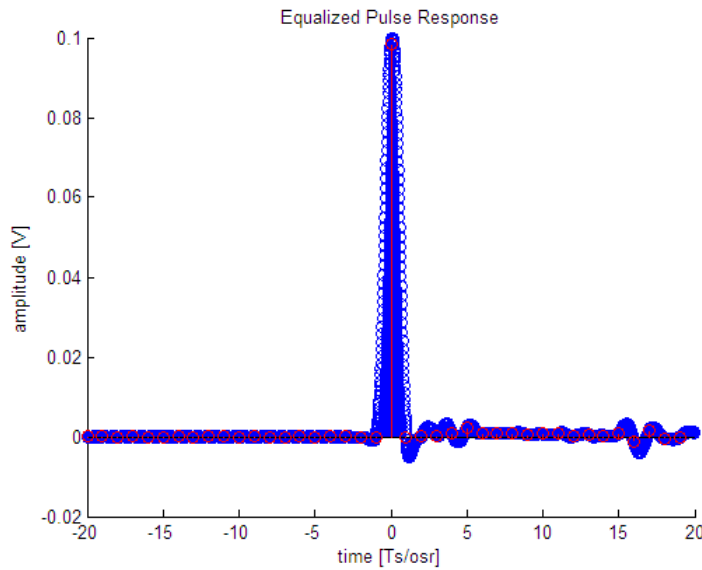
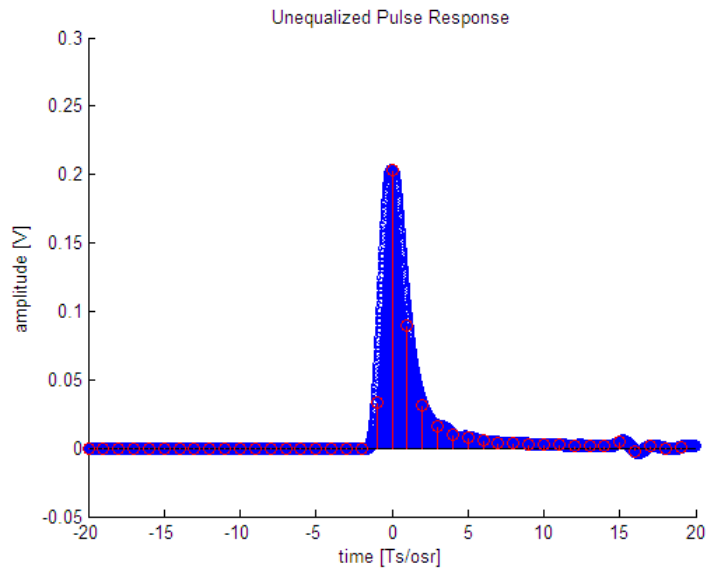
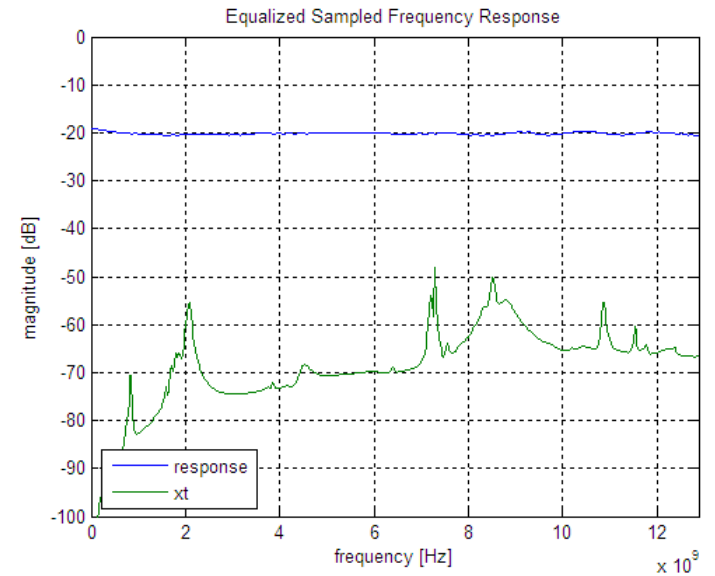
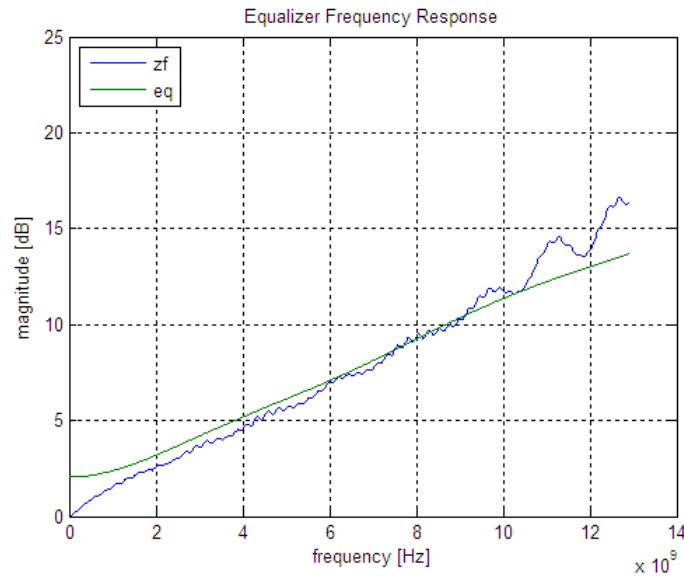
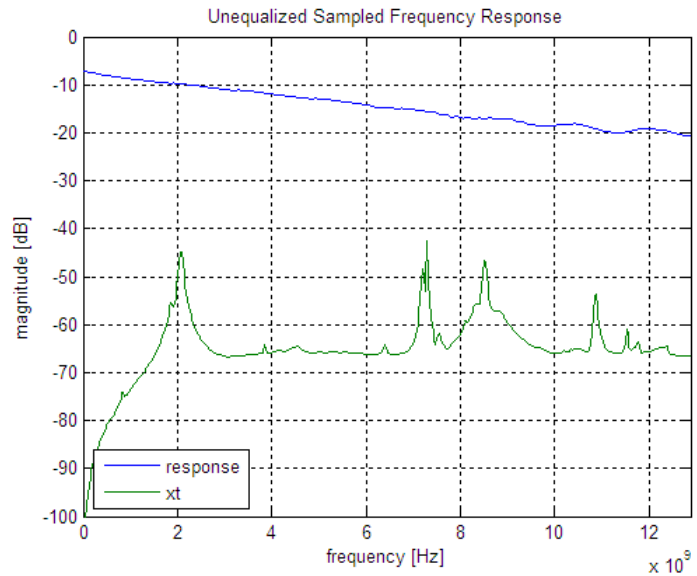


- Analog IO signal models based on existing 28nm, 25G NRZ design
- Package XT models based on existing 28nm, 25G NRZ design
- Aggressors assumed filtered by same TX FIR as victim
- RX input referred white noise -155dBm/Hz (~1.6mV rms)
- Slicer offset $\sim \pm 2\%$
- Jitter $\sim 0.2UI$ p2p
 - TX, RX, and CDR

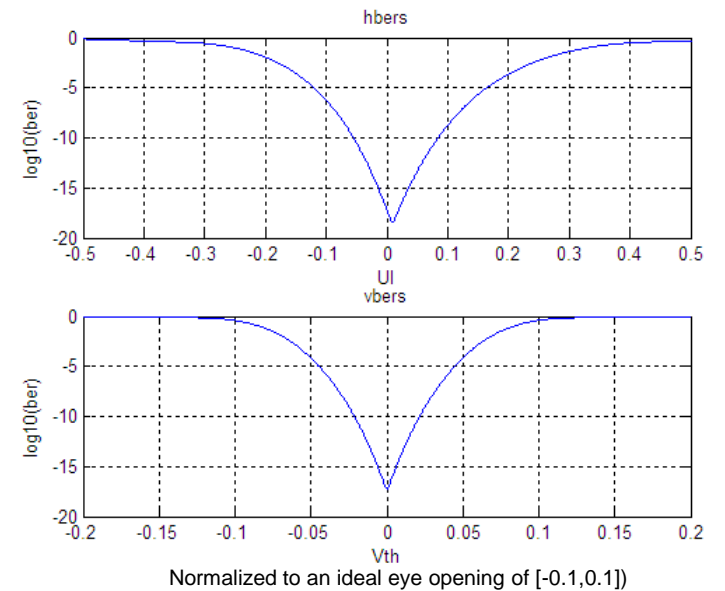
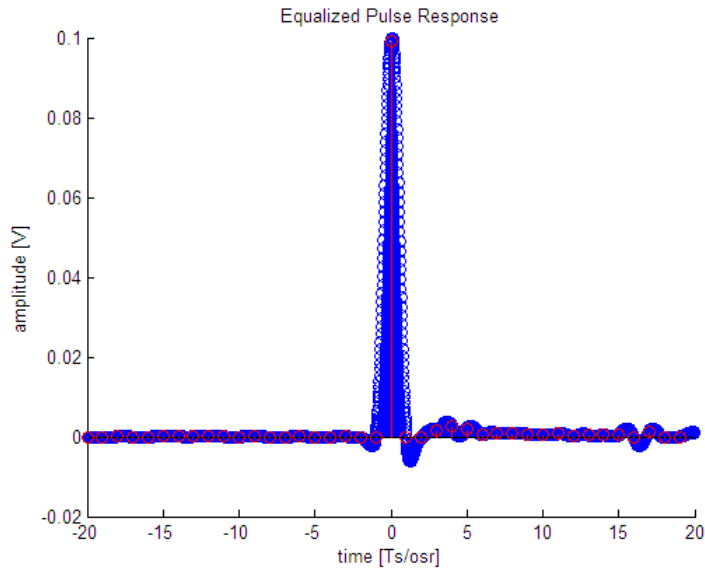
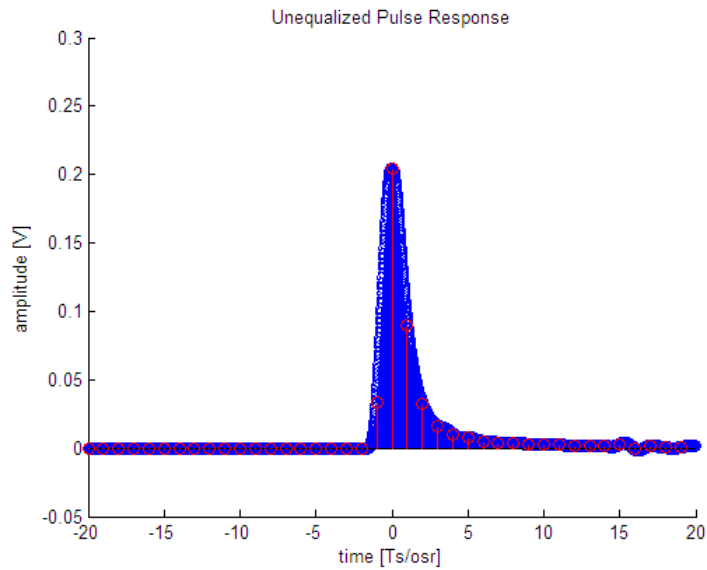
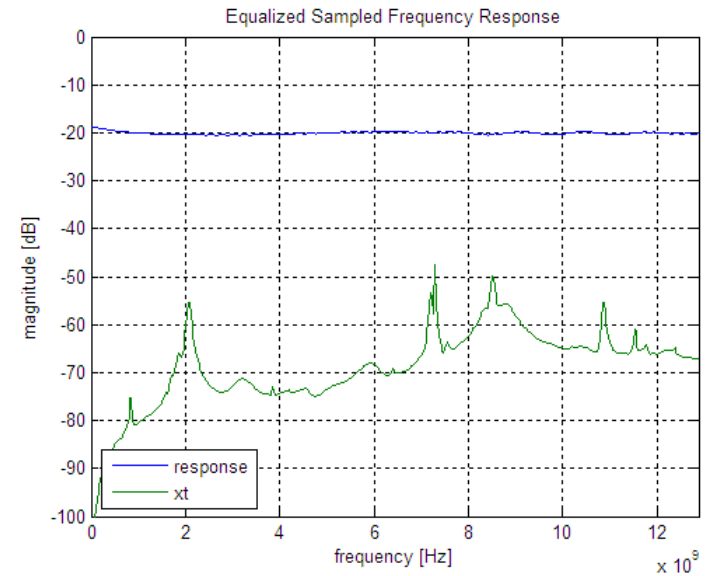
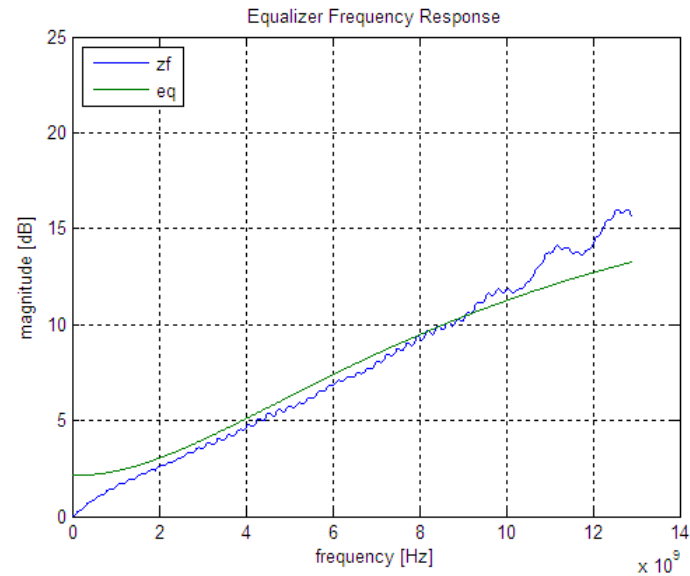
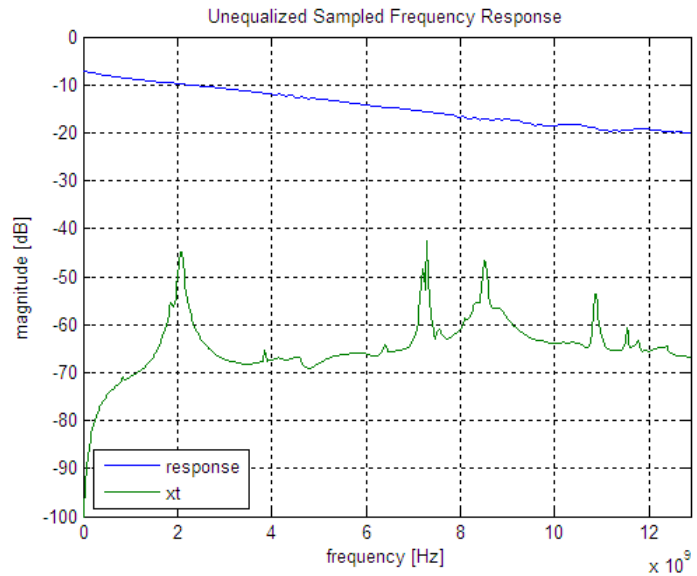
OIF2014.149.01, 9.2DB, 5 FEXT – 3-TAP TX FIR



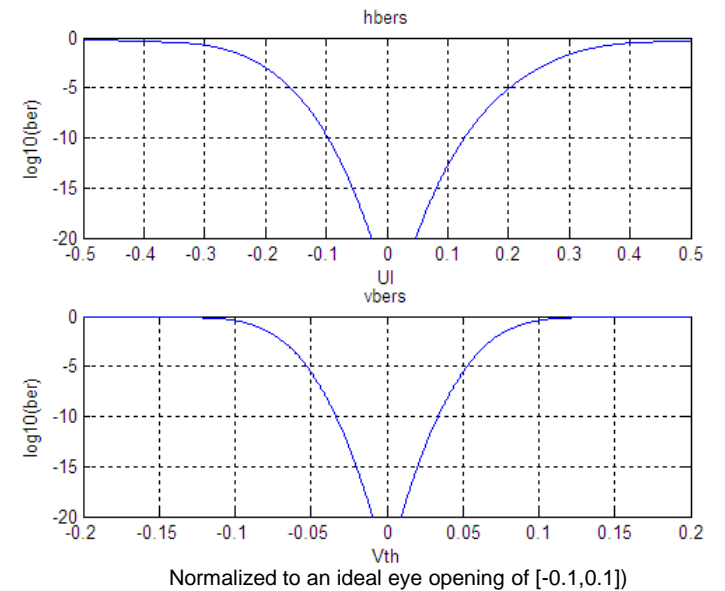
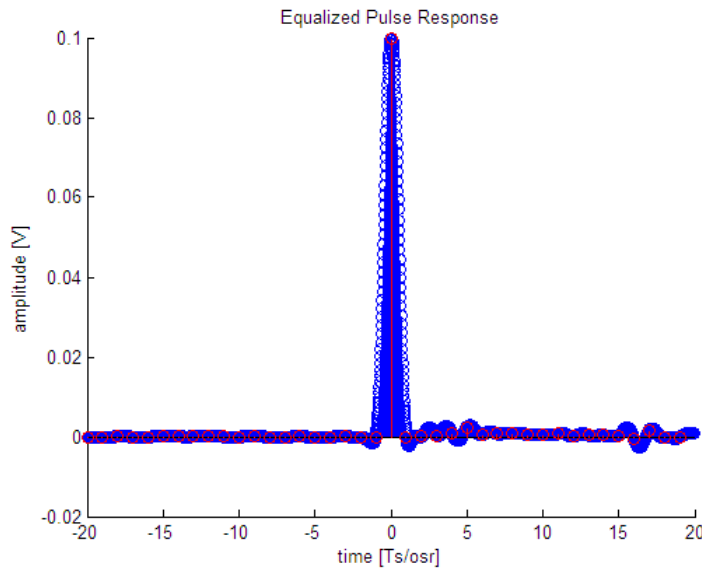
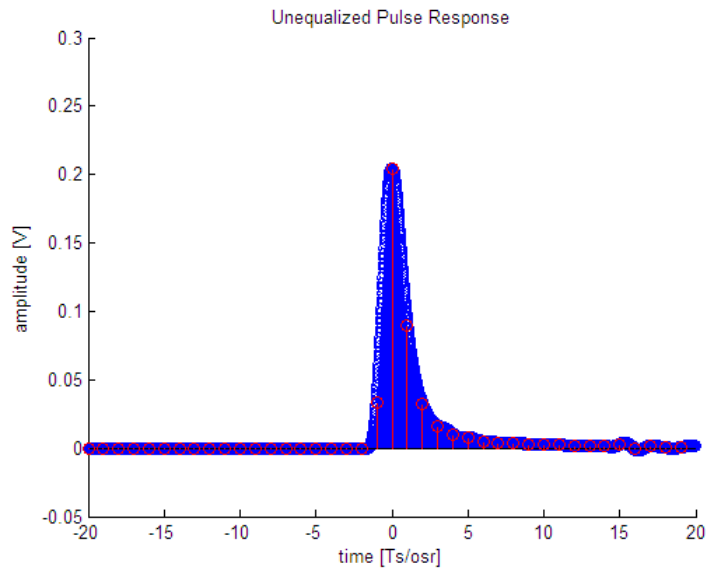
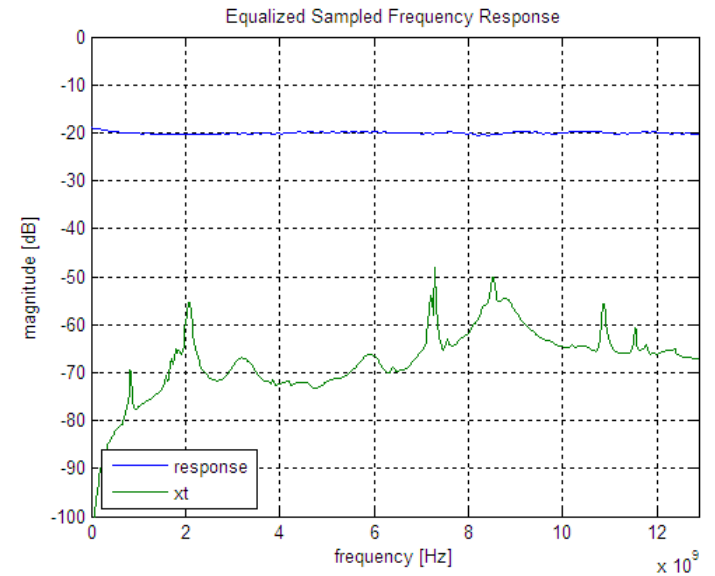
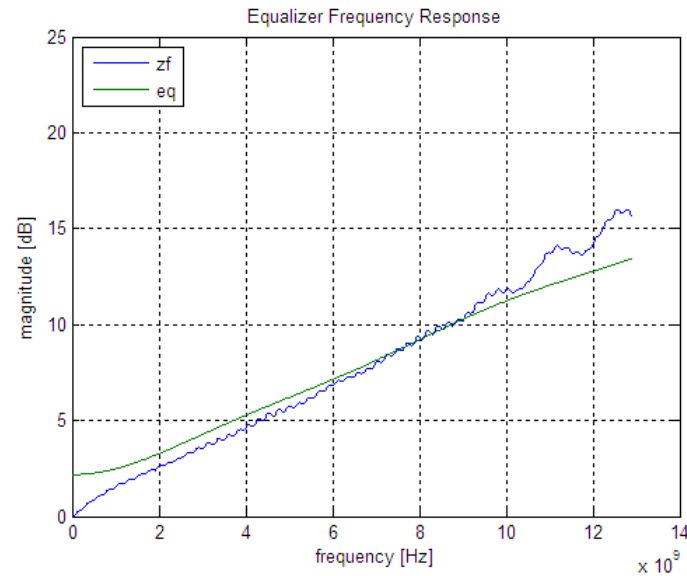
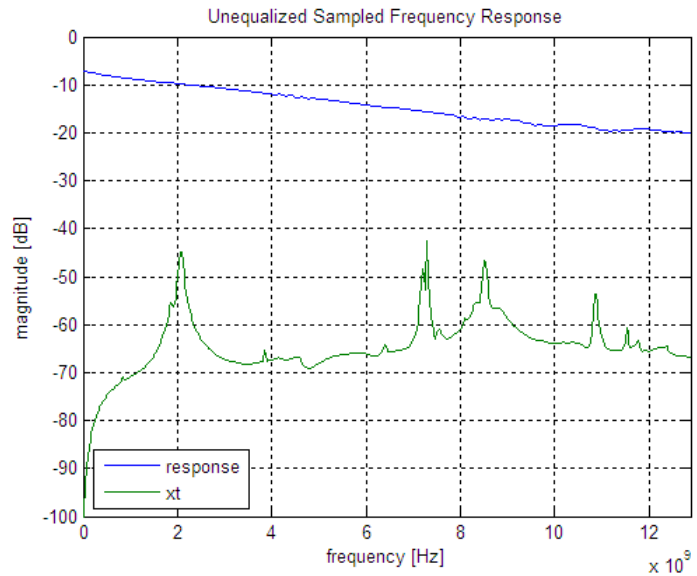
OIF2014.149.01, 9.2DB, 5 FEXT – 5-TAP TX FIR



OIF2014.150.00, 9.1DB, 11 FEXT – 3-TAP TX FIR



OIF2014.150.00, 9.1DB, 11 FEXT – 5-TAP TX FIR



Channel	BER	
	3-tap Tx FIR	5-tap Tx FIR
OIF2014.149.01, 9.2dB IL, 5 FEXTs	4×10^{-15}	9×10^{-20}
OIF2014.150.00, 9.1dB IL, 11 FEXTs	6×10^{-18}	1×10^{-25}

- **Meets BER requirement of 10^{-18} , without FEC**
- **Simple scheme, allows low-power implementation**
- **No DFE → No error propagation issues**
- **Extendable to higher loss channels**
 - Additional mechanisms (coding, precoding, etc.)