A CDAUI-16 Chip-to-Chip (c2c) and Chip-to-Module (c2m) Specification Proposal

For IEEE 802.3bs

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Purposes

- Propose a CDAUI-16 specification for c2c and c2m electrical interfaces in support the 400 GbE to fulfil its objective of:

  Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

Background and Motivation (I)

- 1st generation c2c and c2m electrical interfaces for 400GbE is likely CDAUI-16 (16x25.78 Gb/s) due to
  - Technical feasibility:
    - 25 - 28G and CAUI-4 serdes are widely available
    - CAUI-4 and CDAUI-16 performance is expected to be similar
    - Electrical characteristics (IL, xtalk) for a CDAUI-16 connector have been shown as about the same as CAUI-4[1]
    - CAUI-4 channel length has been shown to be good enough for the CDAUI-16[1]
  - Economic feasibility:
    - 25 - 28G and CAUI-4 serdes have been in production since 2012 from many FPGA/ASIC/ASSP/optical module vendors
    - Volume drives down the cost and power

Background and Motivation (II)

- Why 1st generation c2c and c2m interfaces for 400 GbE is unlikely to be CDAUI-8 (8x51.56 Gb/s)?
  - Technical feasibility:
    - 50 - 56 G and CDAUI-8 serdes are not available
    - It will take longer time to develop 50-56 G serdes technologies/products due to:
      - 50 - 56 G c2m serdes may be PAM4, not NRZ
      - 50 - 56 G c2c serdes will be PAM4, not NRZ
  - Economical feasibility:
    - Initial demand and volume for the 400 GbE is expected to be low, making it hard to justify the high-cost for new technology investments

Background and Motivation (III)

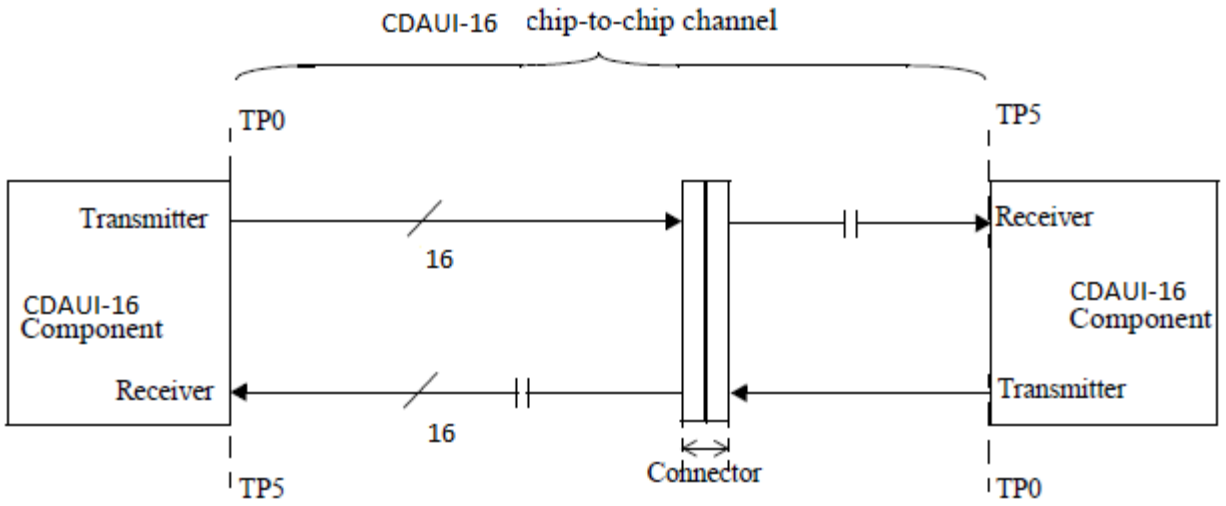
- There are three likely options for 802.3bs regarding CDAUI-n specification
  1) CDAUI-16 only
  2) Both CDAUI-16 and CDAUI-8
  3) CDAUI-8 only

  – Option 3 is not realistic due to the longer time to develop the new technology
  – For either option 1 or 2, we will need a spec for CDAUI-16, so we may as well go ahead and define one.

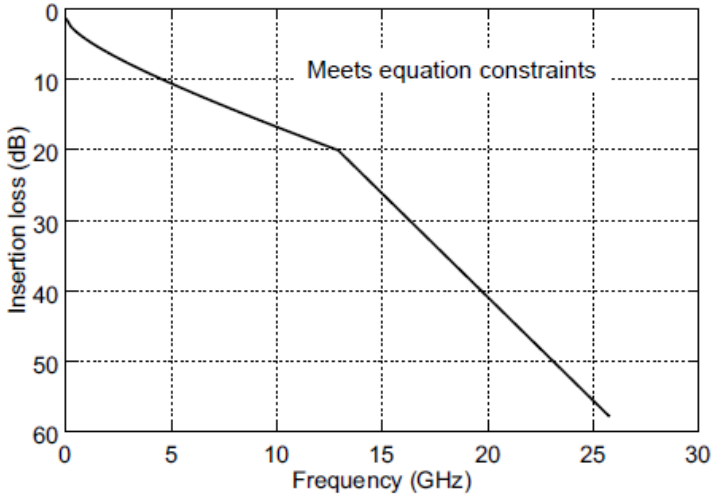
A Proposal for CDAUI-16 Spec: Reuse the CAUI-4 c2c and c2m Specifications

- CAUI-4 c2c and c2m can meet the CDAUI-16 serdes and channel requirements
- Reuse CAUI-4 serdes and channels, 4(x4) CAUI-4 or 1(x16) CDAUI-16 connector
  - Can be implemented as 4xCAUI-4 or “monolithic” CDAUI-16
  - Support 4x100G breakout easily
  - Enable fast time-to-market with low risk
  - Enable low initial development cost

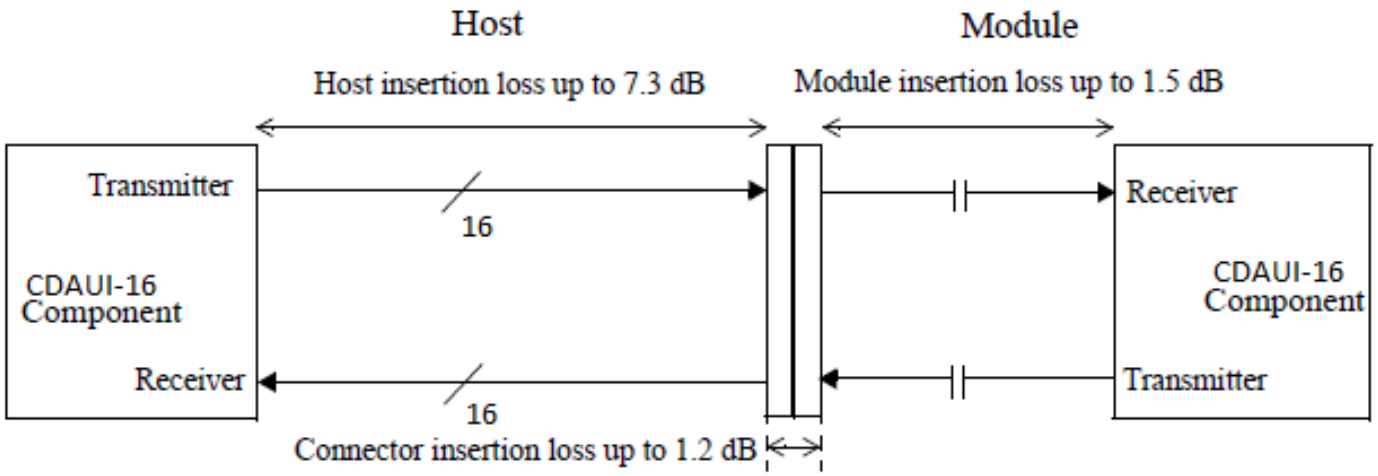
CDAUI-16 Link Topology I: c2c



Max IL



CDAUI-16 Link Topology II: c2m



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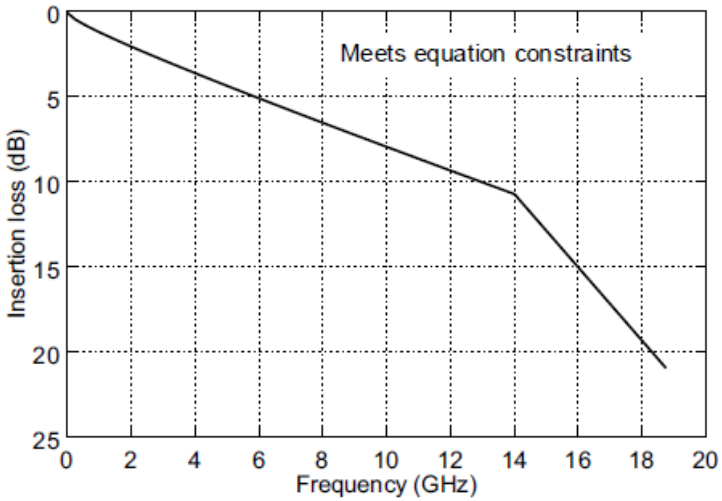

CDAUI-16 Meets 400GbE BER

- CDAUI-16 PMA interface will have < 1e-15 BER if it is not FEC protected and is with reuse and extension of CAUI-4 specification
  - However, if CDAUI-16 PMA is FEC protected (a likely scenario), then CAUI-4 specification could be relaxed when used to develop the CDAUI-16 specification
- 400 GbE requires a BER < 1e-13 at the MAC/PLS service interface (or equivalent FLR)
- CDAUI-16 will meet the 400 GbE BER objective

Summary

- CDAUI-16 as the 1st Gen 400 GbE c2c and c2m PMA bears good technical and economic merits
- CDAUI-16 specification can reuse existing CAUI-4 specification
  - Device and channel performance is expected to be similar between CDAUI-16 and CAUI-4
  - If CDAUI-16 is FEC protected, then the CAUI-4 spec could be relaxed when used to develop CDAUI-16
- CDAUI-16 meets the 400 GbE optional PMA definition objective
- CDAUI-16, with reuse of CAUI-4 specification, meets the 400 GbE BER objective

References

[1]:http://www.ieee802.org/3/bs/public/14_05/palkert_3bs_01_0514.pdf