CDAUI-8 50Gb/s Mezzanine Chip to Chip Channels

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TOC

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Motivation

- 400Gb/s using current SERDES rate (~25 Gbit/s per lane) implies CAUI-16 chip-to-module interface.
- The market would benefit from a reduced lane count interface, if it can work over a useful topology.
- For a sample set of channel constructions, what would it take to get 50 Gbit/s per lane?

PCB Finished Construction Terminology (just to help classify channels)

Dielectric[1]	Df@10GHz
Tier 5	0.003 ~0.005
Tier 4	0.005 ~0.007
Tier 3	0.007 ~0.01

[1]Gold Circuit Electronics - minten_01a_1111.pdf

PCB constructions 5 to 6.5mil trace widths used

Finished Copper Treatment Construction	
"Smooth"	IPC Very Low Profile (VLP) copper foil – Maximum roughness Rz < or = to 5.1 microns[2]
"Very Smooth"	IPC H-VLP to describe copper foil with maximum roughness Rz 2.0 to 2.5 microns.[2]
"Ultra Smooth"	Improved H-VLP Rz < 2 micron .. Idealized target

[2] http://www.pcbcarolina.com/images/Lake_High_Speed_Materials.pdf

Calculated Finished Trace Construction Loss at 85 degrees C and 85% Relative Humidity

- Ultra smooth Tier5 construction
  - Idealized PCB target goal
  - Micro strip - 0.86 dB/inch at 12.89GHz
    - pair to pair separation 8 times the dielectric height
  - Strip line – 0.63 dB/inch at 12.89GHz
    - pair to pair separation 4 times the dielectric height
- Very smooth Tier4 construction
  - These enhanced constructions are available today
  - Micro strip – 1.07 dB/inch at 12.89GHz
    - pair to pair separation 6 times the dielectric height
  - Strip line – 0.95 dB/inch at 12.89GHz
    - pair to pair separation 4 times the dielectric height
- Impedance tolerance set to +/-8 %
  - Can this be really delivered across manufacturing and environmental conditions?

Channel list: Thru, 3 NEXT, 4 FEXT

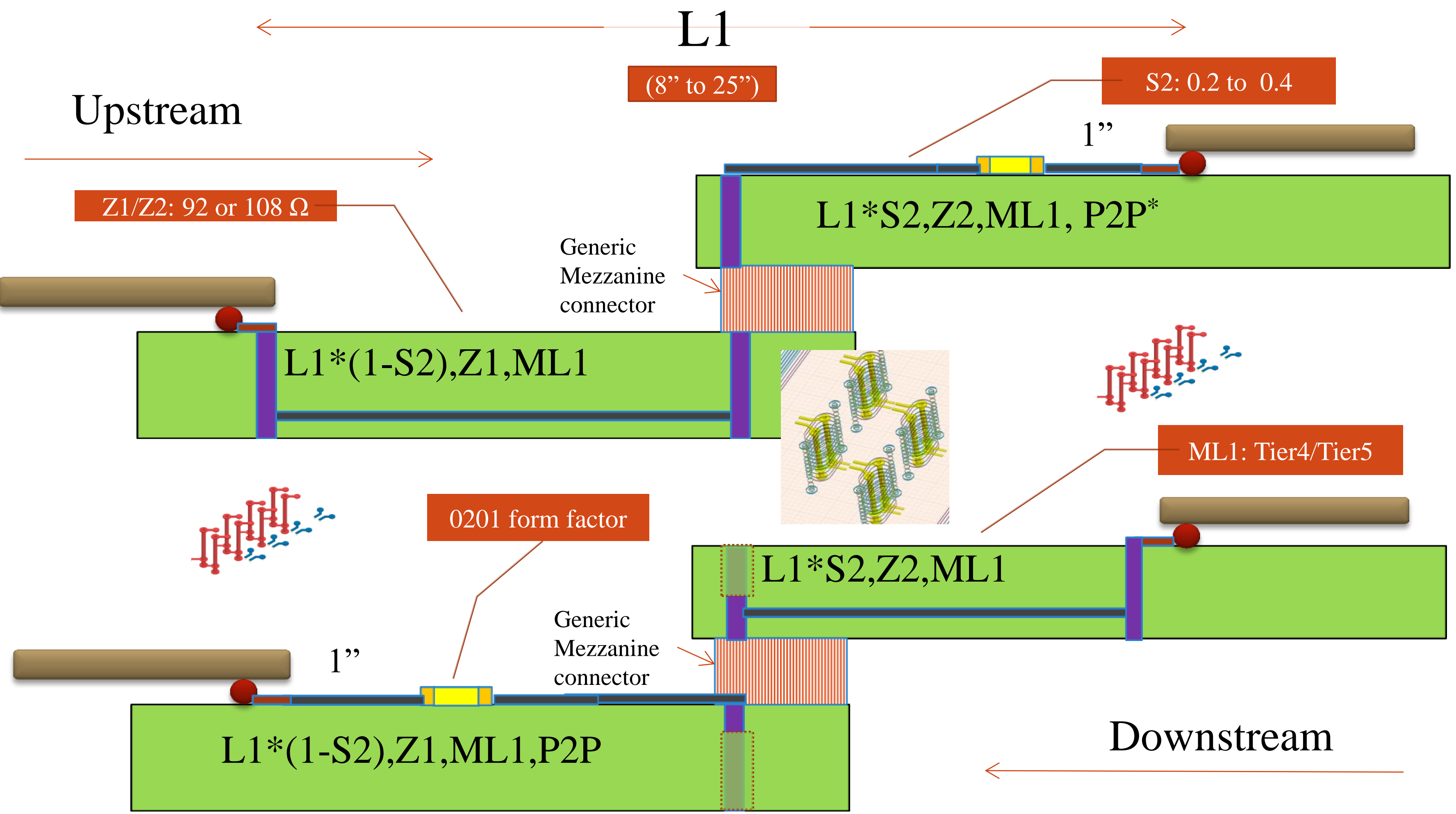
Idealized PCB target material

Channel	Length (in)	Copper	Dielectric
Case _000001	25	“Ultra Smooth”	Tier5
Case _000002	18	“Ultra Smooth”	Tier5
Case _000003	7	“Ultra Smooth”	Tier5
Case _000004	17	“Very Smooth”	Tier4
Case _000005	15	“Very Smooth”	Tier4
Case _000006	9	“Very Smooth”	Tier4
Case _000007	7	“Very Smooth”	Tier4

Similar to best ‘bj material

Chip to Chip One Connector (Mezzanine Topology)

108 MIL THICK 20 LAYER BOARDS WITH MAX OF 18 MIL VIA STUBS

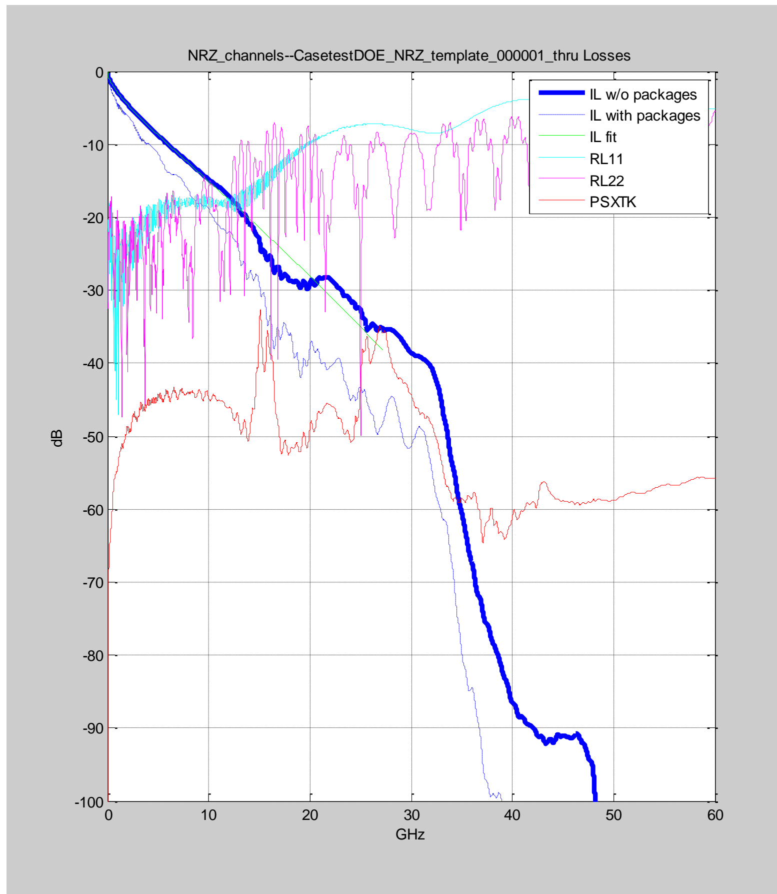


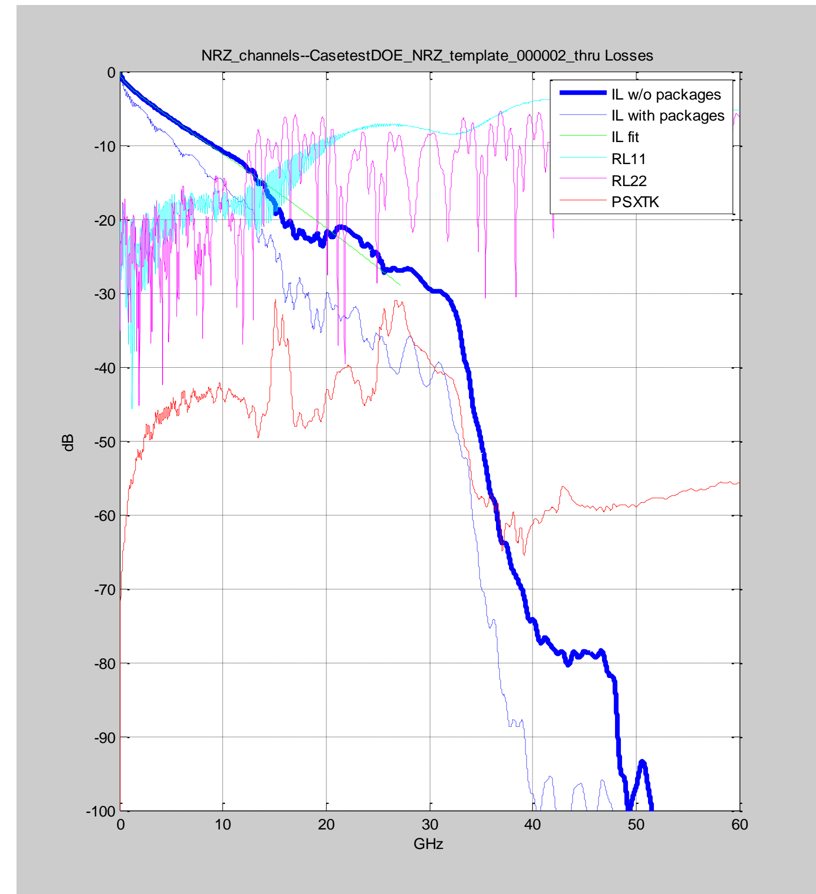
*LENGTH, IMPEDANCE, MATERIAL LOSS, PAIR TO PAIR SPACING IN RELATION TO DIELECTRIC HEIGHT)

More Channel Details

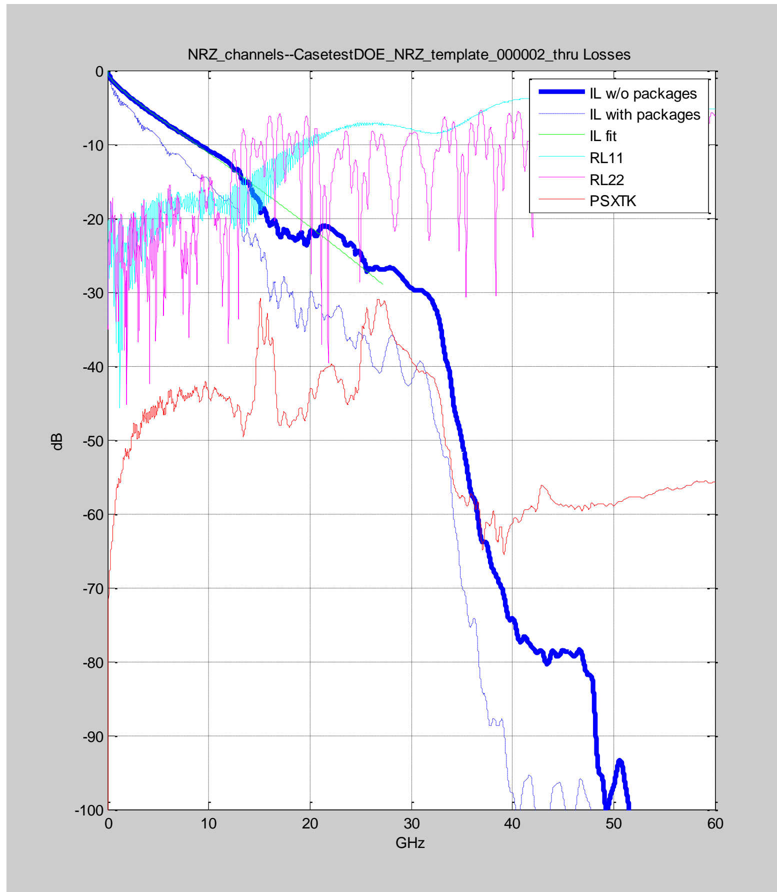
Channel	L1 (inches)	S2 (ratio)	ML1	Z1 (Ohms)	Z2 (Ohms)	P2P Spacing
Case 000001	25	0.2	Ultra Smooth Tier5	92	108	8
Case 000002	18	0.2	Ultra Smooth Tier5	92	108	8
Case 000003	7	0.33	Ultra Smooth Tier5	108	92	8
Case 000004	17	0.2	Smooth Tier4	92	108	6
Case 000005	15	0.33	Smooth Tier4	108	92	6
Case 000006	9	0.33	Smooth Tier4	108	92	6
Case 000007	7	0.33	Smooth Tier4	108	92	6

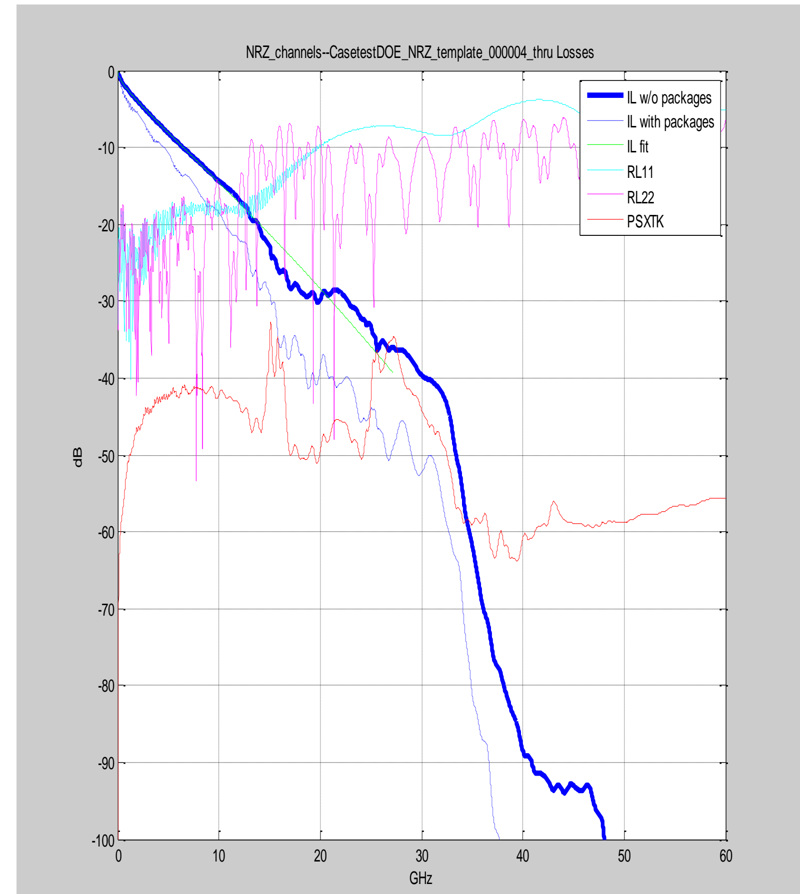
Case_000001, Case_000002



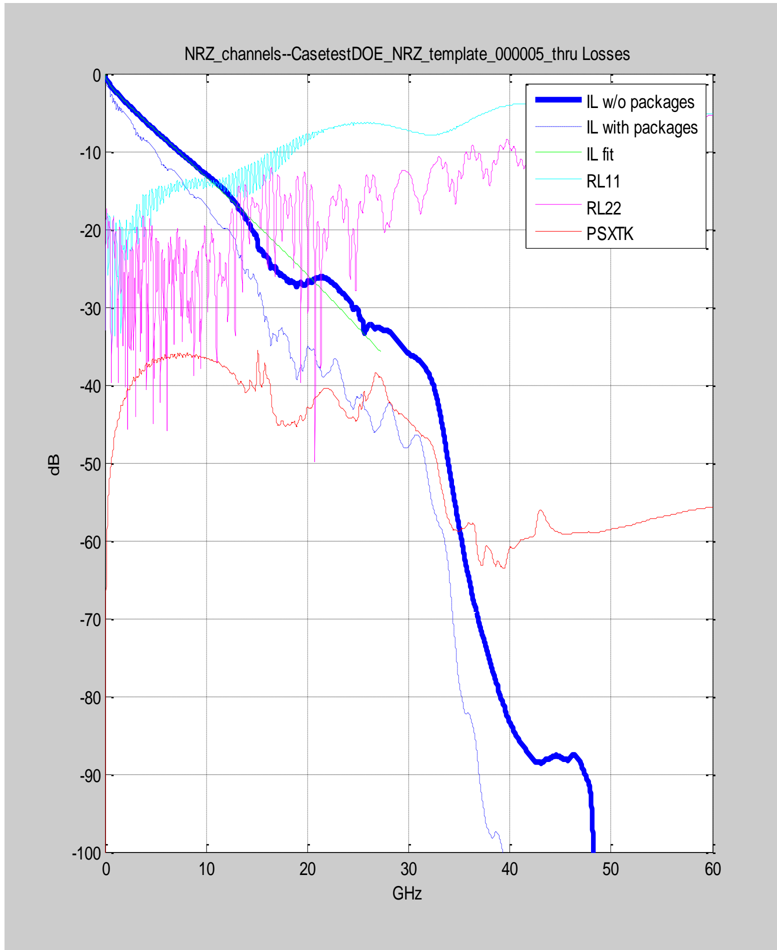


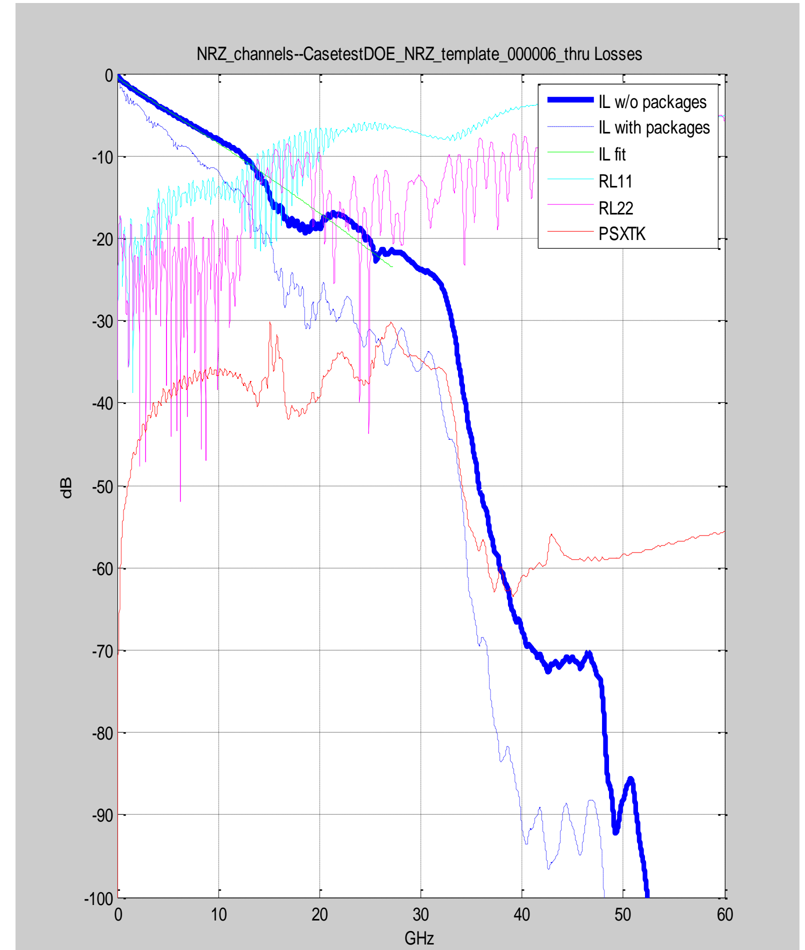
Case_000003, Case_000004



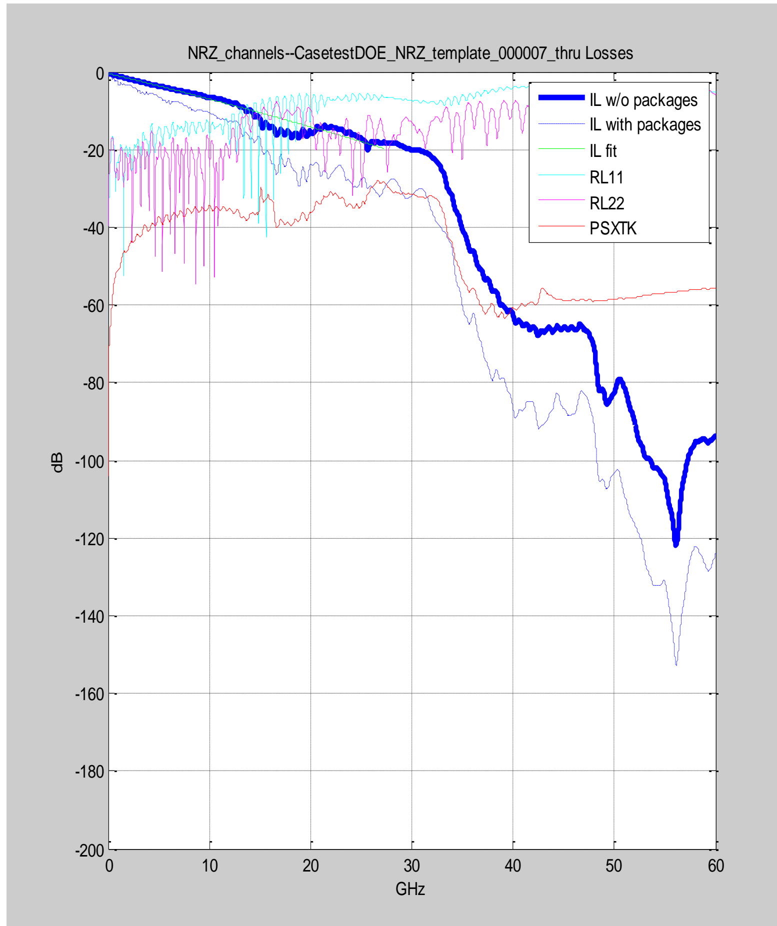


Case_000005, Case_000006





Case_000007



Minimum COM set at 4dB to Comprehend:

- DFE tap quantization
- CDR jitter
- Slicer sensitivity
- Power supply sensitivity
- DFE Taps sensitivities

Scaled jitter and low device loading do not seem sufficient

COM results with 'bj jitter

	FEC (DER 1e-4)	DER 1e-12	DER 1e-15
NRZ	Very Smooth Tier 4 One passing case Ultra Smooth Tier 5 no passing cases	COM <0dB	COM <0dB
PAM-4	Very Smooth Tier 4 No passing cases Ultra Smooth Tier 5 One passing case	COM <0dB	COM <0dB

COM parameters

- Scaled 'bj jitter
- SNR_Tx
  - 31dB PAM4
  - 27dB NRZ
- CLTE range
  - -20db to 0 dB
- C_d
  - 100 fF …!
  - This is very small
- Very sensitive to small layout channels
- Not really a good solution
- All channel pass CAUI-4

Very low jitter and low device load seems to offer hope for 50 Gb/s C2C signaling with FEC

COM results with low jitter

	FEC (DER 1e-4)	DER 1e-12	DER 1e-15
NRZ	Very Smooth Tier 4 Two cases passing Two cases falling Ultra Smooth Tier 5 One cases failing Two cases failing	COM <0dB	COM <0dB
PAM-4	Very Smooth Tier 4 Two cases passing Two cases failing, but marginal Ultra Smooth Tier 5 **All cases passing**	COM <0dB	COM <0dB

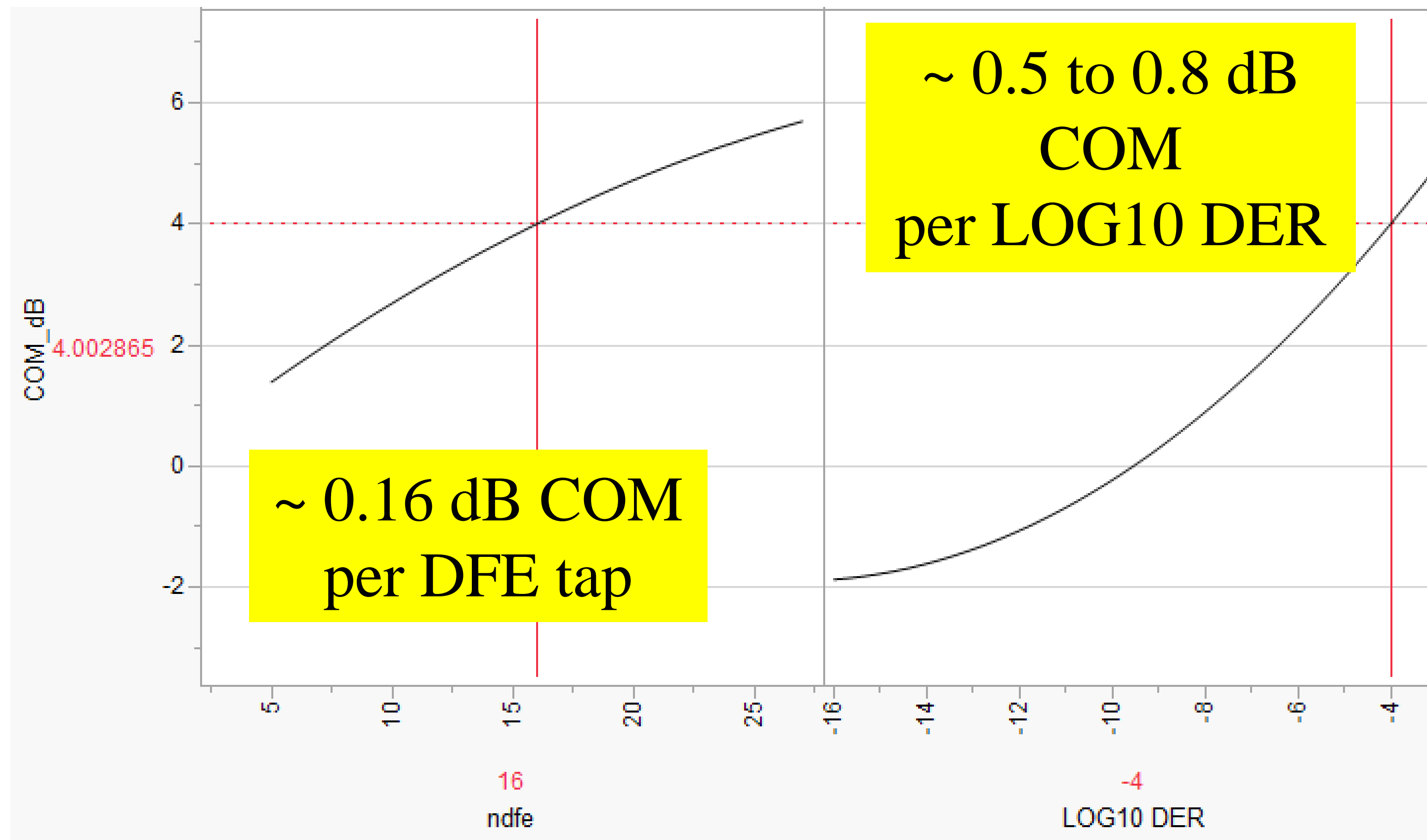
COM parameters

- PAM4 Jitter
  - Sigma_rj ~ 0.00125 UI or 46fs…!
  - A_dd ~ 0.00625 UI or 230fs …!
- NRZ jitter i
  - Sigma_rj ~ 0.0025 UI…!
  - A_dd ~ 0.0125 UI …!
- SNR_Tx
  - 31dB PAM4
  - 27dB NRZ
- CLTE range
  - -20db to 0 dB
- C_d
  - 100 fF …!
- Perhaps somewhat unrealistic

Results

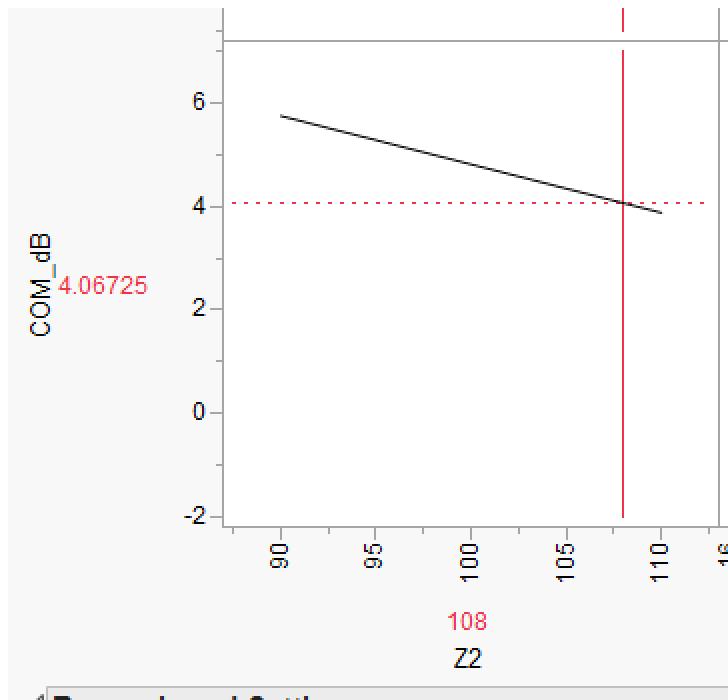
Channel	IL dB at 25.8GHz	IL dB @ 13.6GHz	COM dB NRZ low jitter	COM dB PAM4 low jitter	COM dB NRZ bj scaled jitter	COM dB PAM4 bj scaled jitter	COM dB CAUI-4	L1 (inches)	ML1
Case 000001	**35.31**	**19.64**	**1.92**	**4.50**	**1.47**	**3.39**	**2.01**	**25**	Ultra Smooth Tier5
Case 000002	**26.82**	**15.31**	**3.85**	**5.34**	**3.05**	**4.19**	**2.78**	**18**	Ultra Smooth Tier5
Case 000003	**14.95**	**7.86**	**4.71**	**4.67**	**3.96**	**3.90**	**3.06**	**7**	Ultra Smooth Tier5
Case 000004	**35.98**	**19.46**	**1.52**	**3.90**	**1.11**	**2.95**	**2.01**	**17**	Smooth Tier4
Case 000005	**32.82**	**17.81**	**3.01**	**3.70**	**2.40**	**2.82**	**2.18**	**15**	Smooth Tier4
Case 000006	**22.06**	**11.45**	**4.86**	**5.06**	**3.93**	**3.92**	**2.95**	**9**	Smooth Tier4
Case 000007	**19.28**	**9.80**	**4.87**	**4.64**	**4.04**	**3.77**	**3.02**	**7**	Smooth Tier4

Typical COM Sensitivity to log10 DER and number of DFE taps (ndfe)



Results obtained using Design of Experiment

Typical COM Sensitivity to Impedance Tolerance.



~ 0.2 dB COM per +/-% impedance tolerance

Results obtained using Design of Experiment

Summary

- FEC seems mandatory
- PAM or NRZ could be both be constrained to work
  - The managed channels provided do not fall off until around 30 GHz.
- A variety of channel lengths and constructions provided illustrate COM interaction for a somewhat typical chip to chip mezzanine design.

- Challenges
  - Determine realistic silicon specification improvements
    - Can we assume ultra-low jitter in the silicon?
    - Can we assume <100 fF of die pad load (across PVT)?
  - How much and what kinds of channel variation do we want to assume?
  - How much better PCB construction can be assumed?
    - We don’t have much room to improve materials.
- These challenges suggest the question:
  - Is 50 Gb/s per lane technically ready for a widely manufactured C2C marketplace?