Technical Feasibility of 56Gb/s NRZ Electrical Interface Signaling

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400G Considerations

- Extension of NRZ Coding to 56Gb/s?
- CEI-56G VSR, XSR, USR?
- 400G I/O density?
  - Dictates the module form factor and ASIC pin count
- 400G power concern?
  - I/O becomes dominant[1]

[1] http://www.ieee802.org/3/bs/public/14_05/ghiasi_3bs_01b_0514.pdf

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Transmitter Feasibility

- Transmitters have been built to operate up to 48-60Gb/s NRZ in 65nm CMOS[2,3]
- Broadcom has shown 49Gb/s NRZ transmitter with 2-tap de-emphasis fabricated in 40nm CMOS[4]
- Transmit equalization has been demonstrated by IBM at 64Gb/s NRZ LD for VCSEL[5]

[2] A. Hafez et al., "A 32-to-48Gb/s serializing transmitter using multiphase sampling in 65nm CMOS", *ISSCC Dig. Tech Papers,* pp. 36-37, Feb 2013.
[3] P. Chiang et al., "60Gb/s NRZ and PAM4 transmitters for 400GbE in 65nm CMOS", *ISSCC Dig. Tech Papers,* pp. 42-43, Feb 2014.
[4] B. Raghavan et al., "A Sub-2W 39.8-to-44.6Gb/s transmitter and receiver chipset with SFI-5.2 interface in 40nm CMOS", *ISSCC Dig. Tech Papers,* pp. 32-33, Feb 2013.
[5] D. Kuchta et al., "64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL", in *Optical Fiber Communication Conference*, OSA Technical Digest (online) (Optical Society of America, 2014), paper Th3C.2.

Receiver Feasibility

- Broadcom demonstrated a receiver with amplifiers with 30GHz bandwidth, 35dB gain, and 8dB peaking fabricated in 40nm CMOS. BER<1e-12 was achieved for 20dB loss channel at 44.6Gb/s[5]
- A 3-tap Decision-feedback equalizer (DFE) was shown possible to operate at 66Gb/s using 65nm CMOS[6]
- Fujitsu announced a DFE-based receiver capable of 56Gb/s operation for CPU I/O and module applications[7]

[5] D. Kuchta et al., "64Gb/s Transmission over 57m MMF using an NRZ Modulated 850nm VCSEL", in *Optical Fiber Communication Conference*, OSA Technical Digest (online) (Optical Society of America, 2014), paper Th3C.2.

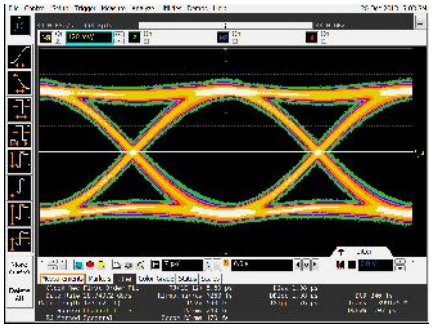
[6] Y. Lu, and E. Alon, "A 66Gb/s 46mW 3-Tap Decision_feedback Equalizer in 65nm CMOS", *ISSCC Dig. Tech Papers,* pp. 30-31, Feb 2013.

[7] http://www.fujitsu.com/global/about/resources/news/press-releases/2014/0613-01.html

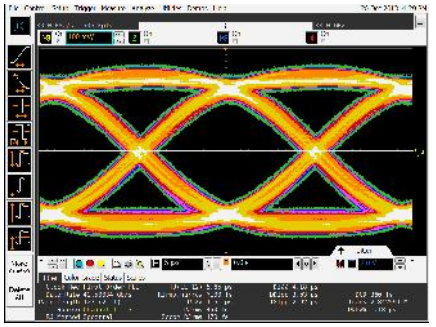
Credo SerDes Proven in Silicon

- 28Gb/s (65nm)
  - >25dB loss handling
  - In production qualification
- 28Gb/s SerDes (40nm)
  - >35dB loss handling
- 28Gb/s SerDes (40nm)
  - >20dB loss handling with low power
- 50Gb/s NRZ SerDes (40nm)
  - >30dB loss handling
  - Operates up to 55Gb/s

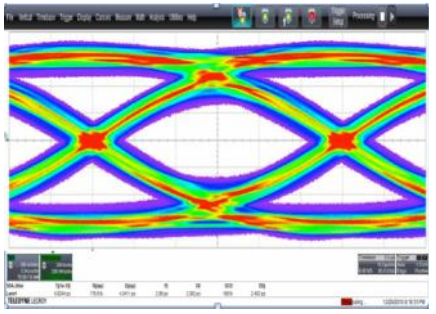
28G



42.5G



50G



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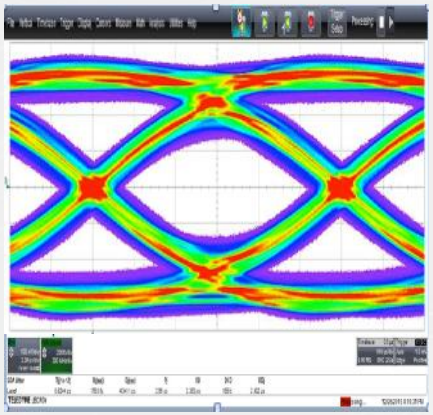
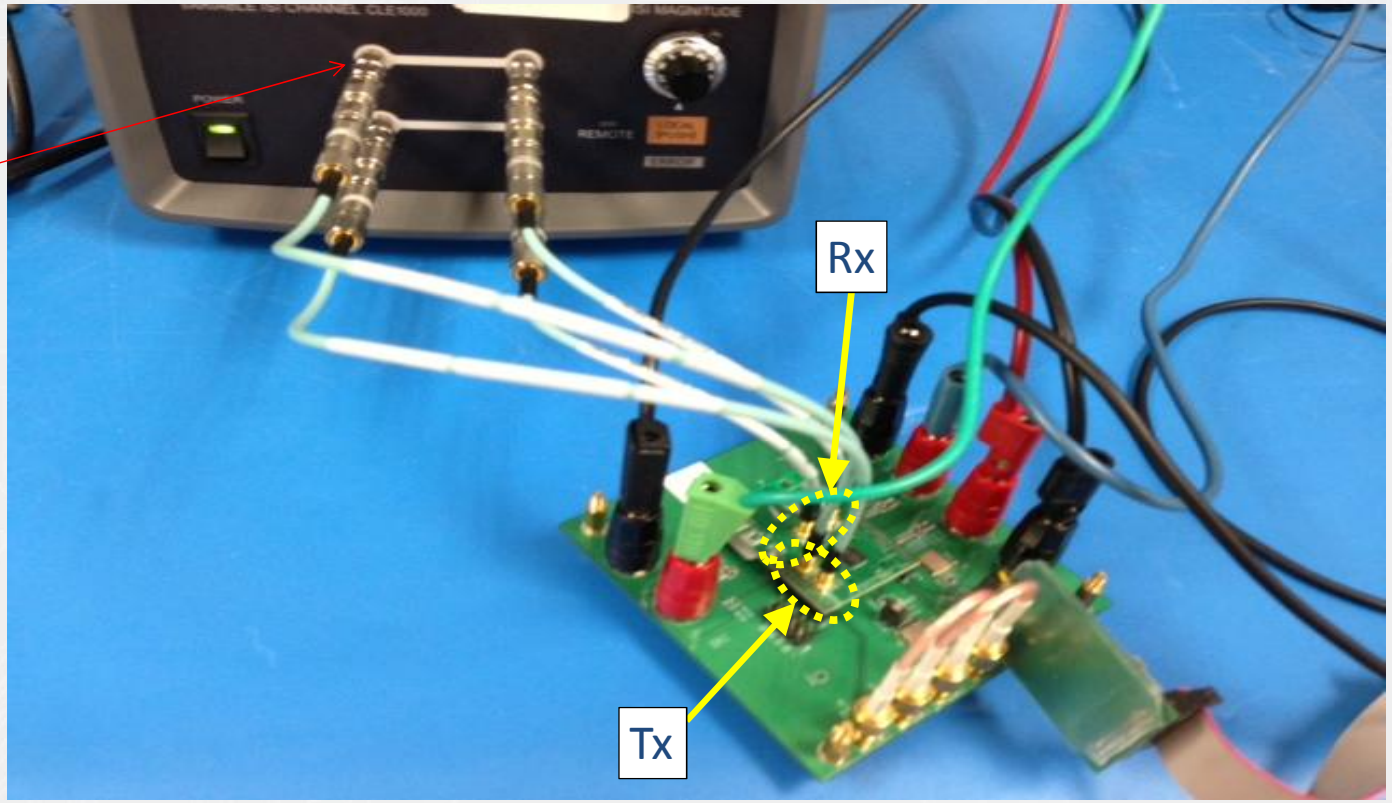
50Gb/s Test Setup



Tx eye after cable



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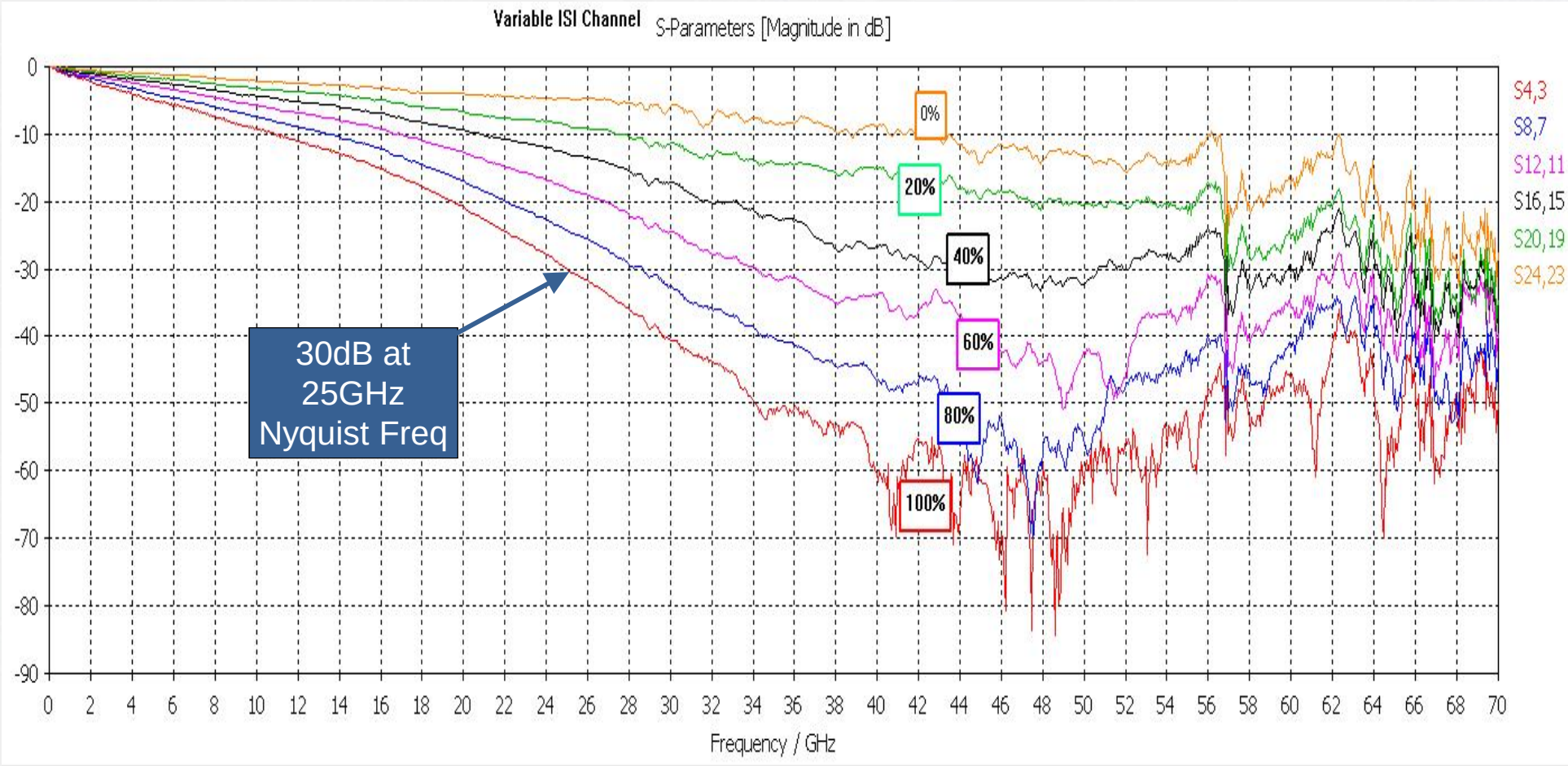
50Gb/s Channel Loss

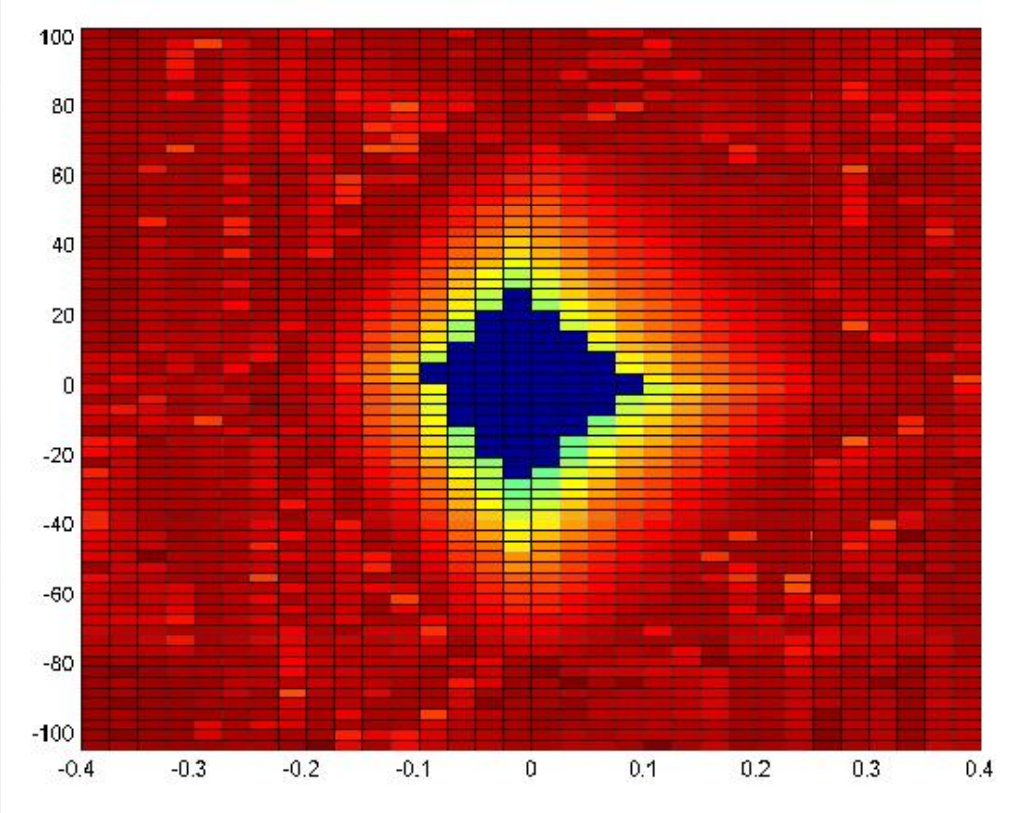


Artek variable ISI channel CLE1000-H1 at 100% attenuation

50Gb/s 40nm Silicon Results

- 3-tap TX equalization
- >20dB CTLE
- Multi-tap DFE
- >30dB loss handling

Rx internal eye margin after 30dB channel , CTLE and DFE



Reliable path to 56Gb/s in 28nm, 16nm, …

- Scalable receiver architecture
  - Completed porting from 40nm to 28nm in 3 months
  - 16FF+ PDK received, design port target in 4 months
- Efficient process power scaling
  - 16FF+ vs 28nm: 30-40%
  - < 175mW per transceiver at 56Gb/s in 16FF+
    (reference point: 75mW per 28G transceiver in 40nm)

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Summary

- 56Gb/s NRZ is feasible and advantageous for 400GE
  - CEI-56G VSR, XSR, USR can all be met with margin (30dB+ proven in silicon at 50Gb/s in 40nm)
  - Power efficient for next generation switch chip designs (<175mW/ch)
  - Provides placement flexibility for OE and backplane drivers

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