25 Gb/s and 50 Gb/s Electrical Interface
Consensus Building

IEEE 802.3bs 400Gb/s Ethernet
September 2014 version r4
Overview

Quick Note

A Process - Simple Steps Forward

Looking at Implementations

Working towards possible adoptions

Steps to November
Quick Note: This is a Consensus Building Meeting

This was reviewed at each meeting:

Not an official IEEE meeting

Build Consensus towards a presentation or adoption covering interface type, rate, modulation, and loss

Offer lots of constructive comments to converge quickly

Please mute your phone

Requested Presentation Time for September

Requested Evening Time for Further Discussion

Supporters Appreciated / Attendees will be listed

There are some things discussed that are outside the scope of the project, but are necessary to complete the system level discussion and drive the best Electrical Interface possible.
Goals for this Presentation

Reviewing 3 meetings worth of thoughts and conversations towards building consensus

Is there anything we can propose / adopt at the interim?
The Process Steps

The following simplified process steps are used to build consensus:

- Defining / Discussing Reach
- System Architecture
- Channel Loss – the first crack at it because one needs an egg to get to the chicken
- Modulation
- Equalization
- Error Correction
- Power
Attendees
People Who Requested to Attend

<table>
<thead>
<tr>
<th>Peter</th>
<th>Anslow</th>
<th>Ciena</th>
<th>Yasuo</th>
<th>Hidaka</th>
<th>Fujitsu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vittal</td>
<td>Balasubramani</td>
<td>Dell</td>
<td>Sammy</td>
<td>Hindi</td>
<td>Juniper</td>
</tr>
<tr>
<td>Arash</td>
<td>Behziz</td>
<td>TE</td>
<td>Kiyohisa</td>
<td>Hiramoto</td>
<td>Oclaro</td>
</tr>
<tr>
<td>Liav</td>
<td>Ben Artsi</td>
<td>Marvell</td>
<td>Scott</td>
<td>Irwin</td>
<td></td>
</tr>
<tr>
<td>Bill</td>
<td>Brennan</td>
<td>Credo</td>
<td>Elizabeth</td>
<td>Kochuparambil</td>
<td></td>
</tr>
<tr>
<td>David</td>
<td>Brown</td>
<td>Semtech</td>
<td>Paul</td>
<td>Kolesar</td>
<td>Cisco</td>
</tr>
<tr>
<td>Matt</td>
<td>Brown</td>
<td>APM</td>
<td>Ryan</td>
<td>Latchman</td>
<td>CommScope</td>
</tr>
<tr>
<td>derek</td>
<td>Cassidy</td>
<td>BT</td>
<td>David</td>
<td>Lewis</td>
<td>Macom</td>
</tr>
<tr>
<td>Chris</td>
<td>Cole</td>
<td>Finisar</td>
<td>Jeffery</td>
<td>Maki</td>
<td>JDSU</td>
</tr>
<tr>
<td>John</td>
<td>DAmbrosia</td>
<td>Dell</td>
<td>Yonatan</td>
<td>Malkiman</td>
<td>Juniper</td>
</tr>
<tr>
<td>Piers</td>
<td>Dawe</td>
<td>Mellanox</td>
<td>Rich</td>
<td>Meltz</td>
<td>Mellanox</td>
</tr>
<tr>
<td>Chris</td>
<td>Diminico</td>
<td>Broadcom</td>
<td>Andy</td>
<td>Moorwood</td>
<td>Intel</td>
</tr>
<tr>
<td>Yuval</td>
<td>Domb</td>
<td>Qlogic</td>
<td>Gary</td>
<td>Nicholl</td>
<td>Infinera</td>
</tr>
<tr>
<td>Mike</td>
<td>Dudek</td>
<td>IBM</td>
<td>Takeshi</td>
<td>Nishimura</td>
<td>Cisco</td>
</tr>
<tr>
<td>John</td>
<td>Ewen</td>
<td>Semtech</td>
<td>David</td>
<td>Ofelt</td>
<td>YEU</td>
</tr>
<tr>
<td>Edward</td>
<td>Frlan</td>
<td>Clariphy</td>
<td>Vasudevan</td>
<td>Parthasarathy</td>
<td>Juniper</td>
</tr>
<tr>
<td>Mike</td>
<td>Furlong</td>
<td>Xilinx</td>
<td>Scott</td>
<td>Powell</td>
<td>BroadCom</td>
</tr>
<tr>
<td>Ali</td>
<td>Ghiasi</td>
<td>Avagotech</td>
<td>Haoli</td>
<td>Qian</td>
<td>ClariPhy</td>
</tr>
<tr>
<td>Mark</td>
<td>Gustlin</td>
<td>TE</td>
<td>Rick</td>
<td>Rabinovich</td>
<td>Credo</td>
</tr>
<tr>
<td>Adam</td>
<td>Healey</td>
<td></td>
<td>Vineet</td>
<td>Salunke</td>
<td>ALU</td>
</tr>
<tr>
<td>David</td>
<td>Helster</td>
<td></td>
<td>Omer</td>
<td>Sella</td>
<td>Cisco</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Mellanox</td>
</tr>
</tbody>
</table>
## Attendees By Meeting

<table>
<thead>
<tr>
<th>Date</th>
<th>Attendees</th>
</tr>
</thead>
<tbody>
<tr>
<td>8/27/2014</td>
<td>Adam Healey, Ali Ghiasi, Andy Moorwood, Beth Kochuparambil, Chris Cole,</td>
</tr>
<tr>
<td></td>
<td>Dave Brown, David Ofelt, Gary Nicholl, Jeff Twombly, Jeff Maki, Joel Goergen, Liav Ben-Artsi, Megha Shanbhag, Matt Brown, Megha Shanbhag, Mike Dudek, Nathan Tracy, Piers Dawe, Pirooz Tooyserkani, Rich Melitz, Rick Rabinovich, Scott Irwin, Tony Zorke, Vasu Parthasarathy, Vittal Balasubramanian, Vivek Telang, Xinyuan Wang, Yuval Hidaka, Yuval Domb</td>
</tr>
</tbody>
</table>
| 8/20/2014      | Alan Tipper, Ali Ghiasi, Andy Zambell, Chris Cole, Dave Brown, Derek Cassidy,  
|                | Ali Ghiasi, Yuval Domb, Arash Behziz, Beth Kochuparambil, John Ewen, Joe Laroche, Jeff Maki, Joel Goergen, Liav Ben-Artsi, Matt Brown, Mark Gustlin, Mark Gustlin, Mike Dudek, Nathan Tracy, Piers Dawe, Pirooz Tooyserkani, Rich Melitz, Scott Irwin, Tony Zorke, Tony Zorke, Vasu Parthasarathy, Vittal Balasubramanian, Vivek Telang, Xinyuan Wang, Yuval Hidaka |
| 8/13/2014      | Adam Healey, Tony Zorke, Ali Ghiasi, Vasu Parthasarathy, Andy Moorwood,  
|                | Andy Zambell, Chris Cole, Dave Brown, Derek Cassidy,  
|                | Ed Frlan, Gary Nicholl, Jeff Maki, Joel Goergen, Liav Ben-Artsi, Matt Brown, Mark Gustlin, Mike Dudek, Nathan Tracy, Oded Wertheim, Omer Sella, Peter Anslow, Piers Dawe, Pirooz Tooyserkani, Rich Melitz, Rick Rabinovich, Scott Irwin, Tony Zorke, Tony Zorke, Vasu Parthasarathy, Vittal Balasubramanian, Vivek Telang, Xinyuan Wang, Yuval Hidaka |

Note: The list of attendees may be incomplete due to space constraints.
Thank You

3 meetings – over 5 hours of courteous technical conversation.

54 people volunteering what time they could free up.
<table>
<thead>
<tr>
<th>Name</th>
<th>First Name</th>
<th>Company</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vittal</td>
<td>Balasubramani</td>
<td>Dell</td>
</tr>
<tr>
<td>David</td>
<td>Brown</td>
<td>Semtech</td>
</tr>
<tr>
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<td>Finisar</td>
</tr>
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<td>Edward</td>
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<td>Semtech</td>
</tr>
<tr>
<td>Ali</td>
<td>Ghiasi</td>
<td>Ghiasi Quantum</td>
</tr>
<tr>
<td>Paul</td>
<td>Kolesar</td>
<td>Commscope</td>
</tr>
<tr>
<td>Ryan</td>
<td>Latchman</td>
<td>Macom</td>
</tr>
<tr>
<td>Jeffery</td>
<td>Maki</td>
<td>Juniper</td>
</tr>
<tr>
<td>Andy</td>
<td>Moorwood</td>
<td>Infinera</td>
</tr>
<tr>
<td>Gary</td>
<td>Nicholl</td>
<td>Cisco</td>
</tr>
<tr>
<td>Rick</td>
<td>Rabinovich</td>
<td>ALU</td>
</tr>
<tr>
<td>Megha</td>
<td>Shanbhag</td>
<td>TE</td>
</tr>
<tr>
<td>Nathan</td>
<td>Tracy</td>
<td>TE</td>
</tr>
<tr>
<td>Andrew</td>
<td>Zambell</td>
<td>FCI</td>
</tr>
</tbody>
</table>
Clarifying Reach Definitions
- Used to define 25Gb/s Interfaces Reaches
- Projecting Forward to 50Gb/s Interfaces
## Length, Loss & Applications

<table>
<thead>
<tr>
<th>Length</th>
<th>Loss</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10mm/0.4in</td>
<td>1.5dB@14GHz</td>
<td>Bump-to-bump Inside MCM or 3D Stack</td>
</tr>
<tr>
<td>&lt; 50mm/2.0in</td>
<td>4dB@14GHz</td>
<td>Ball-to-ball Across PCB</td>
</tr>
<tr>
<td>&lt; 200mm/7.9in</td>
<td>10dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>&lt; 500mm/19.7in</td>
<td>20dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>&lt; 1000mm/39.4in</td>
<td>35dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
</tbody>
</table>
**Length, Loss & Applications:**
Today a single 25Gb/s SERDES core can cover all these ranges.

<table>
<thead>
<tr>
<th>Range</th>
<th>Loss Parameters</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10mm/0.4in</td>
<td>USR 1.5dB@14GHz</td>
<td>Bump-to-bump Inside MCM or 3D Stack</td>
</tr>
<tr>
<td>&lt; 50mm/2.0in</td>
<td>XSR 4dB@14GHz</td>
<td>Ball-to-ball Across PCB</td>
</tr>
<tr>
<td>&lt; 200mm/7.9in</td>
<td>VSR 10dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>&lt; 500mm/19.7in</td>
<td>MR 20dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>&lt; 1000mm/39.4in</td>
<td>LR 35dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
</tbody>
</table>

These ranges can be easily covered with one SERDES core today for 25Gb/s.
### Length, Loss & Applications: Grouping (Perspective 1)

How does a 50Gb/s SERDES core cover these ranges optimally?

<table>
<thead>
<tr>
<th>Distance</th>
<th>IL</th>
<th>Loss @ 14GHz</th>
<th>Loss @ 28GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>USR &lt; 10mm/0.4in</td>
<td>1.5dB@14GHz</td>
<td>3dB@28GHz</td>
<td>Bump-to-bump Inside MCM or 3D Stack</td>
</tr>
<tr>
<td>XSR &lt; 50mm/2.0in</td>
<td>4dB@14GHz</td>
<td>8dB@28GHz</td>
<td>Ball-to-ball Across PCB</td>
</tr>
<tr>
<td>VSR &lt; 200mm/7.9in</td>
<td>10dB@14GHz</td>
<td>20dB@28GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>MR &lt; 500mm/19.7in</td>
<td>20dB@14GHz</td>
<td>40dB@28GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>LR &lt; 1000mm/39.4in</td>
<td>35dB@14GHz</td>
<td>Ball-to-ball</td>
<td></td>
</tr>
</tbody>
</table>

Unconfirmed but … Under the impression from the group the cores should be compatible
### Length, Loss & Applications: Grouping (Perspective 2)

How does a 50Gb/s SERDES core cover these ranges optimally?

<table>
<thead>
<tr>
<th>Distance</th>
<th>Loss</th>
<th>Core Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10mm/0.4in</td>
<td>1.5dB@14GHz, 3dB@28GHz</td>
<td>USR</td>
</tr>
<tr>
<td>&lt; 50mm/2.0in</td>
<td>4dB@14GHz, 8dB@28GHz</td>
<td>XSR (C2EO)</td>
</tr>
<tr>
<td>&lt; 200mm/7.9in</td>
<td>10dB@14GHz, 20dB@28GHz</td>
<td>VSR (C2M)</td>
</tr>
<tr>
<td>&lt; 500mm/19.7in</td>
<td>20dB@14GHz, 40dB@28GHz</td>
<td>MR (C2C)</td>
</tr>
<tr>
<td>&lt; 1000mm/39.4in</td>
<td>35dB@14GHz</td>
<td>LR (C2F)</td>
</tr>
</tbody>
</table>

Unconfirmed but … Under the impression from the group the cores should be compatible.
**Length, Loss & Applications:**
Future: a single 50GB/s SERDES core to cover all these ranges

<table>
<thead>
<tr>
<th>IL</th>
<th>USR</th>
<th>&lt; 10mm/0.4in</th>
<th>1.5dB@14GHz 3dB@28GHz</th>
<th>Bump-to-bump Inside MCM or 3D Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>XSR</td>
<td>&lt; 50mm/2.0in</td>
<td>4dB@14GHz 8dB@28GHz</td>
<td>Ball-to-ball Across PCB</td>
</tr>
<tr>
<td>VSR</td>
<td>C2EO</td>
<td>&lt; 200mm/7.9in</td>
<td>10dB@14GHz 20dB@28GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>MR</td>
<td>C2M</td>
<td>&lt; 500mm/19.7in</td>
<td>20dB@14GHz 40dB@28GHz</td>
<td>Ball-to-ball</td>
</tr>
<tr>
<td>LR</td>
<td>C2F</td>
<td>&lt; 1000mm/39.4in</td>
<td>35dB@14GHz</td>
<td>Ball-to-ball</td>
</tr>
</tbody>
</table>

These ranges should be covered with one SERDES core in the future for 50Gb/s.
Length, Loss & Application: Technologies for 50Gb/s

<table>
<thead>
<tr>
<th>Application</th>
<th>Length</th>
<th>Loss</th>
<th>Modulation</th>
<th>pJ/bit</th>
<th>DFE?</th>
<th>FEC?</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2EO (XSR)</td>
<td>&lt; 2in</td>
<td>&lt;4dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&lt;8dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>C2M (VSR)</td>
<td>2-8in</td>
<td>4-10dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-20dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>C2C (MR)</td>
<td>8-20in</td>
<td>10-20dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20-40dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>

These Values are under discussion

Knowing the reach definition allows us to begin understanding the next steps in the consensus building process:

- System Architecture
- Channel Loss
- Modulation
- Equalization
- Error Correction
- Power
Looking At System Architecture
The Early Adopter Option

Fabric

PPU /NPU

Optic Module

C2C
C2F

Early Adopter 25G NRZ building blocks

Something to work on for another project

0

x

Mux Handles conversion from what to what

C2M
C2C

C2EO

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

Possible Re-Timer between here

0

15

8

16 by 25G
8 by 50G
4 by 100G

What??

PPU /NPU

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

25G NRZ

40G/50G PAM4

40G/50G PAM4

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The Advanced Early Adopter Option

Fabric

PPU /NPU

Optic Module

C2C
C2F

C2M
C2C

C2EO

Something to work on for another project

Early Adopter 25G NRZ / 50G ??? building block

Early Adopter 25G NRZ building block

Mux
Handles conversion from what to what

Possible Re-Timer between here

Fabric

Optic Module

16 by 25G
8 by 50G
4 by 100G

Something to work on for another project

Early Adopter 25G NRZ / 50G ??? building block

Early Adopter 25G NRZ building block

C2C C2F

C2M C2C
The Evolved Option

Fabric

PPU /NPU

Optic Module

C2C C2F

C2M C2C

C2EO

C2EO

Possible Re-Timer between here

What??

50G ???

50G ???

50G ???

50G ???

0

0

7

Something to work on for another project

Early Adopter 25G NRZ / 50G ???

building block

50G ???

building block

Mux Handles conversion from what to what

16 by 25G

8 by 50G

4 by 100G

16 by 25G

8 by 50G

4 by 100G

25G NRZ

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

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40G/50G PAM4

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40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4

25G NRZ

50G ???

40G/50G PAM4
The Maybe-Some-day Option

PPU/NPU DIE

- 100G
- 25G NRZ 40G/50G PAM4
- 100G
- 25G NRZ 40G/50G PAM4
- 100G

Fabric

C2C C2F

Optic DIE

- What??
- What??

25G NRZ 40G/50G PAM4

C2EO

0

3

0

x

Something to work on for another project

100G “what” building block

4 by 100G

4 by 100G
Some Thoughts

Need to continue to converge these options with work Mark Gustlin and team are addressing.
Looking at Channel Implementations For 50Gb/s
Chip-to-Embedded Optics (C2EO)

Possible Implementations
- System in package (SiP)
- 2.5D/3D Silicon interposer
- Stacked die
- Multi-chip module
- Package-on-package

Offers system advantage/flexibility for routing and architecture.

Discussions still needed to have:
Reasonable to see C2EO interfaces commonly in industry by ____
Die-to-Die definition (instead of ball to ball)?
Can this be defined in the standards or are these proprietary links?
No leap changes in this market from 100G Ethernet; albeit incremental changes have are seen (materials, connectors, quality, system constraints, etc.)

**Module Route**: 0.5”-2”

**Host Route**: 1-4” (up to 7” with low loss techniques)

Ball-to-ball definition (ball meaning BGA on the outside of the package)?

* Looking across the industry, across multiple platforms... typical channel length ranges shown.
Chip-to-Module (C2M) – What does that mean for loss?

Notes:
(lhs) Uses DkDf_AlgebraicModel_v2.05. Where loss is calculated using an algebraic model for dielectric, conductor, and connector loss.

(lhs) The 4” host trace is and should be supported at mid-loss materials by 100G standards... 7” is certainly seen in designs, but industries seem to recognize and adjust with material and design tradeoffs.
Chip-to-Module (C2M) – Comparing channel data

Notes:
- TE Channels developed using HFSS/ADS modeling tools.
- The 4” host trace is and should be supported at mid-loss materials by 100G standards... 7” is certainly seen in designs, but industries seem to recognize and adjust with material and design tradeoffs.

Propose: Use extended CAUI4 C2M–like channels for Modulation discussion/comparison
Chip-to-Chip (C2C)

- No leap changes in this market from 100G Ethernet; albeit incremental changes have are seen (materials, connectors, quality, system constraints, etc.)

- However, there is a push in industry to longer links... while making design tradeoffs

- How far should C2C cover? Let’s look at loss!

*originally from Rabinovich_01_0513
Notes:

← Uses DkDf_AlgebraicModel_v2.05. Where loss is calculated using an algebraic model for dielectric, conductor, and connector loss.

← The typical routes seem to be covered by 20dB at 12.87G... The longer links that industry stretches to reach are not.
Chip-to-Chip (C2C) – What does that mean for loss?

Notes:

- Uses DkDf_AlgebraicModel_v2.05. Where loss is calculated using an algebraic model for dielectric, conductor, and connector loss.

- The typical routes seem to be covered by 20dB at 12.87G... The longer links that industry stretches to reach are not.

- Do we stay with the current CAUI4 coverage or should we cover more channels now seeing industry’s range of implementation??
Chip-to-Chip (C2C) – Let’s compare to channel data.

Notes:

← Channels are public on the .3bs webpage... all channels include connector and an 8% impedance variation from motherboard to daughtercard.

← Are these channels right to use for modulation discussion?

← Is ILD pessimistic for educated 50G channel design?
Chip-to-Fabric (C2F – previously Backplane)

Used for channels too long for C2C, but comes with a power/complexity penalty.

Pure loss is becoming a constricting factor for C2F designs (25-35dB of 100G standards generation). Backplanes are becoming more and more diverse

- Typical FR4 backplane
- Planned repeaters
- Cable backplane
- Mezzanine connectors
- Optics backplane

Out of scope for current project, but good to note as it is part of electrical infrastructure.
Equations plotted for C2C and C2M

802.3bm draft – C2M equation (red curve)

\[
\text{Insertion\_loss}(f) \leq \begin{cases} 
1.076(0.075 + 0.537\sqrt{f} + 0.566f) & 0.01 \leq f < 14 \\
1.076(-18 + 2f) & 14 \leq f < 18.75 
\end{cases} \quad (\text{dB}) \quad (83E-1)
\]

802.3bm draft – c2C equation (red curve) *although, standard uses COM as the normative spec, the following is offered as the informative “limit” line

\[
\text{Insertion\_loss}(f) \leq \begin{cases} 
1.083 + 2.543.\sqrt{f} + 0.761f & 0.01 \leq f < 12.89 \\
-17.851 + 2.936f & 12.89 \leq f < 25.78 
\end{cases} \quad (\text{dB}) \quad (83D-1)
\]

C2M and C2C “extended curve” (blue curves)

Simply extend first portion of above curves for full frequency range; omit 14-18.75G and 12.89-25.78G equations, respectively.

Suggested/modified curve drawn in C2C (green curve)

\[
0.9 + 2.1\sqrt{f} + 1.17f
\]
Starting the Modulation Discussion For 50Gb/s
Does filling out this chart help us close modulation discussions? Yes
Do you want to see companies provide details? Yes
Should we add a column on silicon technology?

<table>
<thead>
<tr>
<th>Application</th>
<th>Length</th>
<th>Loss</th>
<th>Modulation</th>
<th>pJ/bit</th>
<th>DFE?</th>
<th>FEC?</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2EO (XSR)</td>
<td>&lt; 2in</td>
<td>&lt;4dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>&lt;8dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>C2M (VSR)</td>
<td>2-8in</td>
<td>4-10dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-20dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>C2C (MR)</td>
<td>8-20in</td>
<td>10-20dB@14GHz</td>
<td>PAM-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20-40dB@28GHz</td>
<td>NRZ</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>
Next Steps to Consensus

IEEE 802.3bs 400Gb/s Ethernet
Between Now and The November Plenary

Determining the following:

Power per bit / Best fit for Reach

Modulation

Channel Loss

FEC (Y/N) and Equalization requirements
Thoughts on Past Discussions
For a 25Gb/s Electrical Interface

Adopt a 25Gb/s by 16 lane electrical C2C and C2M interface defined by .3bm specifications, using current values as starting baseline text.
For a 50Gb/s Electrical Interface

Adopt a 50Gb/s by 8 lane electrical C2C and C2M interface defined by specifications yet to be provided. Use loss/length definitions and algebraic base line channel discussions to begin baseline text and specifications.
For a 100Gb/s Electrical Interface

Should we continue C2EO discussions for this?
Thank you!

From:
Vasu Parthasarathy
Beth Kochuparambil
Vivek Telang
Joel Goergen