Logic Ad Hoc Report

IEEE P802.3bs 400 Gb/s Ethernet Task Force

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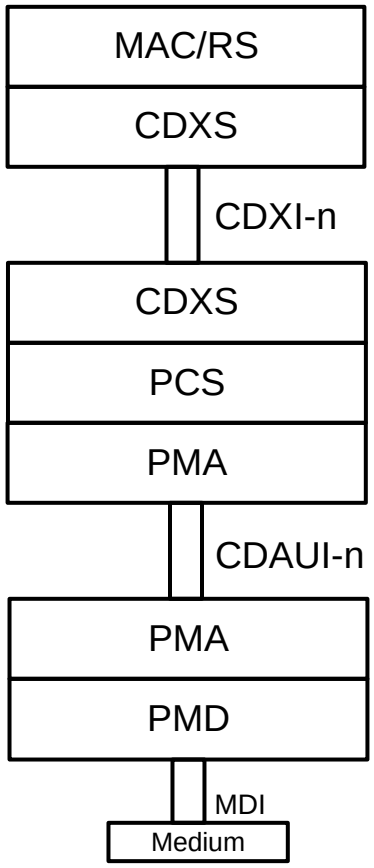
400GbE Logic Ad Hoc Priorities

- The stated charter is: **Work on technical proposals related to the 400GbE Architecture**

- Dates of future logic ad hoc meetings will be announced via the reflector
- The 400 Gb/s Ethernet Task Force Logic Ad Hoc:
  - Offered one meeting on August 25th, did not receive any requests for presentation, so the meeting was cancelled

Architecture

- This architecture has been proposed in the last two meetings, so far I have not heard any reasons why this generic architecture cannot support our needs for the 400GbE project



Decisions that are Key for Logic Progress

- PMD technology choices
  - What FEC is needed, what gain is required to close the budget for each given PMD objective
  - Decide on a latency target
    - Need to make tradeoffs between latency/gain/complexity/re-use
  - Do we need PMA muxing, if yes, bit, block, FOM or some other muxing?
  - Do we want end to end, segment by segment or encapsulated FEC structures?
  - Once we understand the above, we can create a FEC architecture
- Do we need to define an extender sublayer in this project?
- EEE decisions
  - Continue to only support fast wake only, or something else?
- OTN reference point
- Once we make the above decisions, we have a lot of technology/mechanisms we can leverage and we can define a compact PCS and/or CDXS

Thanks!