FEC Configuration Analyses For 400Gb Ethernet

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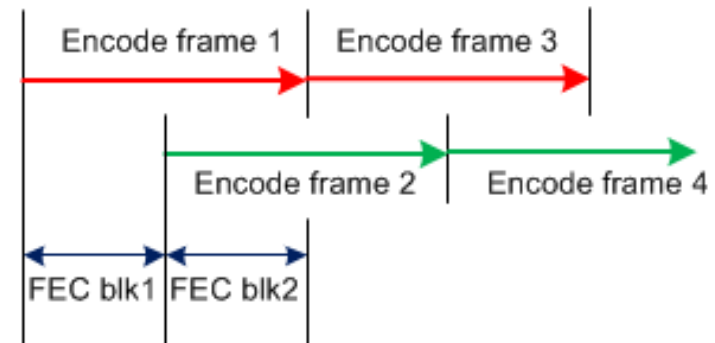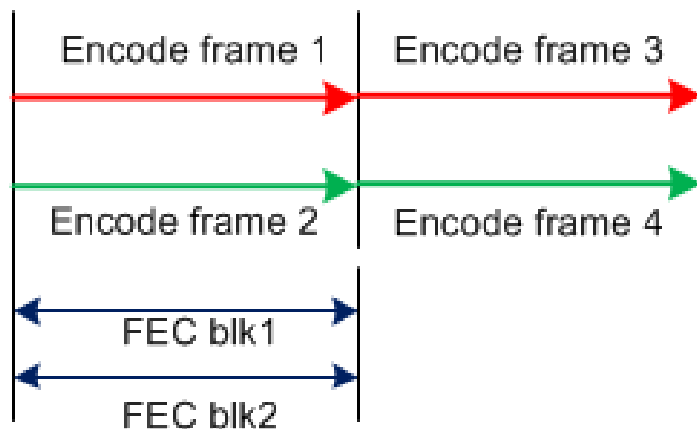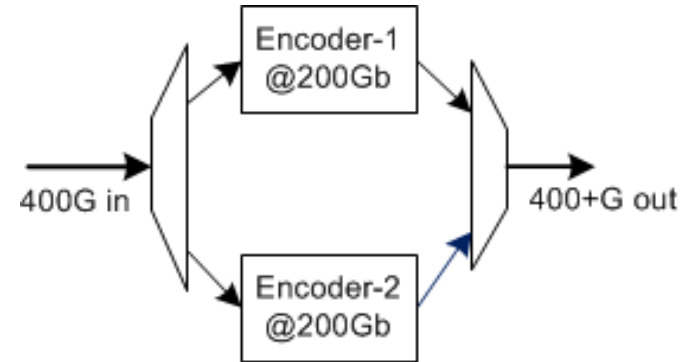
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- **Assume we are working on 4000GbE (in 2022?)**
    - Assume we still use single RS(528, 514, m=10) code.
    - This means that we need finish encoding of a RS block in 1.28ns (i.e., 1 clock cyc with f=781.25Mhz) . With reasonable projection of CMOS technology advancement, this goal is impractical or even impossible to achieve by that time. Thus parallel encoders are required.

- **Question: Are we passing the corner point with 400GbE?**

SIMPLE COMPUTATION

- **Assume digital clock frequency f=400Mhz.**
  - 400Gbps/400Mhz= 1000bits/cyc
  - In 100G-KR, parallelism for RS-FEC is best set as 160bits/cyc. Thus we may need 6x more parallelism, which is most likely impractical or inefficient with current CMOS technology.
  - Employing parallel encoder or decoder modules is a way to meet high throughput requirement [1]. But this may not be a good option.

[1] http://www.ieee802.org/3/bs/public/adhoc/logic/jul01_14/wangz_01_0714_logic.pdf

PARALLEL ENCODER FOR SINGLE AND INTERLEAVED BLOCK CODES

- Assume each encoder is parallelized with a proper level of parallelism.
- The encoding latency for single code is about N bits/400Gbps, where N is FEC block length.
- The encoding latency for interleaved codes is nearly zero.

- Assume each decoder has the same speed.
- The decoder latency for interleaved codes is Nbits/400Gbps longer than single code case.
- In summary, the combined latency for either case is about the same.

COMPARISONS OVER USING SINGLE CODE
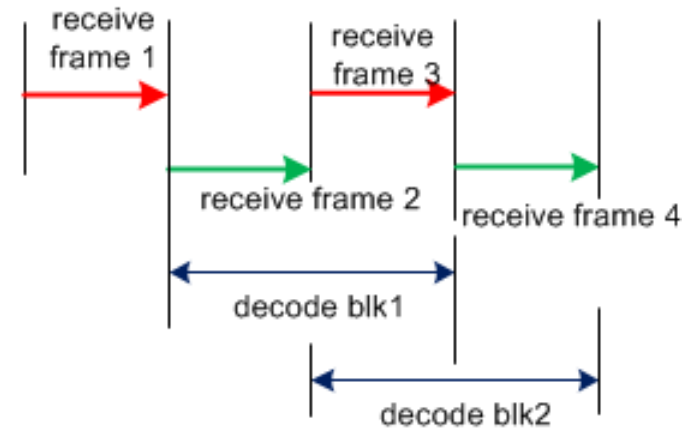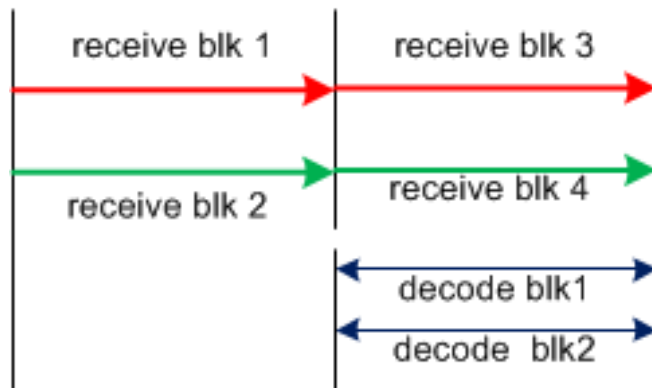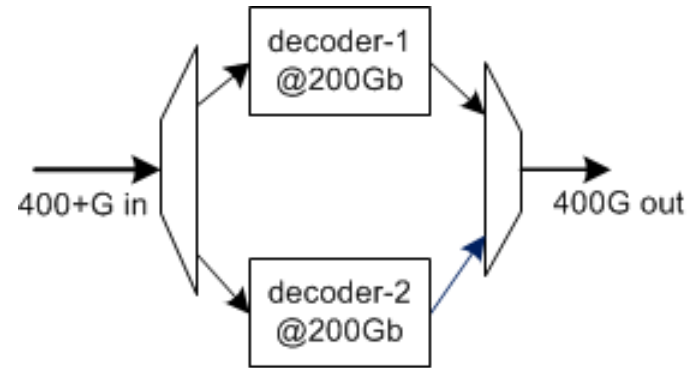
- **Using 2 (or 4??) interleaved codes:**
  - Similar HW complexity and similar power consumption
  - Comparable total latency
  - Linearly increased burst error correction capability
  - Less performance degradation due to error propagation

- **Three FEC strategies were discussed in May meeting (gustlin_3bs_02_0514)**
  1) End to end
  2) Segment by segment
  3) Encapsulated FECs
- **None of the above methods are very promising.**
- **The following strategy may worth consideration:**
  1) Use interleaved RS(528, 514) as base FEC
  2) Add (programmable) extra parity at PMD level
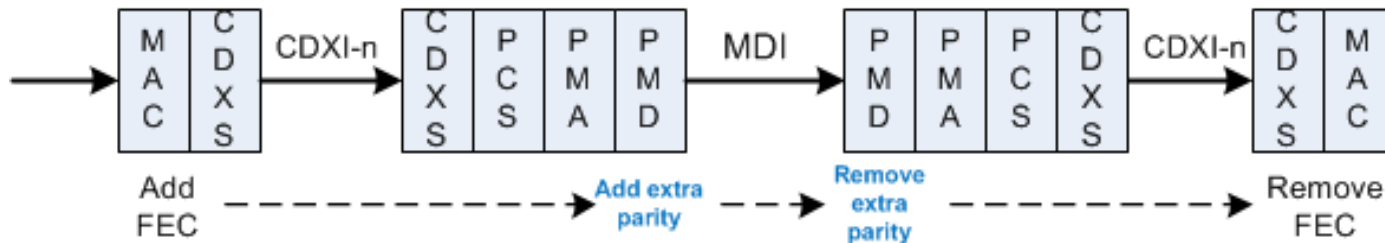
- FEC latency may not decrease as expected when data rate increases beyond certain level because routing congestion in highly-parallel implementation can be a limiting factor.

- Interleaved block codes have advantages in certain aspects over single block code.

- Adding adjustable extra parity at PMD level may resolve FEC strategy issues for 400GbE.

THANK YOU