Single Wavelength 112Gb/s PAM4 Transmission Over 10km SSMF Using a 1.3μm EML

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Objectives

- To investigate the link power budget of a 112Gb/s PAM4 over 10km link by using post-DSP only, or both pre- and post-DSP

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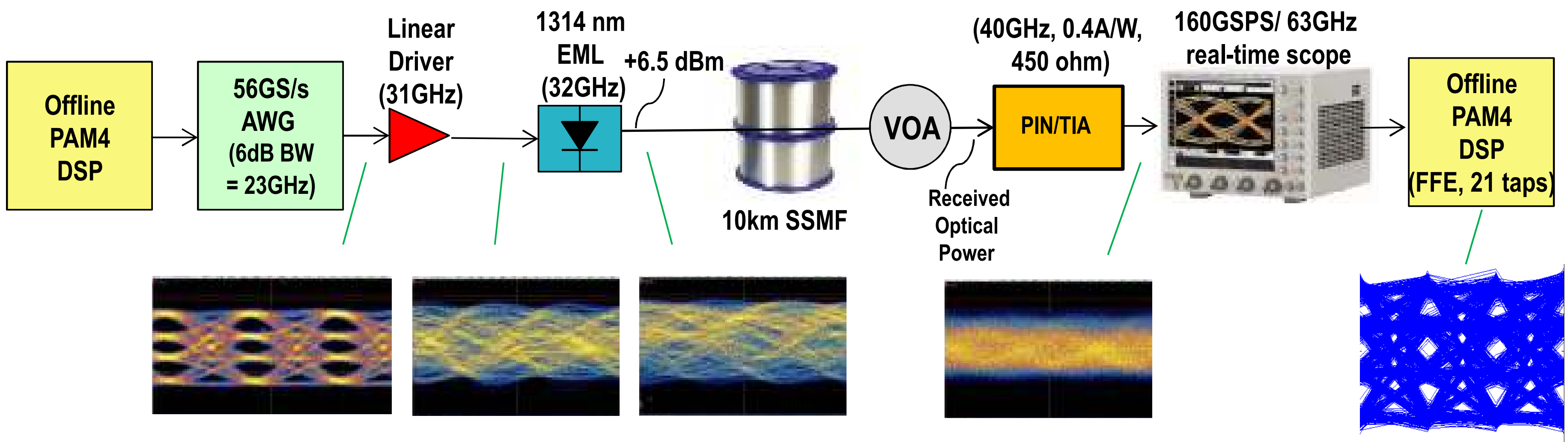
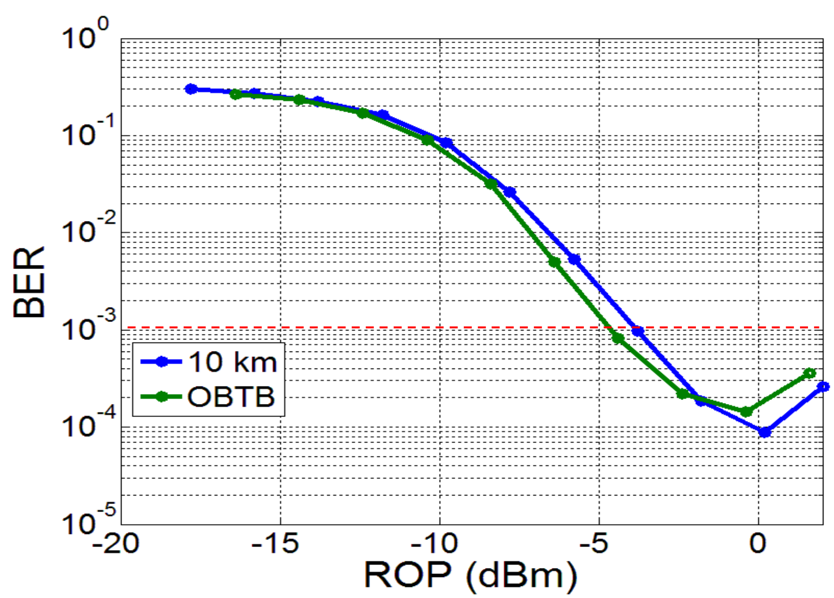
102~112Gb/s PAM-4 Experiments

Reference	Link distance	TX output power (dBm)	ROP @ BER=1e-3	Optical TX	DAC+ Driver Amp BW	RX 3-dB BW	Waveform capture & off-line Equalizer
Stasser_3bs_01_0714	2 km	+3.3dBm	-7.5 dBm	EML 32GHz 6dB ER	PPG + driver (32GHz)	40Gb/s	80GS/s DSO (analog BW=33GHz), FFE (16 taps)
Bhatt_3bs_01_0714	2, 10 km	+0.8dBm	3.8e-3 @ -5.3dBm	SiP MZI 19GHz	DAC (15GHz) + driver (27GHz)	33GHz	DSO (2-ch)
Mazzini_3bs_0814 (ad hoc)	2.2 km	+?dBm	-8.5 dBm (estimated)	LN MZI 35GHz	PPG with No driver	33GHz	160 Gsps DSO (analog BW=63GHz) , FFE (22 taps)
Hirai_3bs_01_0714	0 km	+5 dBm	-6 dBm	LN MZI (? GHz)	DAC (15GHz) + driver	33GHz	100GS/s ADC (~200 taps) Nyquist Shaping
Way_3bs_01_0914	10 km	+6.5dBm	(I) -5 dBm (II) -6 dBm	EML 32GHz 7.4dB ER	AWG + driver (31GHz)	40GHz	160 Gsps DSO (analog BW=63GHz) , (I) post FFE (21 taps); (II) pre-FFE (19 taps)+post-FFE (21 taps)

Total end-to-end link budget of 10~12.3 dB (2 (MUX)+ 2(DEMUX) + 4 or 6.3 (channel) + 2 (TDP)) needs to be met

Single-wavelength 112Gb/s PAM-4 Experiment (I)
Post-DSP Only





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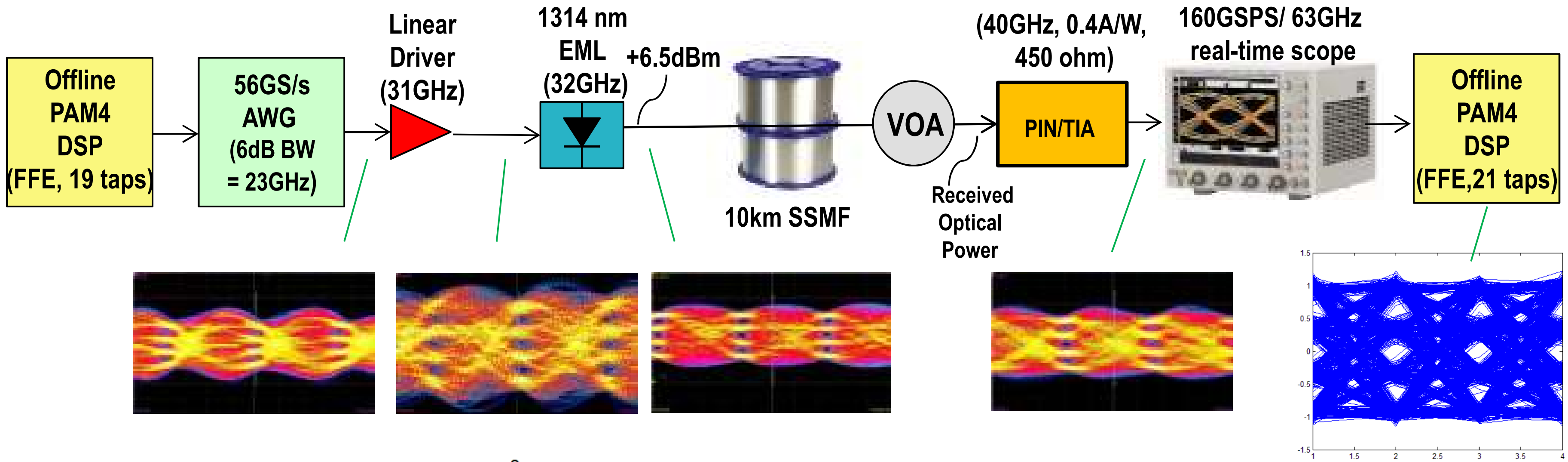
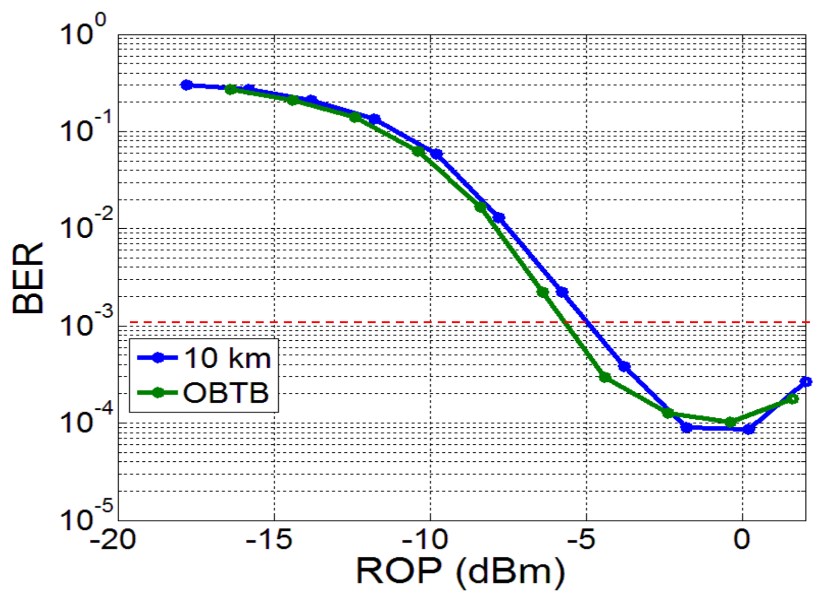
Single-wavelength 112Gb/s PAM-4 Experiment (II)
Pre- and Post-DSP





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112Gb/s PAM4 Experiment Parameters

Parameter	Value	Unit
DAC 6dB bandwidth	23	GHz
DAC ENOB within 6dB bandwidth	> 4.5	bits
Driver amplifier 3dB bandwidth	31	GHz
EML 3dB bandwidth	32	GHz
Extinction ratio	7.4 (4.7 with pre-DSP)	dB
PIN/TIA 3dB bandwidth	40	GHz
Receiver input spectral noise density	≤ 40	pA/√Hz
Receiver responsivity @ 1314nm	0.4	A/W
ADC bandwidth	63	GHz
ADC ENOB (up to 30GHz)	> 5	bits

Practical Product Challenges

- **Signal Integrity**
  - 112Gb/s PAM4 transmission among PAM4 chip, drivers, and TOSA/ROSA with FPC, could incur signal integrity degradation at the junctions of these components and at PCB traces.
  - Success of co-packaging of PAM4 die, driver die, and E/O & O/E dies remains to be proven

- **ADC**
  - Can CMOS-based ADC perform as well as instrument-level ADC (they are not based on CMOS today)?

- **Uncooled CWDM versus Cooled LAN-WDM**
  - Link power budget is too tight to tolerate CWDM optical performance
    - More optical power fluctuation penalty
    - More optical fiber dispersion penalty

Summary

- **Depending on various penalty factors that need to be added, and depending on what the pre-FEC threshold is, the link power budget is tight for 112Gb/s PAM4 over 2km, and even tighter for over 10km**

- **In this experiment, there is still room for improvement on**
  - Receiver responsivity (0.4A/W → > 0.6A/W)
  - Receiver spectral noise density (40 pA/√Hz → < 25~30 pA/Hz)
  - Receiver bandwidth (40GHz → 32~35GHz)

- **Pre- and post-DSP help improve the receiver sensitivity @ BER=1e-3 by 1~1.5dB in comparing to the case of post-DSP only, achieving a total end-to-end budget of 12.5dB**