



## **52Gb/s Chip to Module Channels using zQSFP+**

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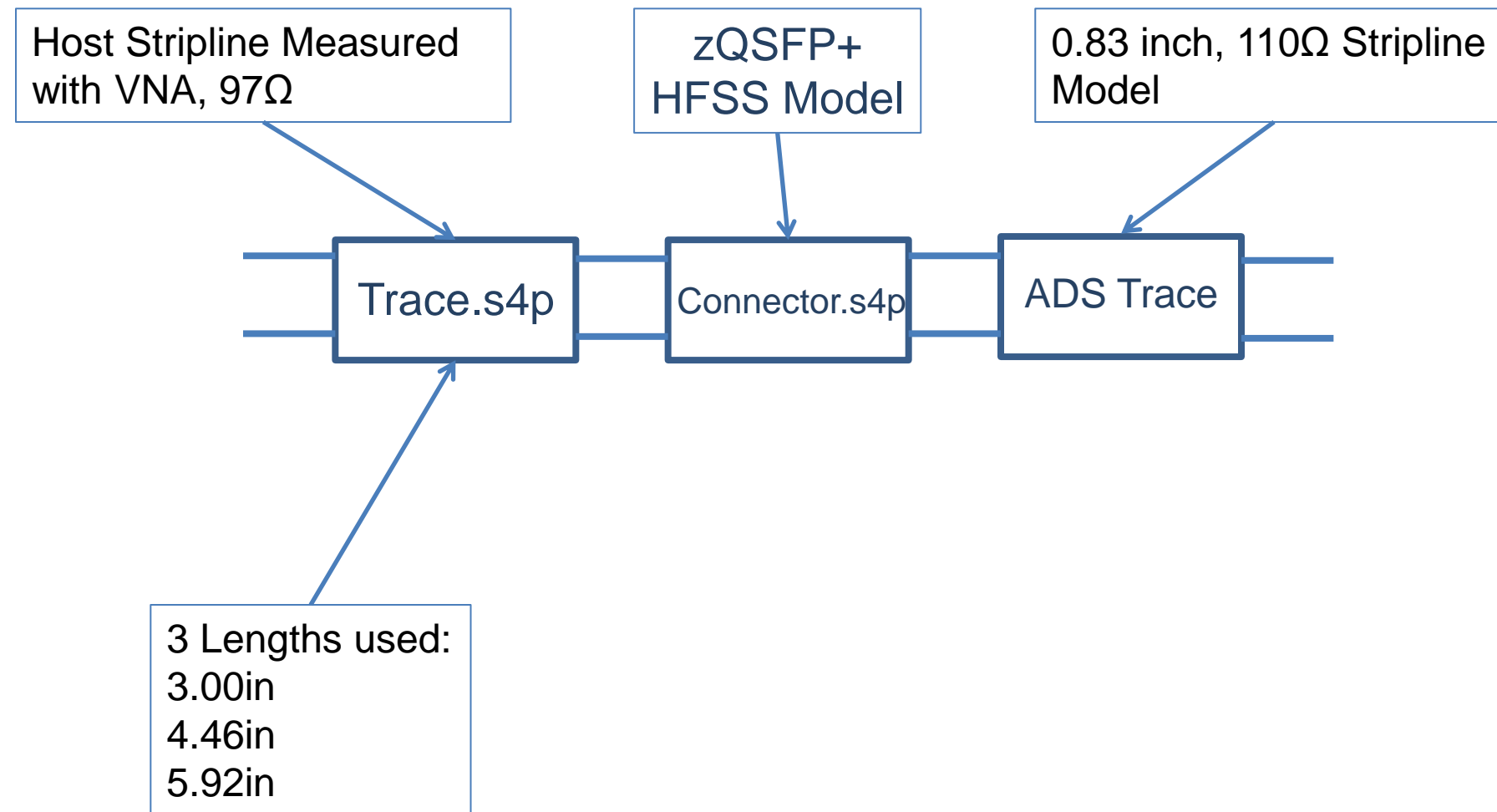
Barrett Bartell      Qlogic

Tom Palkert      Molex

Scott Sommers      Molex

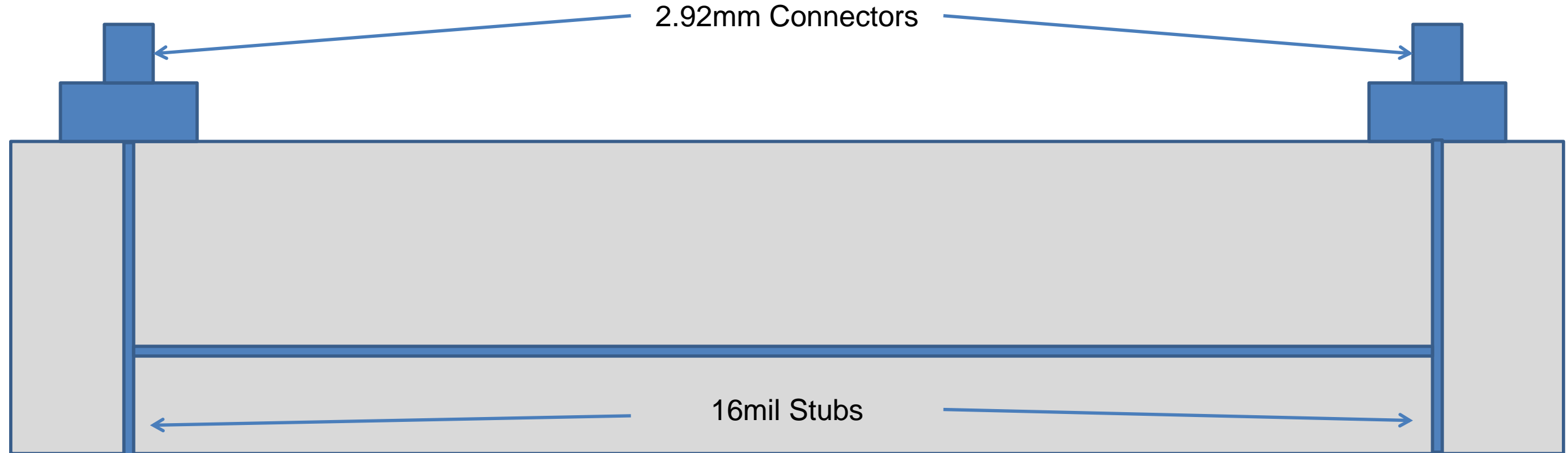
10/23/2014

# Channel



# Host Stripline (measured)

- Trace Width: 4.5mil
- Gap: 5.5mil
- PCB: FR408HR
- Surface Roughness: RTF
- Differential Z: 97Ω



# Molex zQSFP+ (56gig) SMT Connector

- Molex zQSFP+ (56Gig) SMT connector
- S-parameters provided courtesy of Molex
- Backward Compatible
- Retuned and Optimized for 56 gig
- Signal SMT launch pads shortened by .25mm, ground pads remain the same size as today
- Same mating interface (connector to module) as today



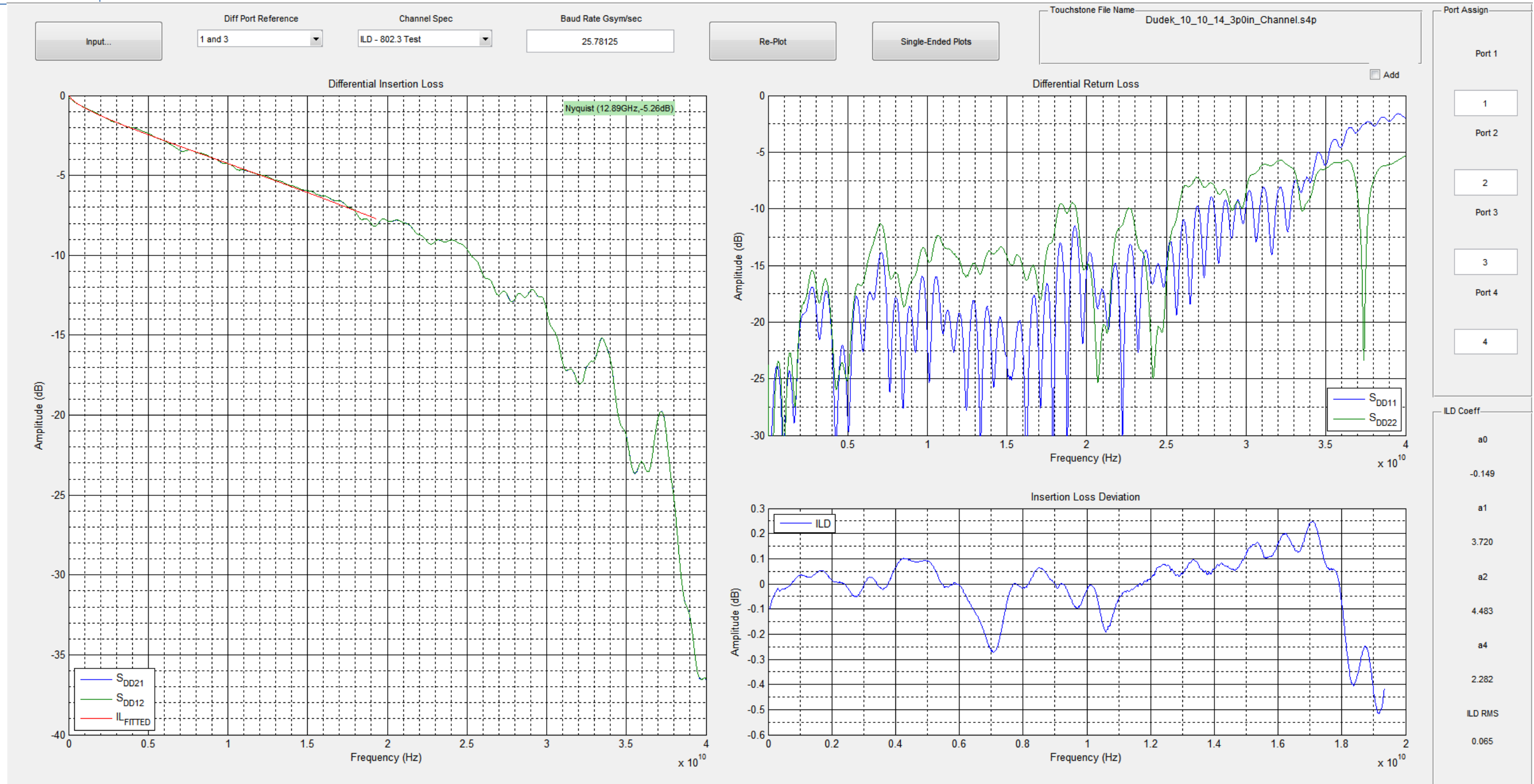
# Comments on the channels.

- Channel loss per inch is conservative (based on measurements of FR408HR), Megtron 6 or equivalent could be used with lower loss.
- Channels are provided with a range of potential target losses.
- Difference in impedance between the host and module boards is not worst case, but 110 Ohms was chosen for the Module board to make it as bad as it could be with the measured channels.
- Via stub length is worst case, however the vias aren't a major contributing factor to the degradation.
- The 2.92mm connectors are probably not as bad as an IC package/breakout is and certainly don't have the loss that a large package would have.
- For these reasons I am not suggesting these are worst case channels, but they are realistic and any proposed solution should operate on them, (or at least the shorter ones if we choose a lower loss maximum target loss).
- The ILD fitting and  $FOM_{ILD}$  are per Clause 93A except that the fitting was only to 0.75\*fb. The fitting was performed for both 52GBaud (NRZ) and 26GBaud (PAM4) results. ( $FOM_{ILD}$  is called  $ILD_{rms}$  )
- Channel Models have been submitted for uploading to the channel data area as Chip to Module channels.

# 3.0 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



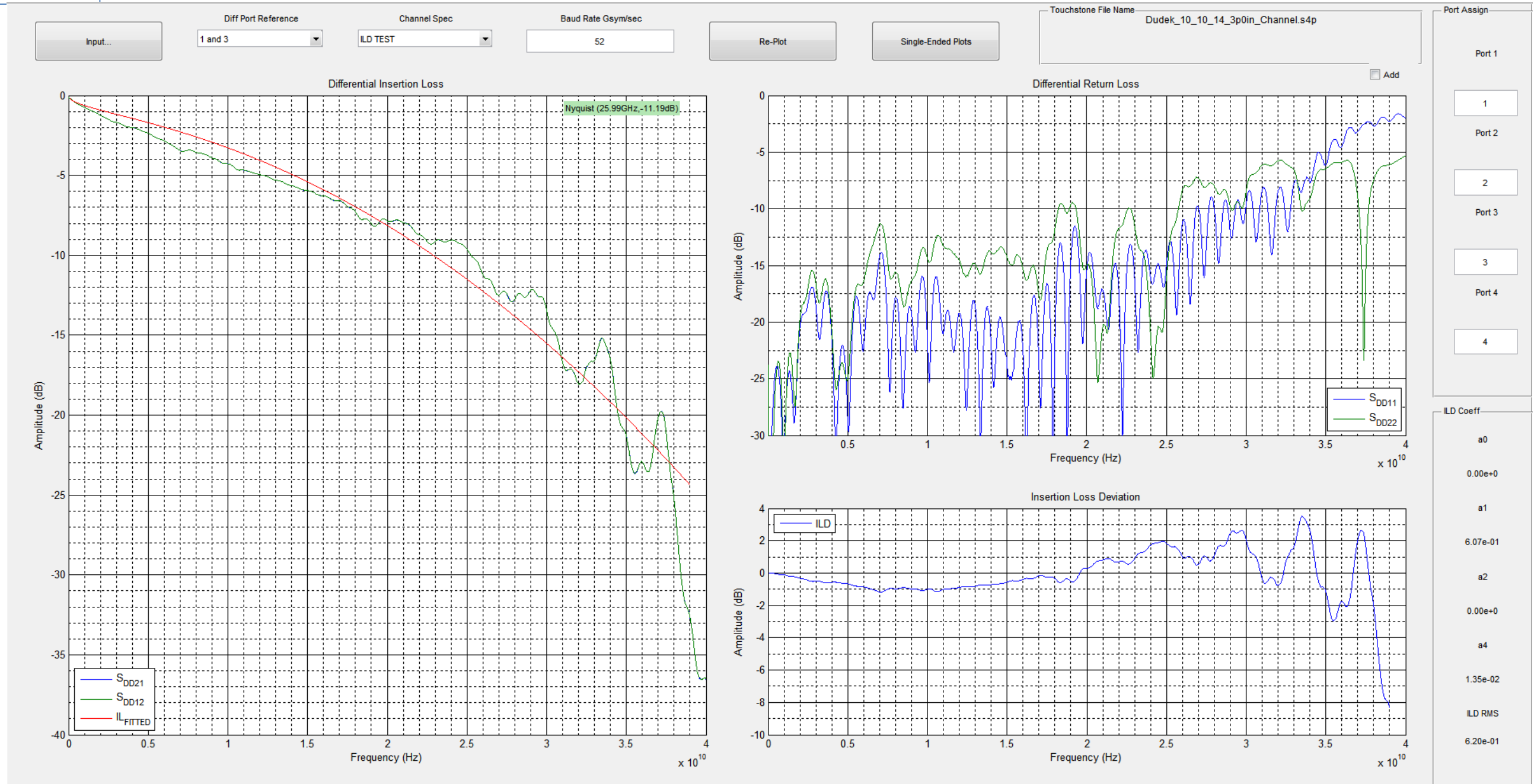
25.78125 Gb/s



# 3.0 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



52 Gb/s

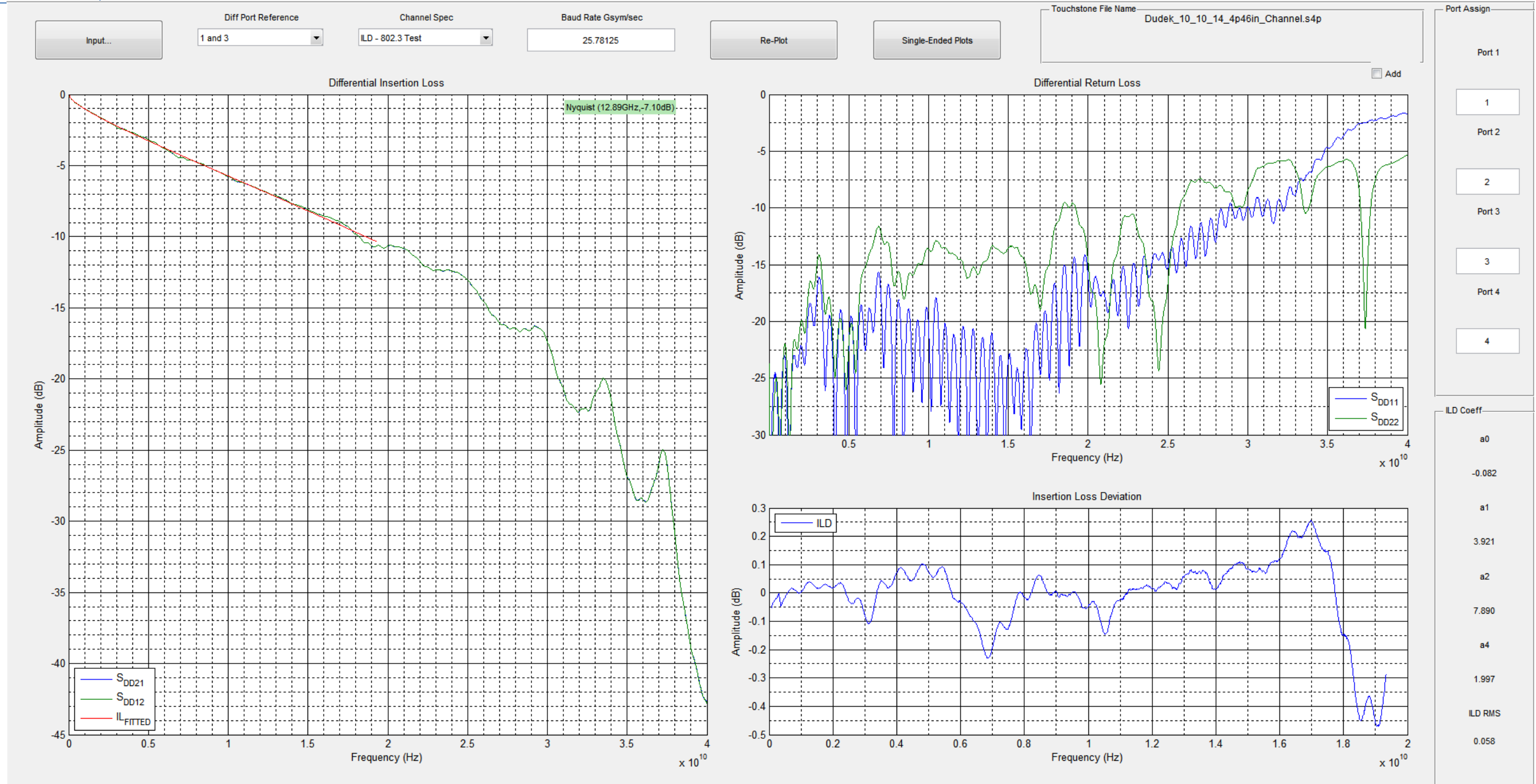




# 4.46 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



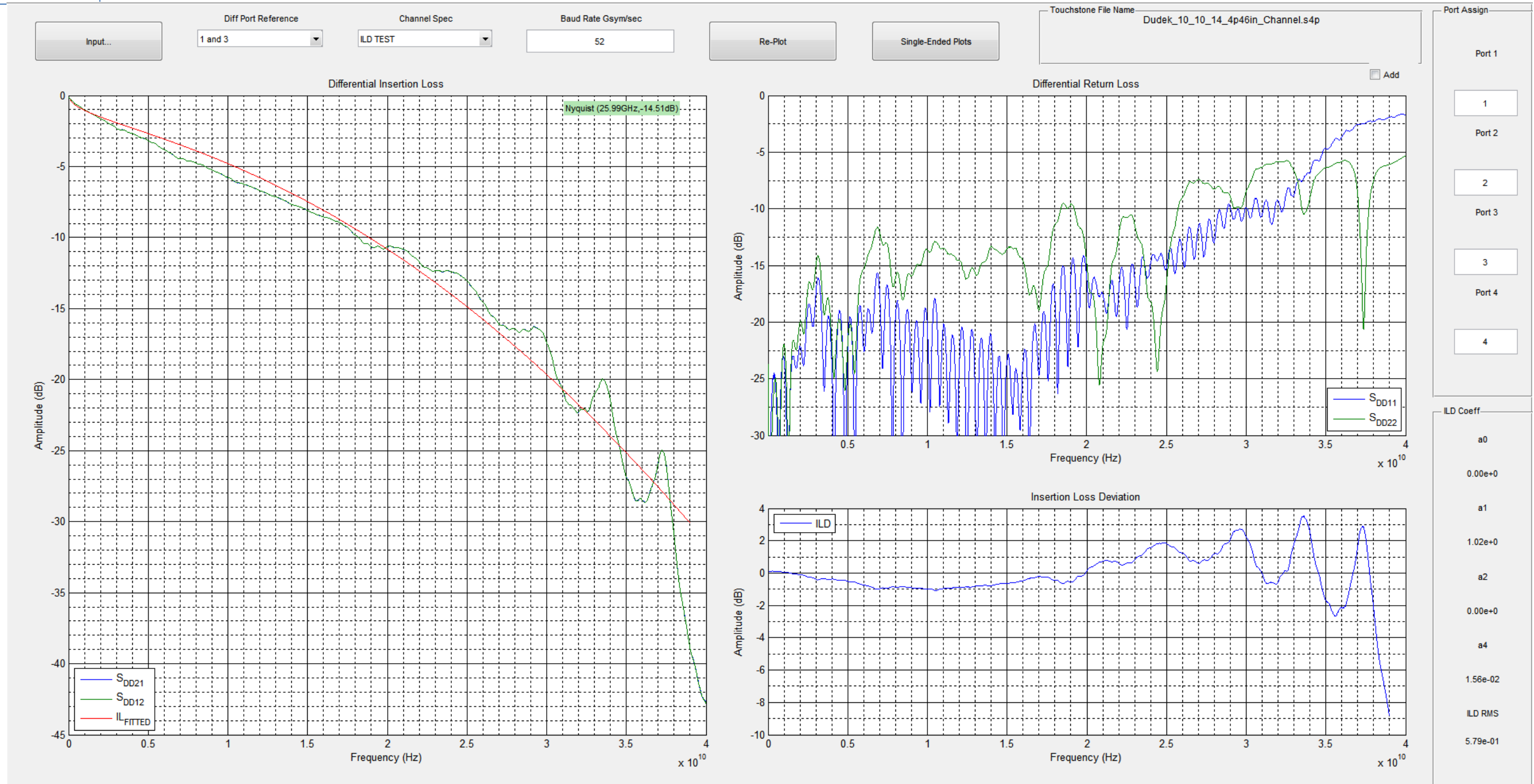
25.78125 Gb/s



# 4.46 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



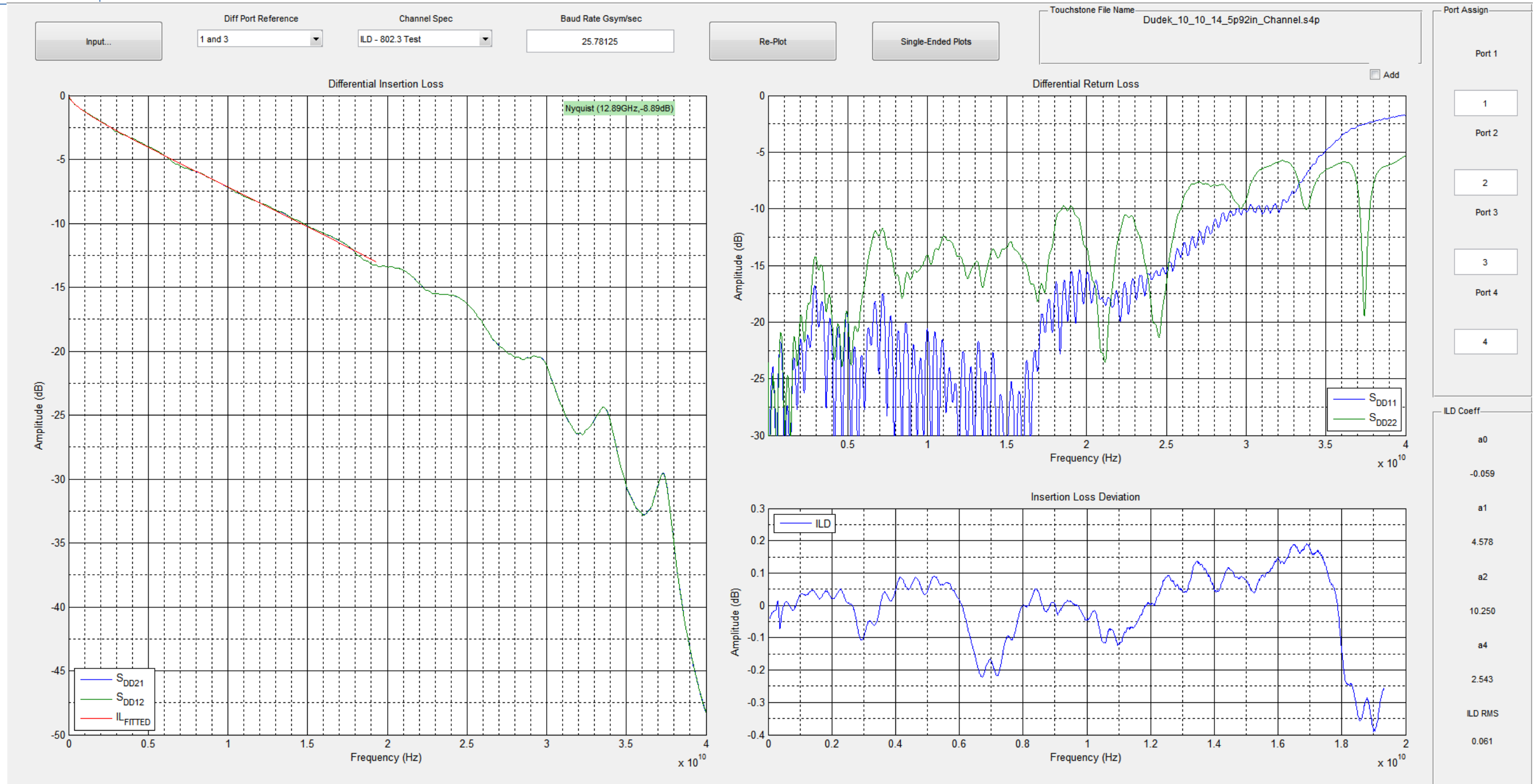
52 Gb/s



# 5.92 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



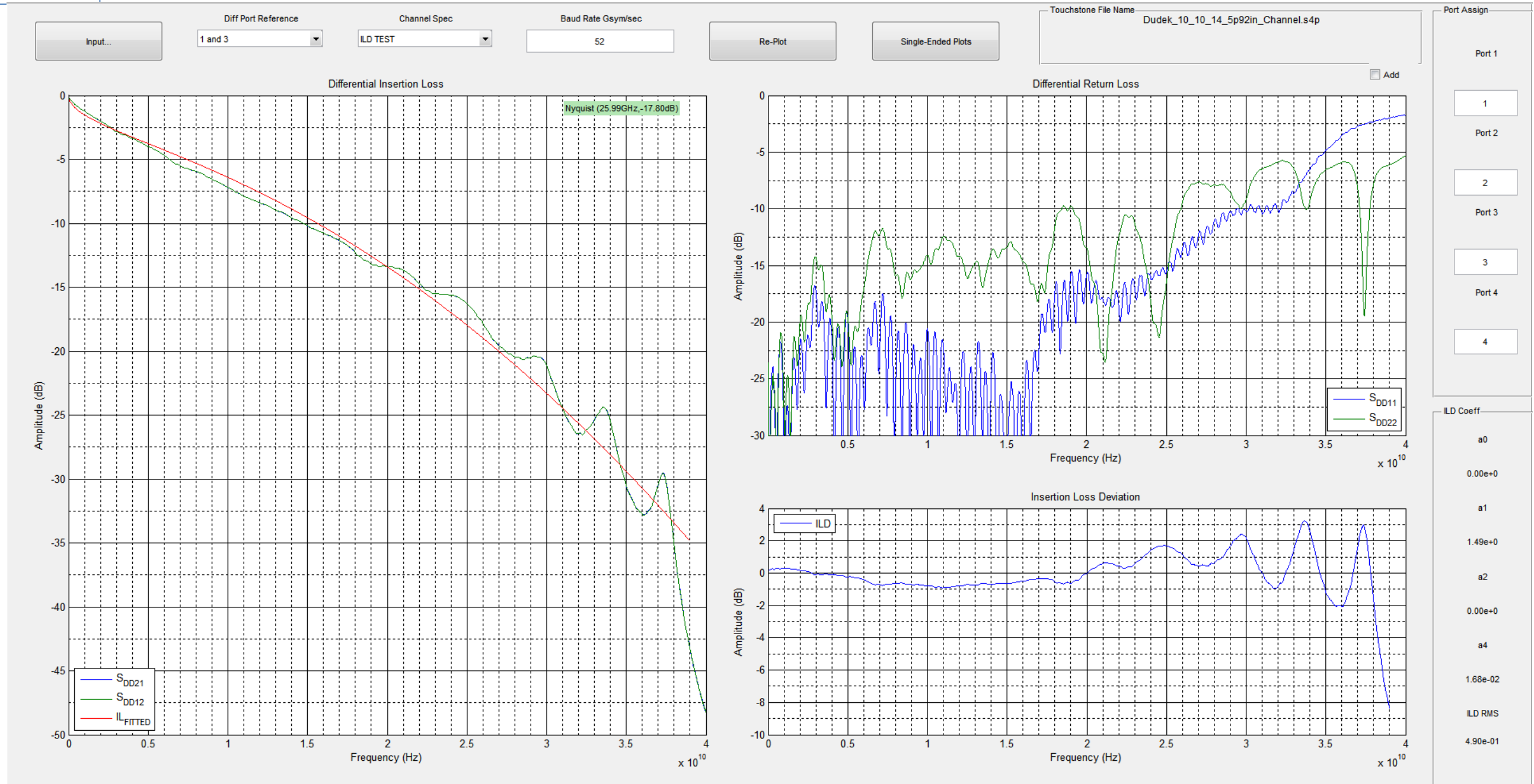
25.78125 Gb/s



# 5.92 inch Host Trace (97Ω) + zQSFP + 0.83 inch Stripline (110Ω)



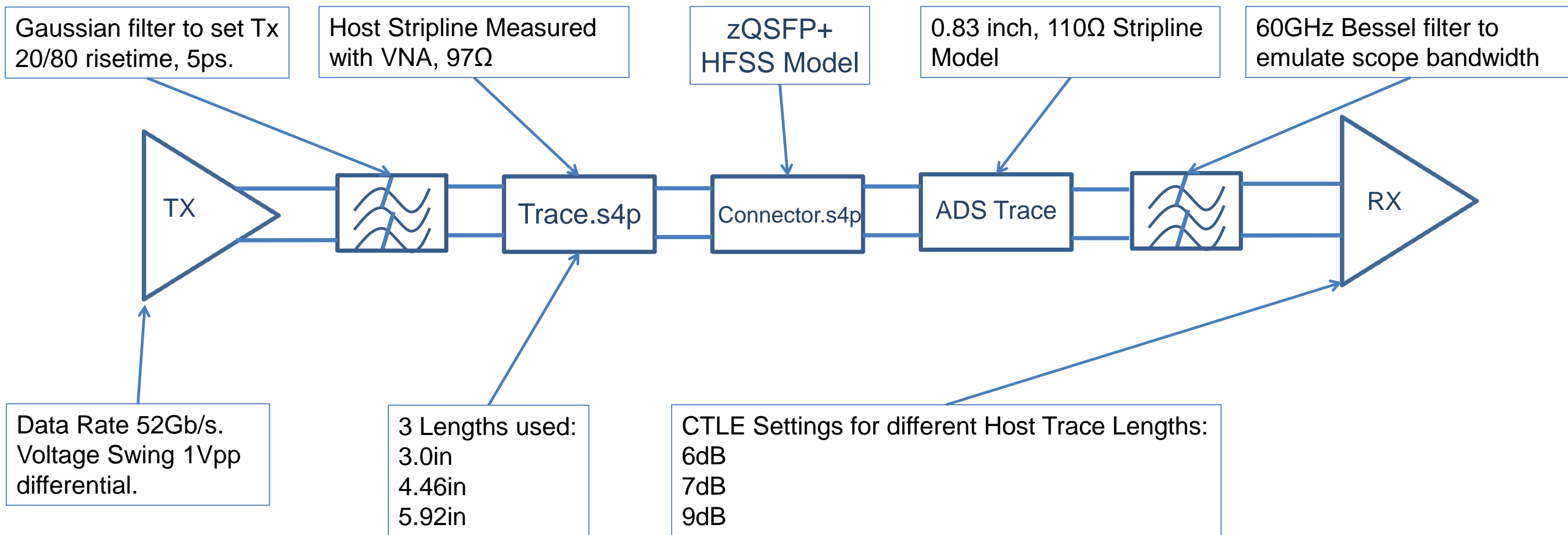
52 Gb/s



# **NRZ Performance with Frequency-scaled 802.3bm CTLE**

**(52 Gb/s, 1e-6 BER)**

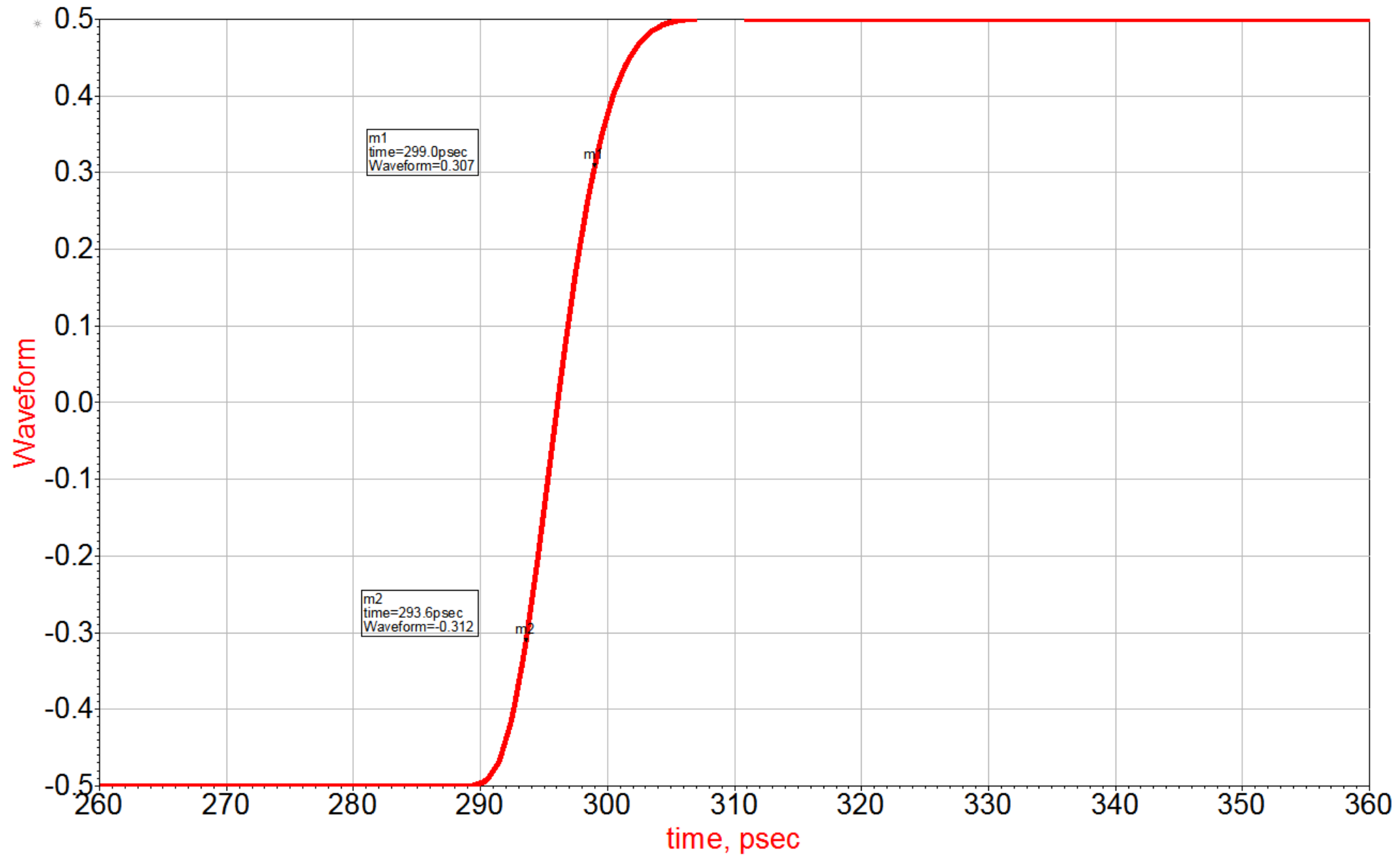
# Channel



# Comments on the Simulations.

- **This simulation is not making a proposal that the optimum solution is no Tx FIR and just an Rx CTLE but it investigates the suggestion that this is out of the question.**
- **The Tx risetime could be somewhat faster than the on-die risetime.**
- **Jitter hasn't been included in the simulation.**
- **As discussed earlier the 2.92mm connectors are likely to be better than an IC package/footprint and the channels aren't completely worst case.**
- **Additional package loss beyond the 2.92mm connector loss is likely to be equivalent to longer host traces.**

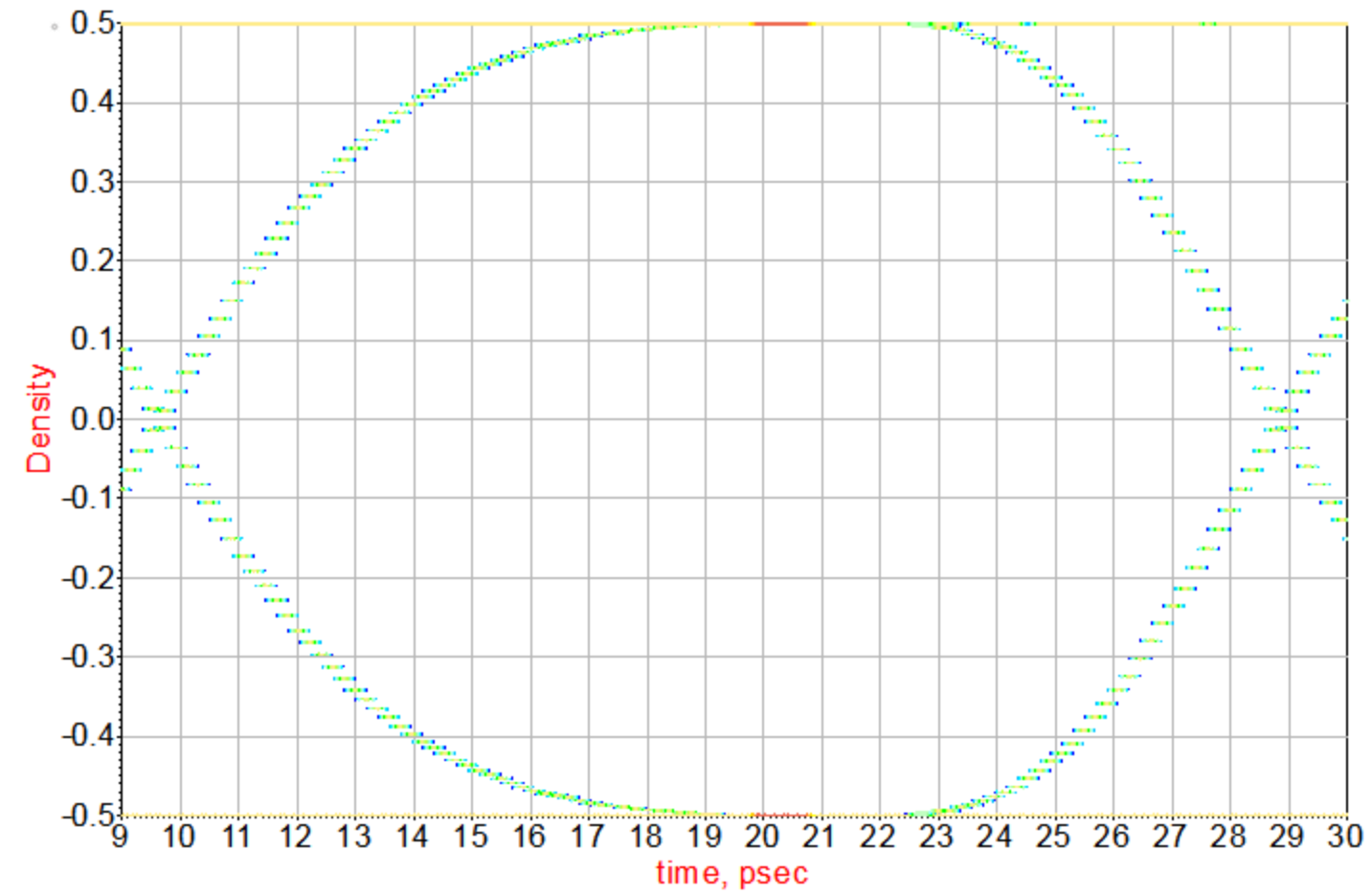
# TX 20/80 Risetime: 5ps





# TX Eye: After Gaussian Filter

BER	HeightAtBERList	WidthAtBERList	EHEW
1.000E-6	0.998	1.905E-11	1.901E-11



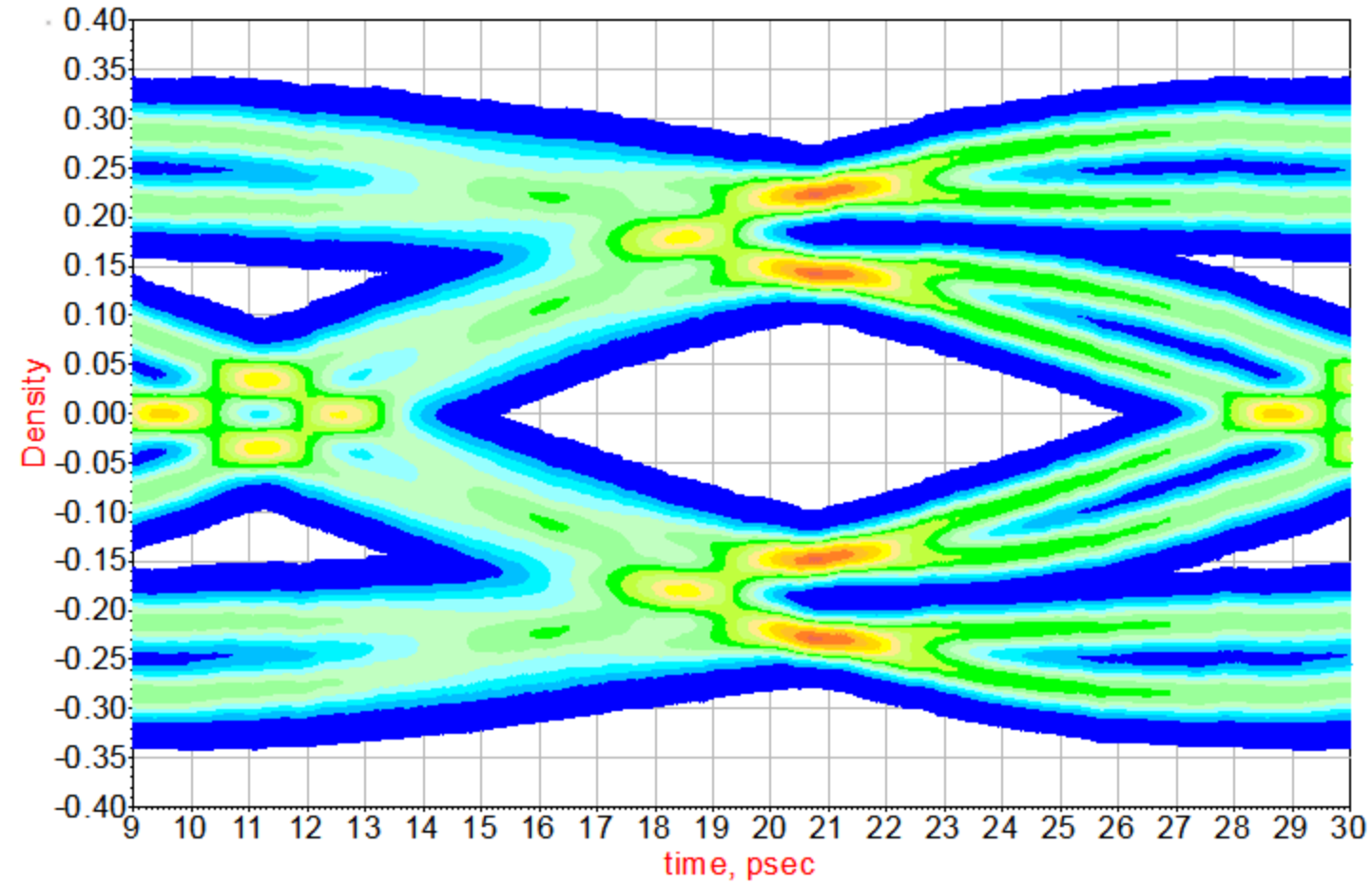
# 3.0 inch Host Trace + zQSFP + 0.83 inch Stripline



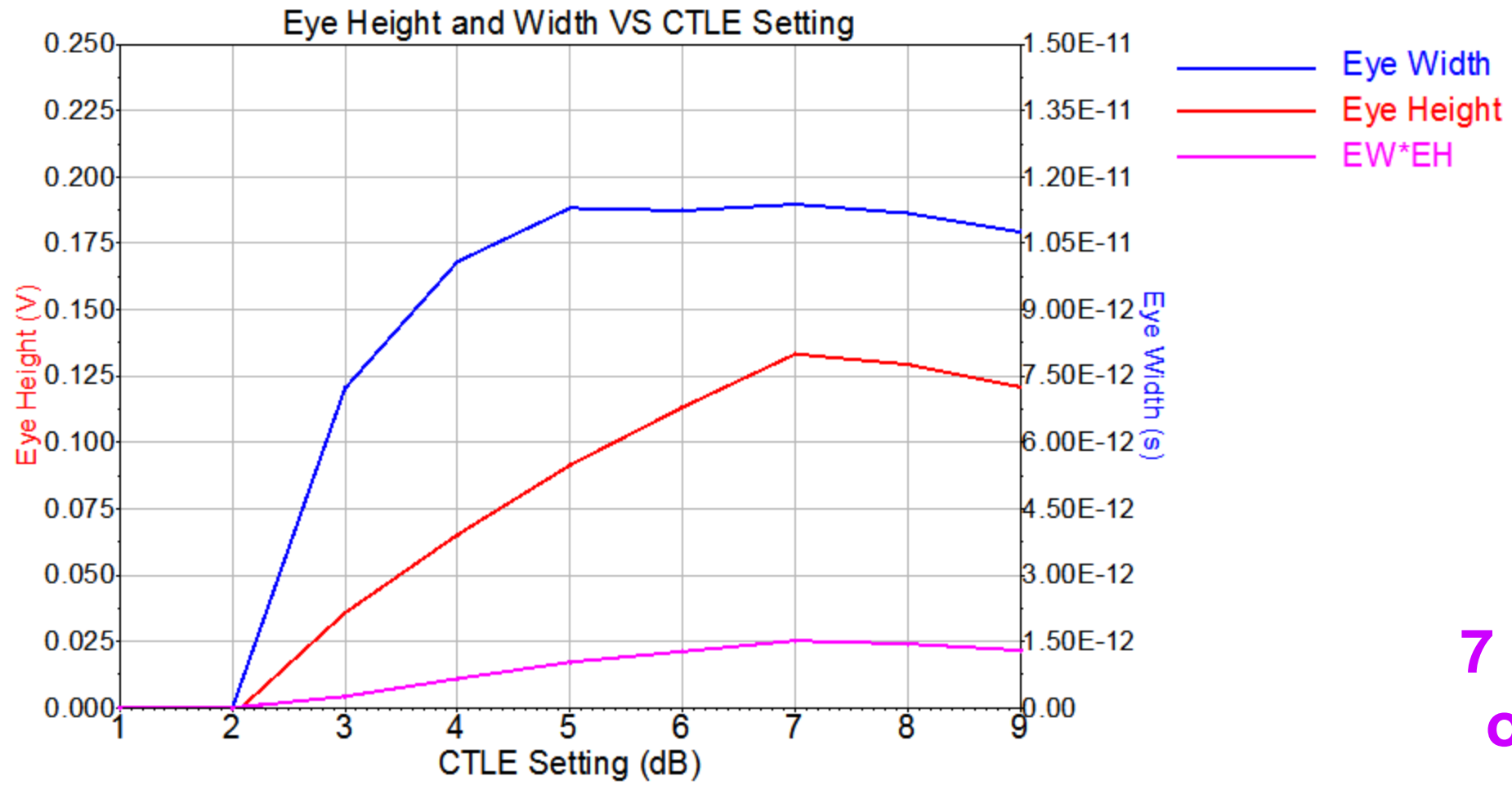
**6 dB CTLE optimum**

# 3.0 inch Host Trace + zQSFP + 0.83 inch Stripline, CTLE 6dB

BER	HeightAtBERList batchNumber=1	WidthAtBERList batchNumber=1	EHEW batchNumber=1
1.000E-6	0.192	1.092E-11	2.099E-12



# 4.46 inch Host Trace + zQSFP + 0.83 inch Stripline

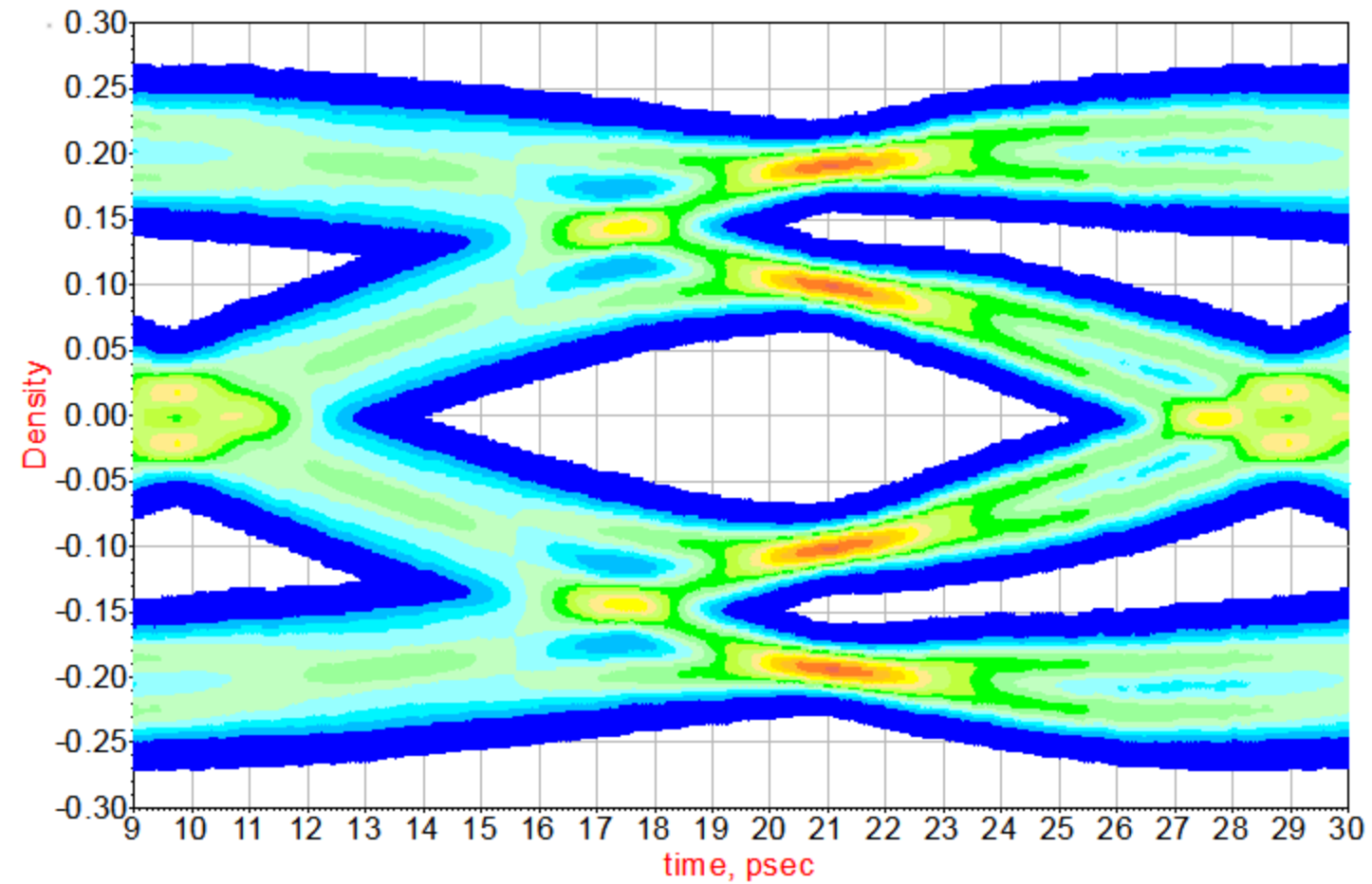


**7 dB CTLE optimum**

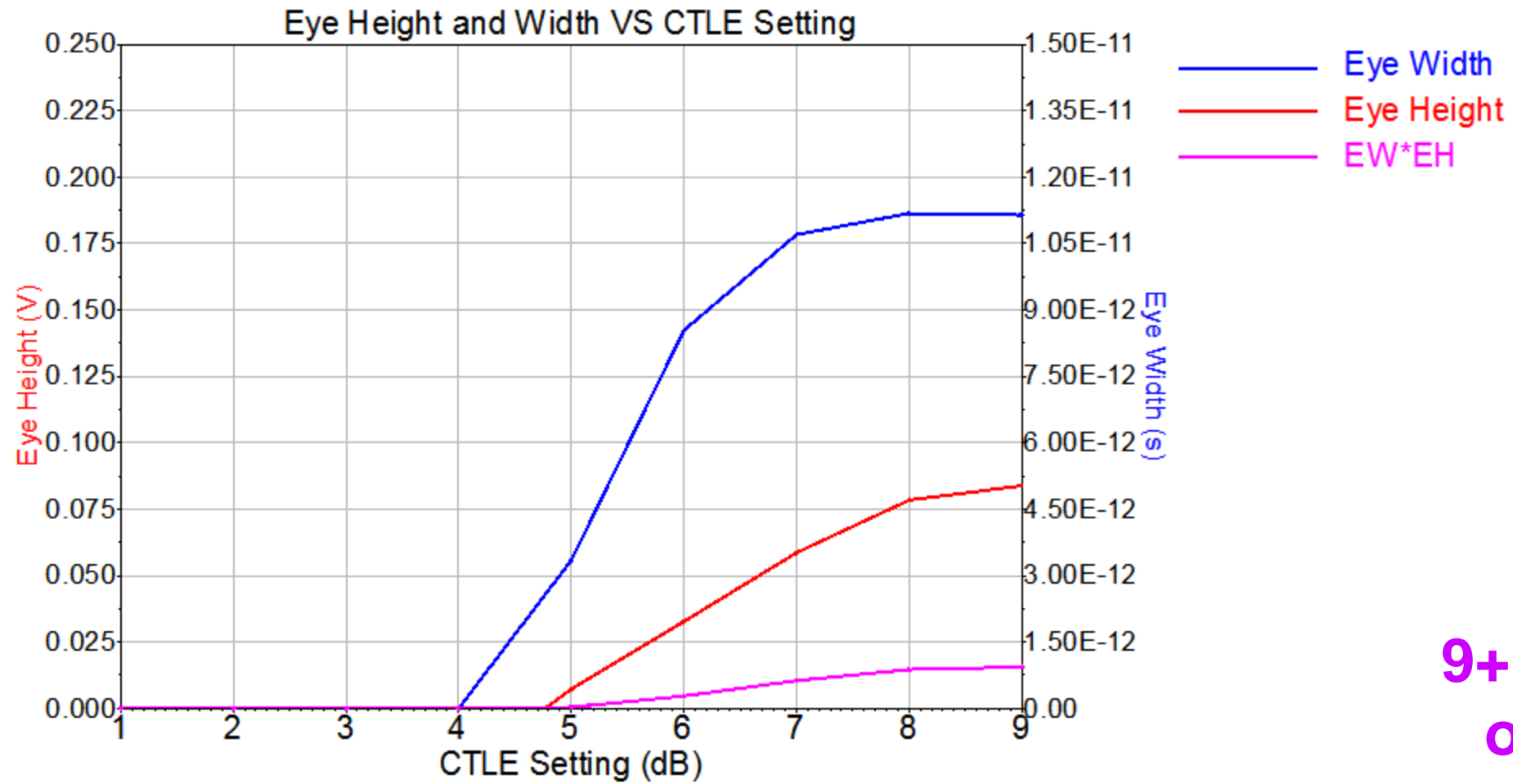
# 4.46 inch Host Trace + zQSFP + 0.83 inch Stripline, CTLE 7dB



BER	HeightAtBERList batchNumber=1	WidthAtBERList batchNumber=1	EHEW batchNumber=1
1.000E-6	0.133	1.138E-11	1.517E-12



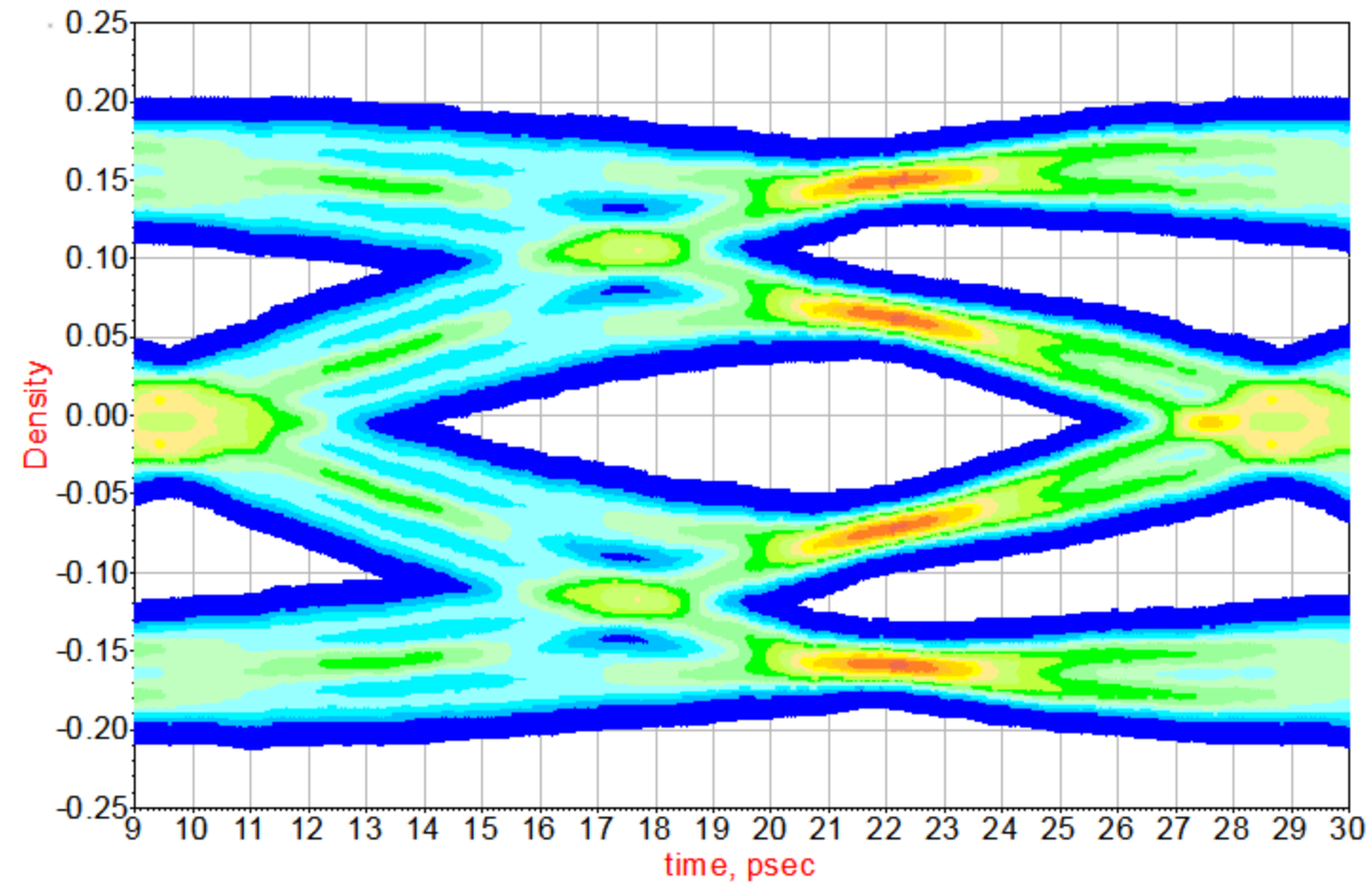
# 5.92 inch Host Trace + zQSFP + 0.83 inch Stripline



**9+ dB CTLE optimum**

# 5.92 inch Host Trace + zQSFP + 0.83 inch Stripline, CTLE 9dB

BER	HeightAtBERList batchNumber=1	WidthAtBERList batchNumber=1	EHEW batchNumber=1
1.000E-6	0.084	1.116E-11	9.416E-13



# Conclusions from the Simulations.

- **The eyes are reasonably open even on the highest loss channel (approx 18dB) at Nyquist.**
- **More work would be required to determine if the NRZ, no Tx FIR, CTLE only Rx is a viable solution for Chip to Module.**