CDAUI-8 chip-to-module and chip-to-chip interfaces using PAM4

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Topics

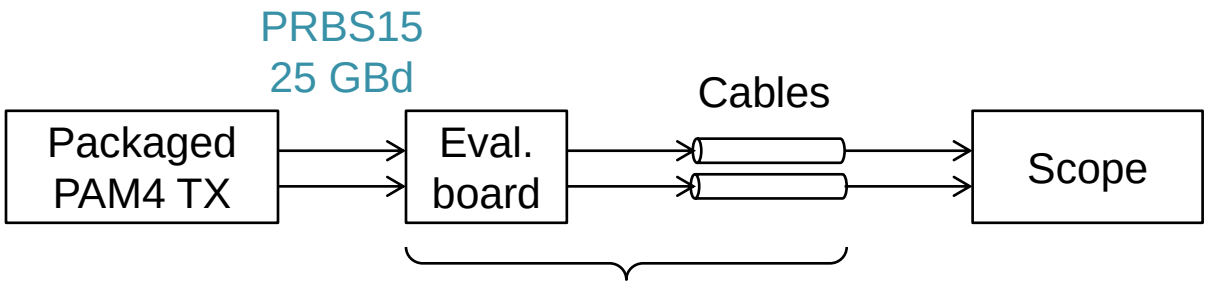
- Measured results
- Simulated results
- Power estimates
- Summary

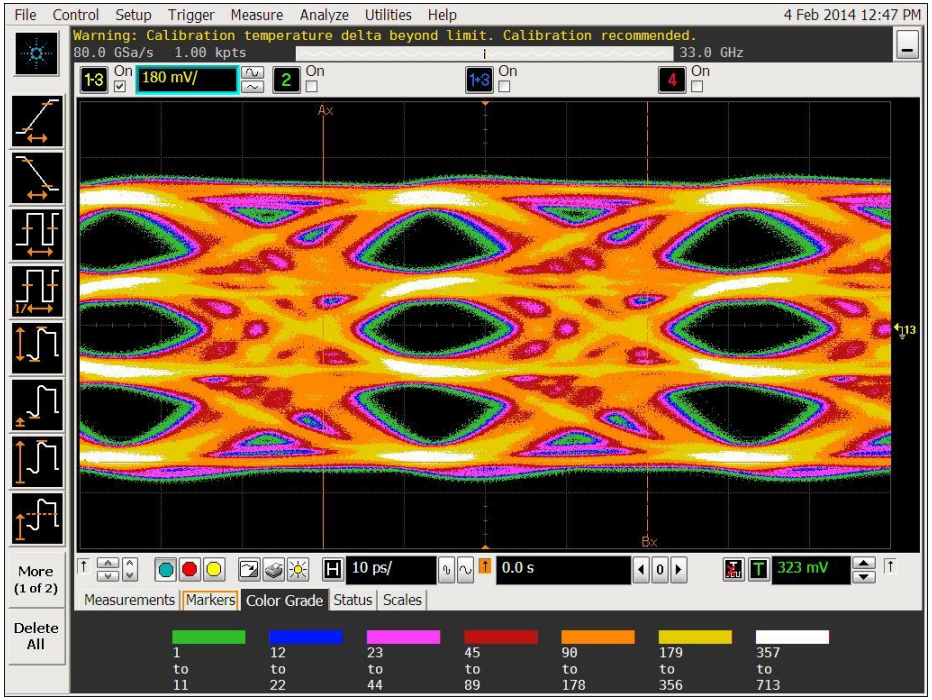
Measured results

- Prototype PAM4 transceiver
  - 28 nm CMOS technology
  - Highly leverages existing circuits from PAM2 implementation
  - No forward error correction
  - Includes PRBS generators and checkers

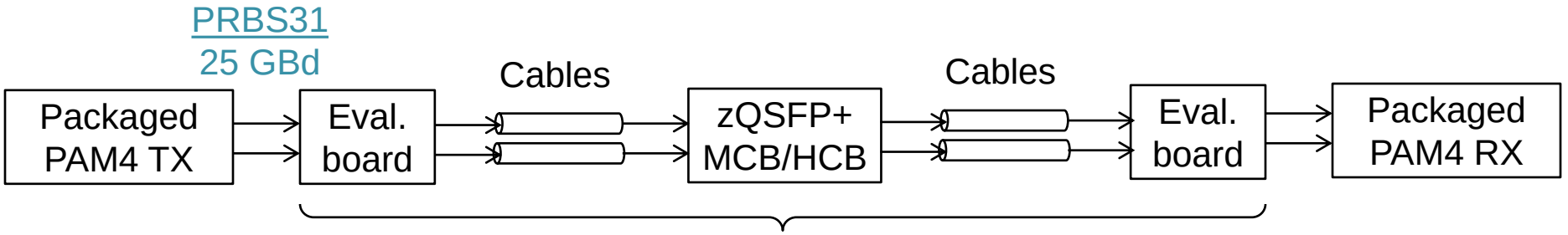
- BER measurements based on internal PRBS checker

Measured results: Experiment #1

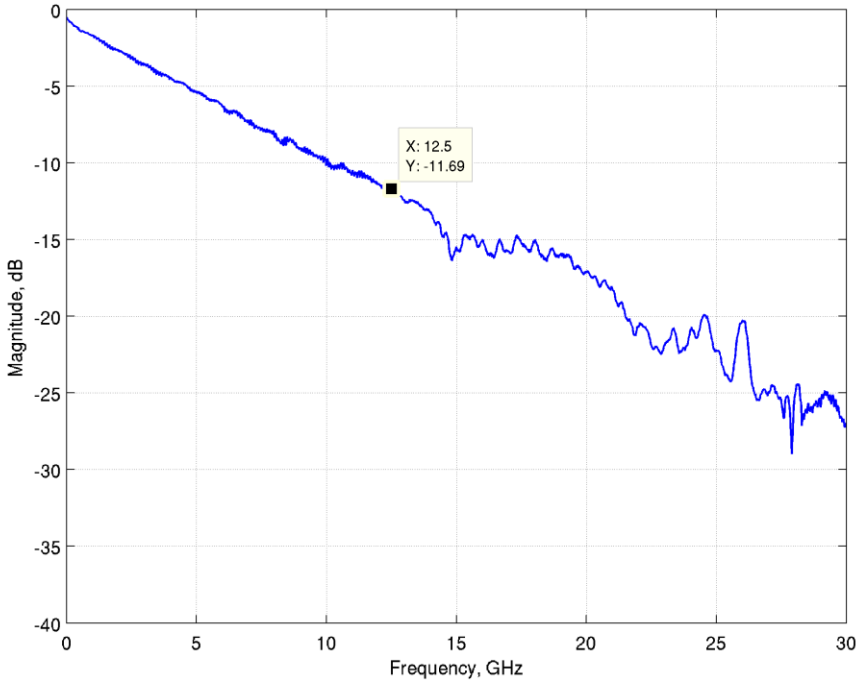




Measured results: Experiment #2

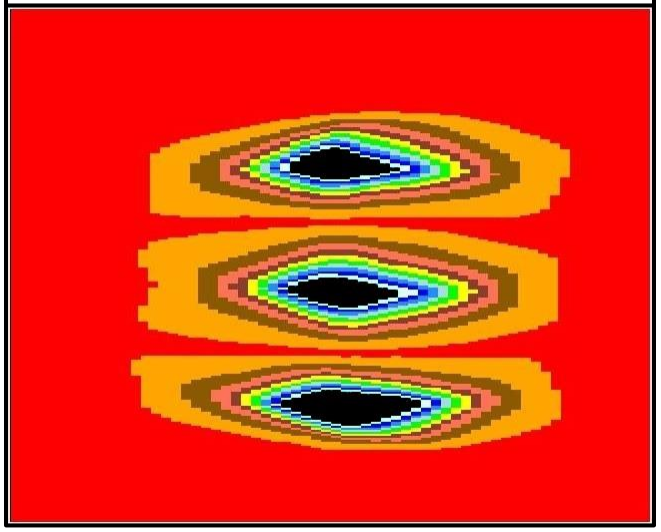


Differential insertion loss ~ 11.7 dB at 12.5 GHz



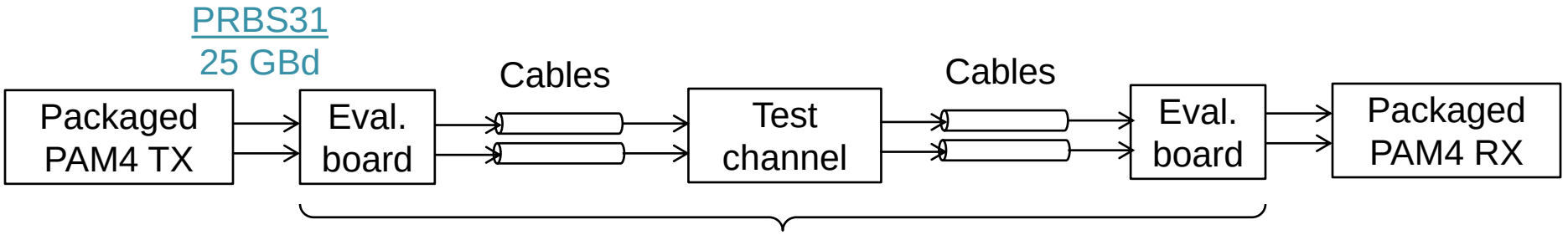
* No crosstalk was included in this experiment

RX internal eye plot

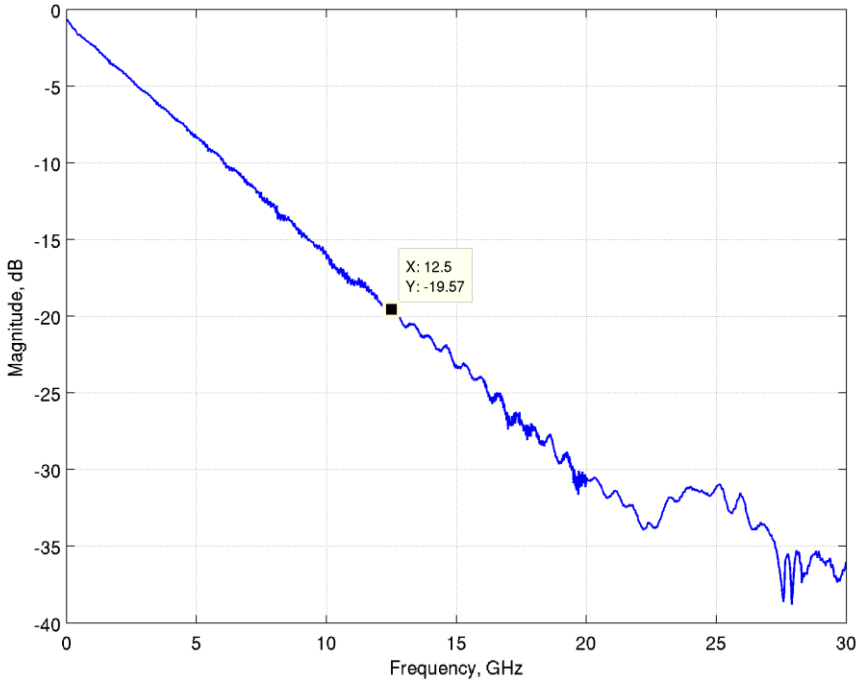


BER ~ 1.64E−11

Measured results: Experiment #3



Differential insertion loss ~ 19.6 dB at 12.5 GHz



* No crosstalk was included in this experiment

RX internal eye plot

Eye plot was not recorded for this experiment

BER ~ 7.64E−9

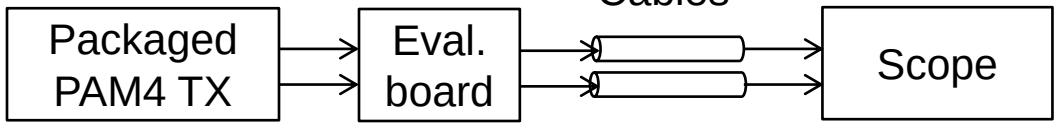
Simulation parameters

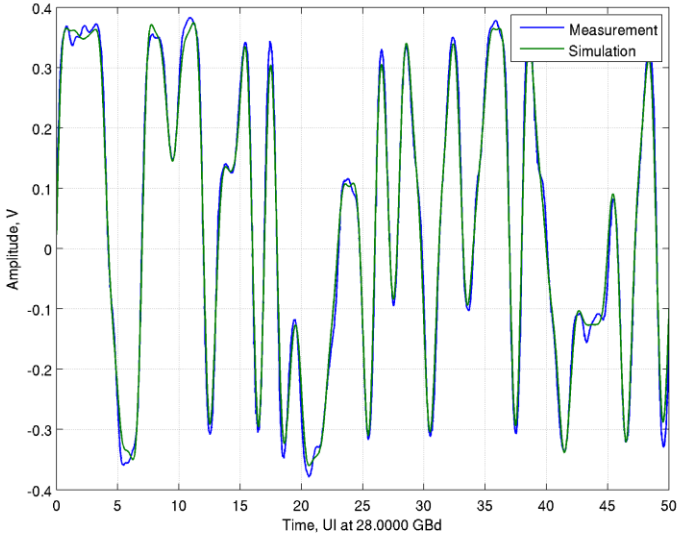
Transmitter parameter	Value
Equalizer	3-tap feed-forward equalizer 1 pre-cursor tap, 1 post-cursor tap Extracted from design
On-die termination	Extracted from design
Device package model	Extracted from design
Peak-to-peak deterministic jitter, ps	1.2 (sinusoidal)
RMS random jitter, ps	0.2

Receiver parameter	Value
Device package model	Extracted from design
On-die termination	Extracted from design
Input-referred noise power spectral density, dBm/Hz	−155
Equalizer	Continuous time linear equalizer Based on IEEE P802.3bm/D3.2 Annex 83E
Peak-to-peak deterministic jitter, ps	0
RMS random jitter, ps	0.2
Minimum latch overdrive, V	0

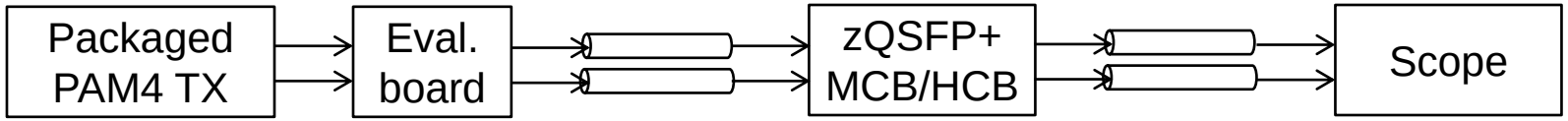
Compare simulation to measurement

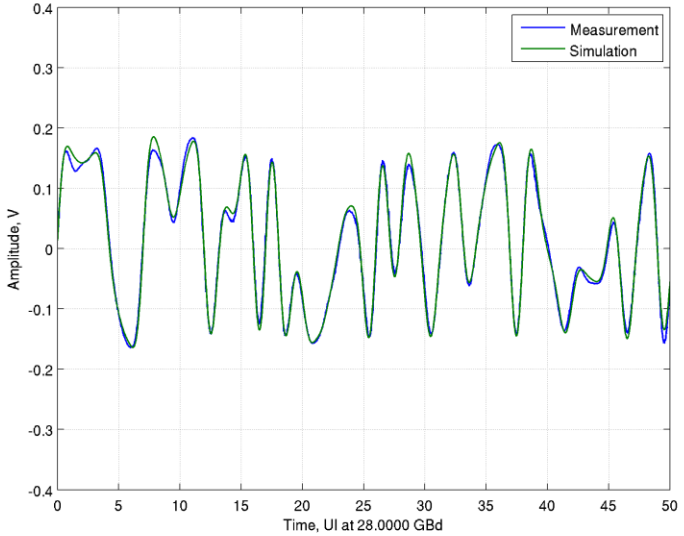
PRBS9
28 GBd



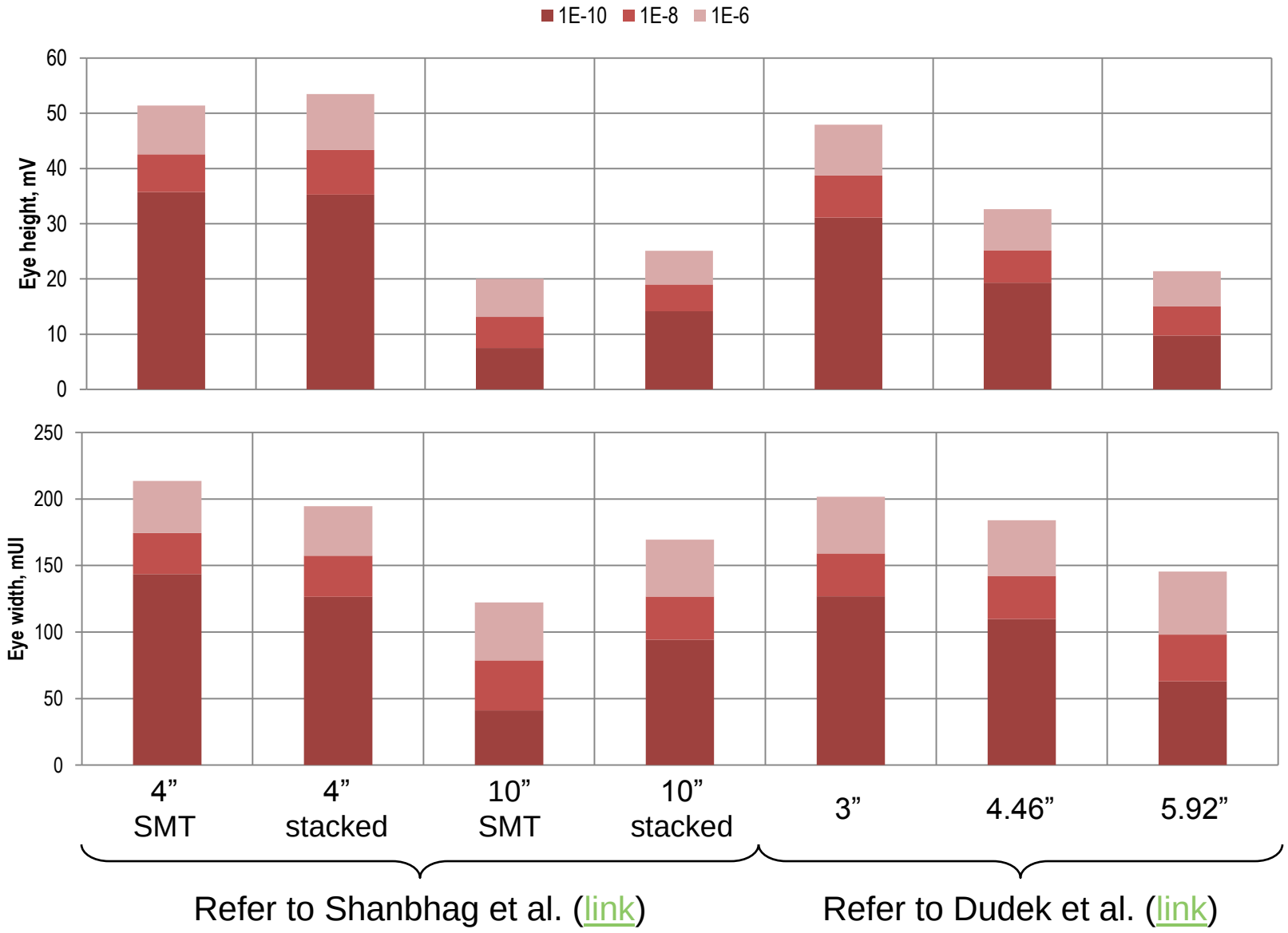


PRBS9
28 GBd





Summary of results: 28 GBd, including crosstalk



Power estimates

	28 GBd PAM2 (28 nm)		28 GBd PAM4 (16 nm)		
	Chip-module	“Long reach”	Chip-module	Chip-chip	“Long reach”
mW	x	1.7x	1.4x	1.7x	2.1x
pJ/bit	y	1.7y	0.7y	0.85y	1.05y

- Estimates should not be interpreted as a product roadmap
- Forward error correction not included
- Based on assumptions about channel loss and the required equalization capability

Summary

- Chip-to-chip and chip-to-module links using PAM4 are feasible
  - Demonstrated via simulation and measurement
  - It is possible to integrate many channels on a single die
- Channels can be similar to CAUI-4 targets
- Building block for future projects e.g., 40 or 50 Gb/s serial Ethernet

Additional observations

- There are advantages to having common modulation across chip-to-module, chip-to-chip, and longer reach links

- Historically, the chip-to-module links serve sockets that also accept direct attach [passive] copper cable
  - PAM4 more favorable for such longer reach (higher loss) links