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Supplementary Information on Nyquist-PAM4

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Technical Background

- Nyquist-shaped signals are widely used in digital communications (digital radio, UWB etc.), much resources are available for DSP implementations.

- Coherent DSP with Nyquist pulse shaping is studied and will appear soon.

Motivation

Based on the background and our own investigation, we would like to make following points clear;

- PAPR penalty
- Receiver timing recovery issues
- Tx and Rx DSP implementations
- Power and cost issues

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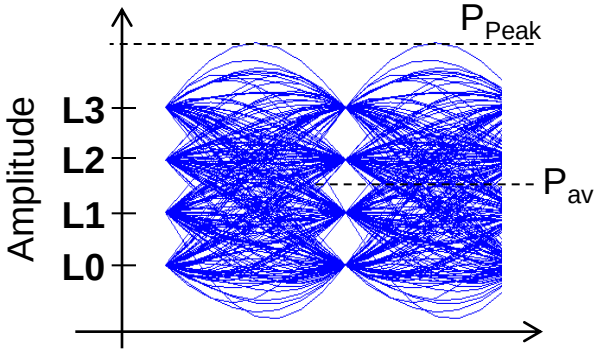
PAPR penalty

In cole_01_0914_smf and subsequent emails, it was pointed out that high PAPR results in excess penalty, as shown in the table below.

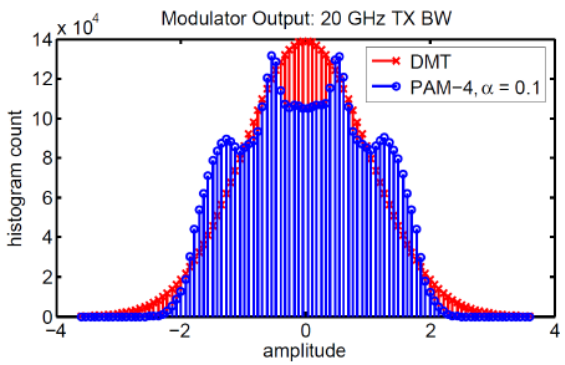
However, an assumption that was missed is that the channel is **bandwidth-limited** due to the narrow bandwidths of the components (i.e. 28-G TOSA/ROSA, ADC/DAC etc).

If this is taken into consideration, one can see that the PAPR penalty is easily offset by benefits elsewhere that result in an enhancement of the overall system budget.



$$PAPR_{opt} = \frac{\text{Peaked power}}{\text{Averaged Power}}$$

*** cole_01a_0814_smf**



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	Modulation penalty + $PAPR_{opt}$ penalty
50G NRZ	0 dB
100G PAM4	4.8 dB
100G Nyquist-PAM4	4.8 + 1.0 dB
100G DMT QAM-16	4.8 + 3.5 dB*

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ROI* of higher PAPR in band-limited channel

*Return On Investment

High PAPR is not just a waste of budget !

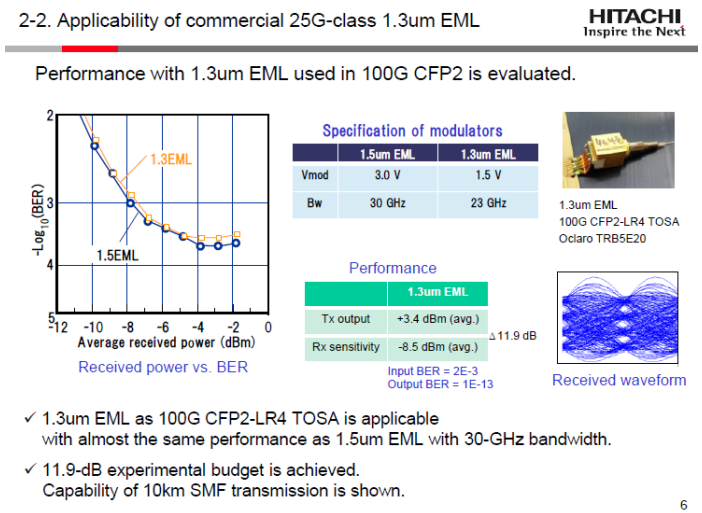
Investment :	- PAPR penalty
Return :	- Applicability of 28G-class devices and ADC/DAC ➡ Low cost, compatibility to 100GbE, etc - Better DSP and Rx sensitivity ➡ Increase of budget

Power budget of Nyquist-PAM4

In spite of ~1dB PAPR penalty, fairly large budget of 11.9 dB have been obtained experimentally with 28G-class devices.

✓2-km SMF PMD budget can be easily satisfied.

✓10-km SMF PMD budget is marginal, but may be satisfied by using APD or SOA.



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Conclusion

High PAPR surely causes some penalty in wide-band channel, however **by assuming band-limited channel**, overall system budget will rather increase with the advantages of using low cost devices.

	Modulation penalty + PAPR penalty	Advantage
100G Nyquist-PAM4	4.8 + 1.0 dB	•The use of 28G-class device •CD tolerance to bridge ~10km SMF transmission
100G DMT QAM-16	4.8 + 3.5 dB*	•The use of 10G-class device •CD tolerance to bridge ~40km SMF transmission*

*takahara_400_01_0114

Again, high PAPR is not just to waste budget in band-limited channels !

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*PD: Phase Detector

Receiver timing recovery issues in Nyquist PAM

- 1 sample per symbol (Ex. Mueller and Müller PD)
  Has especially lower phase error sensitivity at small rolloff

- 2 sample per symbol (Ex. Gardner PD)
  Has lower phase detector gain at small rolloff
  Faster processing required

Situation

- Nyquist pulse shaping has been widely used in electrical communications.

- Nyquist pulses with rolloff ~0.1 will be used in next-gen. coherent 16QAM systems to achieve very high spectral efficiency by rectangular spectral shaping.

Timing recovery of Nyquist pulse is **NOT a specific problem of this proposal**, and is widely studied even now.

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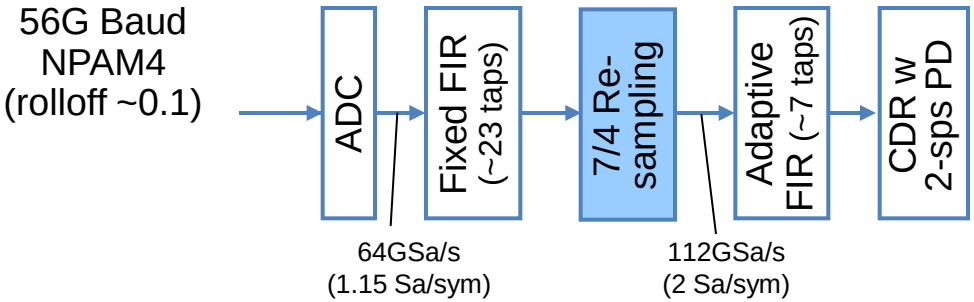
Example: Slight oversampling + 2-sps PD

- Safely use 2-sps without signal loss nor aliasing
- Small circuit size increment from 1-sps configuration (~ 7/4 re-sampling)



References: PDs for low-rolloff Nyquist pulses

[1] N. Stojanovic *et al.*, "Digital Phase Detector for Nyquist and Faster than Nyquist Systems", IEEE COMMUNICATIONS LETTERS, VOL. 18, NO. 3, MARCH 2014.

Use 90-degree shifted data w(t,T/2), instead of original x(t), as a input of a Gardner PD.

$$z(t) = x(t) + x(t + T/2)$$
$$w(t, T/2) = z(t)z^*(t + T/2)$$

[2] M. Yan *et al.*, "Digital clock recovery algorithm for Nyquist signal ", OFC/NFOEC, 2013, paper OTu2I.7.

Uses $x^2(t)$ as input of a Gardner PD.

PD: Phase Detector

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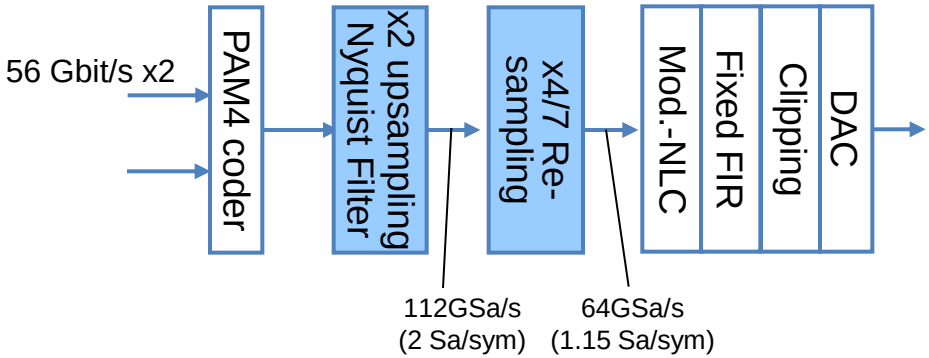
Detailed Tx-side DSP configuration

- In terms of circuit size, two new components added to digital PAM4, "Nyquist filter with x2 up-sampling" and "x4/7 re-sampling circuit"



Implementation options

- Two separate FIR filters (LUT or multiplier based)
- Combined FIR filters (LUT or multiplier based)
- Frequency domain

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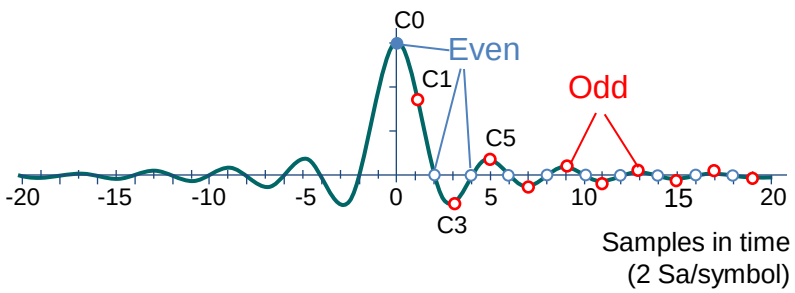
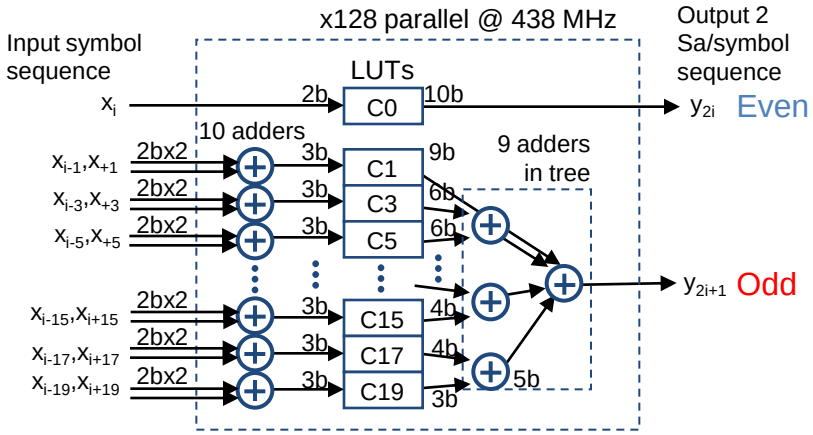
Nyquist filter with x2 up-sampling

- Number of taps may be ~39 in simulation, but
  - Nyquist filter is symmetry in time domain (two-fold implementation)
  - All the even taps except for a center tap are zero
  - Incoming data have just four levels (0,1,2,3)
  - Distant taps have smaller amplitude
- Employing these features, example 128-parallel LUT-based implementation (no multipliers) leads to estimated gate counts of ~0.3M



39-Tap Raised-cosine filter



Example circuit diagram

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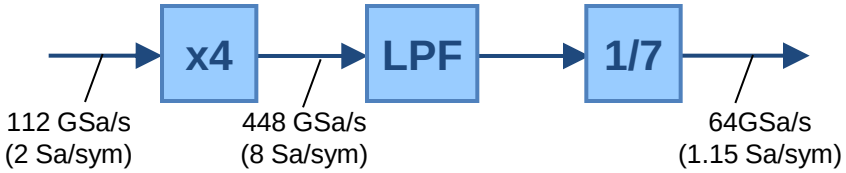
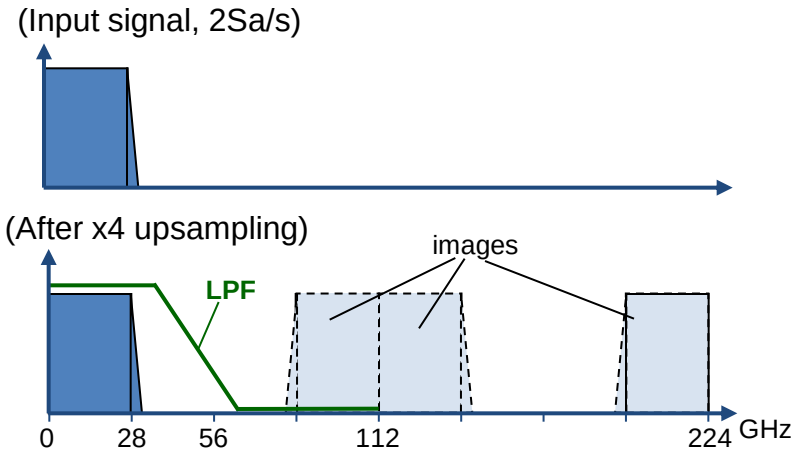
x4/7 re-sampling

- x4/7 re-sampling consists of x4 upsampling, brick-like LPF and 1/7 decimation
- 19-tap is enough for LPF because of separated signal and images.



x4/7 resampling configuration



Signal spectrum

- Poly-phase filter is know to be efficient to implement fractional re-sampling circuit.

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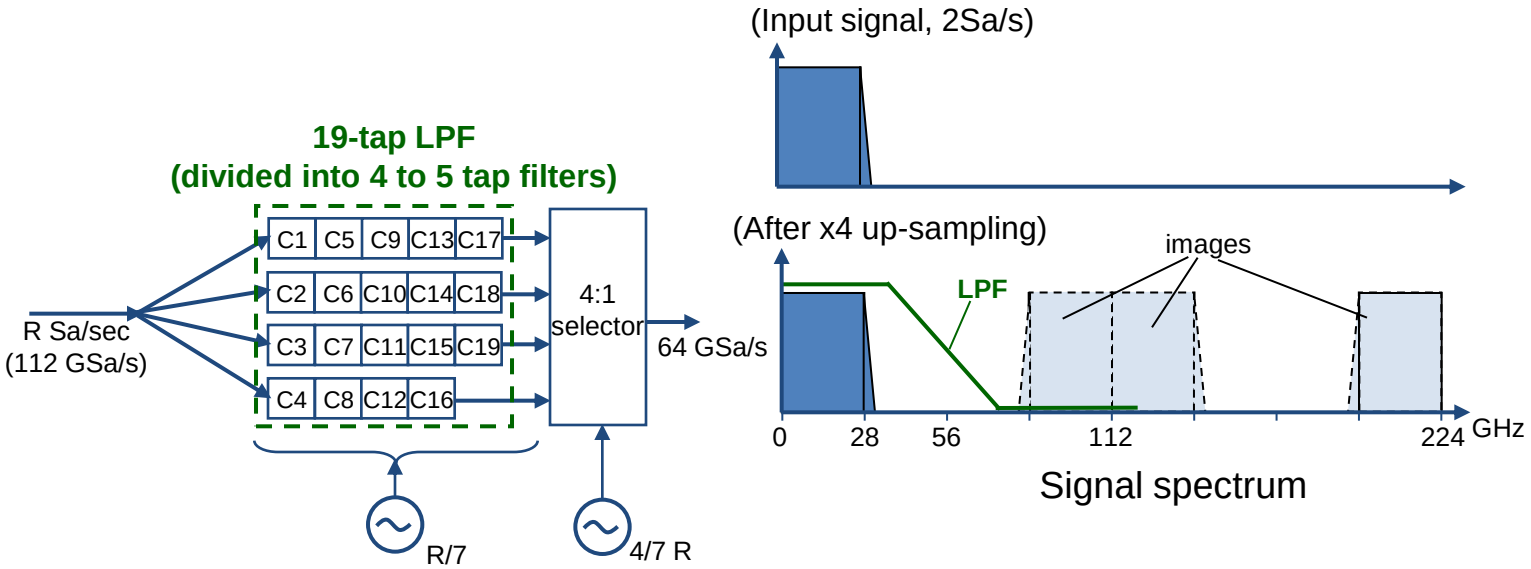
x4/7 Poly-phase filter

- x4 up-sampled signal is sparse, since three out of four samples are zero.
- Six out of seven samples are thrown away at 1/7 decimation.
- "Polyphase filter" is very efficient for re-sampling by calculating only valid output samples with non-zero taps.



- One of four FIR filter is active at a output sampling rate.
- Circuit size is equivalent to a 5-tap FIR filter running at 64 GSa/s (~0.3MGate).

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DSP implementation example

[3] R. Schmogrow *et al.*, "Digital Phase Detector for Nyquist and Faster than Nyquist Systems", *OpticsExpress*, Vol. 22, No. 1, Jan. 2014, p193-209.

- Real-time Tx DSP implementation for Nyquist 14-GBaud 16QAM.
- Use two Virtex-5 (XC5VFX200T), each for I and Q DSP.
- Implemented encoder, Nyquist filter (64 tap) and 4/3 re-sampling.
- 26% usage of LUTs of 2 FPGAs at 218MHz clock.

Circuit size estimation

- Very rough estimation suggests that 58G-Baud Nyqusit PAM requires almost the same circuit size (half of a Virtex-5 FPGA).
  - ... x4 for four-times baud rate
  - ... /2 for PAM4 instead of 16QAM
  - ... /2 for twice processing speed (436MHz) in ASIC
- Direct estimation of ASIC gate counts from FPGA circuit size is very difficult. But the number of FPGAs for the first-generation coherent PM-QPSK prototype (40 ~ 100 without CD compensation) also suggests that NPAM4 circuit size is quite small.

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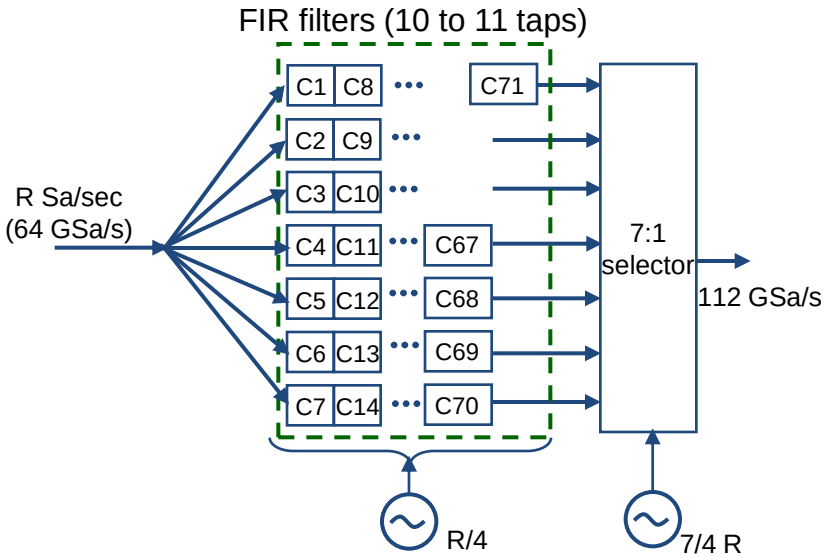
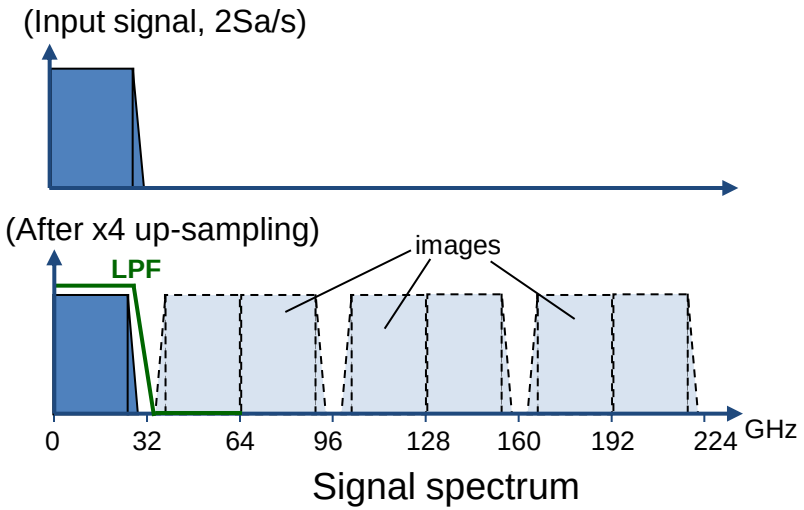
Rx-side x7/4 Poly-phase filter

- x7 up-sampled signal is very sparse, since three out of seven samples are zero.
- three out of four samples are thrown away at 1/4 decimation.
- Sharper LPF (~75 tap) is required to eliminate images.
- "Polyphase filter" implementation is shown below.





- One of seven FIR filter is active at a given sampling time.
- Circuit size is equivalent to a 10-tap FIR filter running at 112 GSa/s.

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Comparison with 50G/λ and other 100G/λ schemes

- 50G/λ is a good near-term solution, but its device cost will be more than two times (or more with wideband devices) of 100GbE at any instant into the future.

- 100G/λ will be a good long-term solution with nearly the same device cost with 100GbE. Especially band-limited design has power and cost advantages by using massively-deployed 100GbE devices.

- Introduction of DSP causes severe power and cost issues now, however, their quick reduction by the future CMOS process improvement is promised. In future, device power and cost will be dominant in 400GbE.

	100GbE	400GbE		
	25Gx4λ	50Gx8λ	100Gx4λ (wideband)	100Gx4λ (band-limited)
TOSA (EML)	4 ch	8 ch	4 ch	4 ch
Drivers	4 ch	8 ch	4 ch	4 ch
ROSA (PD+TIA)	4 ch	8 ch	4 ch	4 ch
WMUX/WDEMUX	4 ch	8 ch	4 ch	4 ch
Device power and cost	1	2+α	1+α	1

7. Conclusion

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✓Higher PAPR caused by band-limited PAM waveform requires some Tx-side power penalty, but it is a viable option for employing 28-G class low-cost 100GbE devices.

✓Timing recovery is not a big issue on Nyquist shaped signals

✓Tx- and Rx-side DSP implementations and their circuit size of Nyquist modulation are presented

✓100G/lambda scheme is advantageous in power and cost.
Especially band-limited one will have almost the same cost with 100GbE in future.

Thank you